Modeling Size Limitations of Resistive Crossbar Array With Cell Selectors

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***Abstract*— Due to recent developments in emerging memory technologies, resistive crossbar arrays have gained increasing importance. The size of the crossbar arrays is, however, limited due to challenges brought by the interconnect resistance, sneak path currents, and the physical area of the peripheral circuitry. In this paper, three figures of merit that characterize the limitations of resistive crossbar arrays with selectors are described, such as the driver resistance, voltage degradation across the cell, and read margin. The models, exhibiting good agreement with SPICE, are compared with different biasing schemes during both write and read operations. These models are also used to predict the device requirements of resistive crossbar arrays with selectors and to project parameter values, such as the nonlinearity factor, ON-state resistance, and tolerable interconnect resistance per cell for large-scale crossbar arrays.**

***Index Terms*— Crossbar array, emerging memory technologies, interconnect resistance, nonlinearity factor, sneak path leakage.**

I. Introduction

RESISTIVE crossbar arrays were developed before the invention of emerging memory technologies, such as MRAM, RRAM, and phase change memory (PCM) [1], [2]. With the recent development of RRAM devices [3], resistive crossbar arrays, for use in memory, have gained increasing popularity due to the advantages of $4F^2$ density and non-volatility. Existing analyses of resistive crossbar arrays show that the array size is limited by the degradation in read margin and voltage loss across the cells due to parasitic interconnect resistances, sneak path leakage currents, and ON–OFF resistance ratios [4]–[7]. These analyses have been primarily simulation-based. In [8], a matrix-based theoretical solution is presented for solving the voltages and currents of each cell within a crossbar array. This paper, however, does not provide intuitive models to support the design of resistive crossbar arrays due to the complexity of large arrays. Moreover, large matrix sizes are computationally complex. Therefore, simple analytic models that can intuitively characterize the limitations imposed on resistive crossbar arrays and project device and circuit requirements for large-scale arrays would be useful [9].

In this paper, three challenges in designing a resistive crossbar array are considered, such as the driver size, voltage degradation across the selected cell, and read margin. For each of these issues, models have been developed which provide intuition into the design of resistive crossbar arrays while also clarifying device requirements and limitations on the array size as interconnects continue to scale. These models are valid for both unipolar and bipolar memory elements. Moreover, different biasing schemes for writing and reading are compared to clarify possible advantages and design tradeoffs.

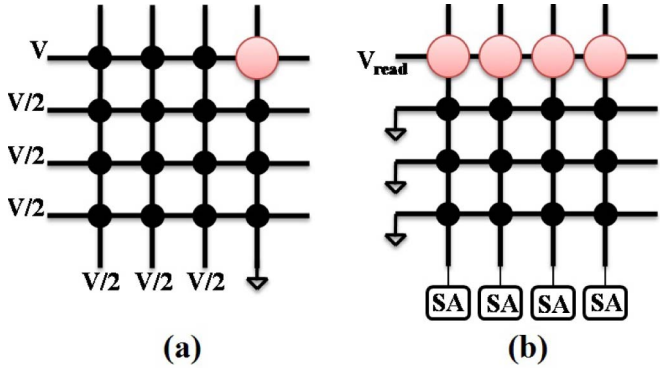

Fig. 1. Biasing scheme for a crossbar array when (a) writing to a cell and (b) reading from a cell.

In Section II, the models of the driver size, voltage degradation across the selected cell, and read margin are described and compared with simulation. In Section III, these models are considered under different biasing schemes to enhance nonlinearity and to mitigate size limitations. In Section IV, projected device requirements for large arrays are discussed. In Section V, an example of the application of the proposed models to the crossbar array design process is demonstrated. In Section VI, some conclusions are offered.

II. Models of Crossbar Array Design Parameters

Expressions that model three primary design parameters of resistive crossbar arrays, such as the driver size, voltage degradation across the selected cell, and read margin are introduced in this section. For simplicity, an equal number of rows and columns are assumed under worst case conditions. For the write operation, the $V/2$ biasing scheme [10] is considered. For the read operation, the scheme in which a read voltage is applied to the selected row while connecting the remaining portion of the rows to ground and the columns to sense amplifiers [11] is considered, as shown in Fig. 1. In Sections II-A–II-C, the driver resistance, voltage degradation across the selected cell, and read margin are discussed.

A. Driver Size

An important advantage of a crossbar structure in memory systems is physical density. Resistive crossbar arrays,

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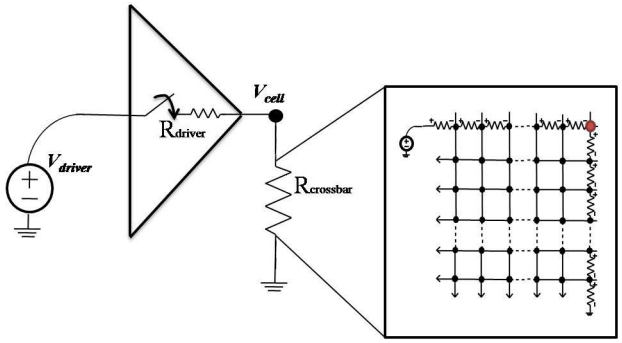

Fig. 2. Driver circuit.

however, require large peripheral circuits due to the high current required to drive large arrays of closely packed devices. The physical area of a crossbar array is ultimately determined by the cell size and the peripheral circuitry, as well as the drivers.

The driver resistance is the output resistance of the driving circuit, as shown in Fig. 2. This output resistance depends upon the input resistance of the selected row as well as the voltage drop across the selected cell. Although the lower bound on the resistance of a single memory element could reach tens of kilohms in an RRAM crossbar structure, the effective resistance between the driver at a selected row and the sense amplifier at a selected column(s) drastically decreases with a larger array size. Since the effective resistance is also dependent on the number of selected cells, the driver resistance varies depending upon whether a read or write operation is executed. In this analysis, the interconnect resistance and the input resistance of the sense amplifier are considered to be negligible.

For a write operation, the worst case condition occurs when the selected cell is initially in the ON-state and switches to the OFF-state. Since selector devices are in series with the resistive memory elements, a nonlinear relationship between the cell voltage and current exists. Hence, the resistance of each cell varies nonlinearly with the voltage across the cell. This nonlinearity is described by the nonlinearity factor. For a worst case analysis, in which the highest current is required by the crossbar array, half-selected cells are assumed to be in the ON-state. Based on these assumptions, the following expression for the driver resistance at the selected row is

$$R_{\text{driver(write)}} = \frac{R_{\text{ON}}\left(\frac{V_{\text{driver}}}{V_{\text{cell}}} - 1\right)}{\frac{N-1}{K_r} + 1} \tag{1}$$

where R_{ON} is the resistance of a memory cell (the selector and resistive memory element) in the ON-state, V_{driver} is the driver output voltage when the driver resistance is zero, V_{cell} is the voltage drop across the selected cell, N is the array size (the number of rows or columns), and K_r is the nonlinearity factor

$$K_r = \frac{I_{\text{cell}}(V_{\text{write}})}{I_{\text{cell}}(V_{\text{write}}/2)} = 2 \times \frac{R_{\text{ON at } V_{\text{write}}/2}}{R_{\text{ON}}} \tag{2}$$

where $R_{\text{ON at } V_{\text{write}}/2}$ is the ON-state cell resistance when the voltage across the cell (V_{cell}) equals half of the write voltage. K_r is the ratio of the current flowing through the selected cell to the current flowing through the half-selected cell. The nonlinearity factor characterizes to what extent the current flowing into the unselected columns compares with the current flowing into the selected column.

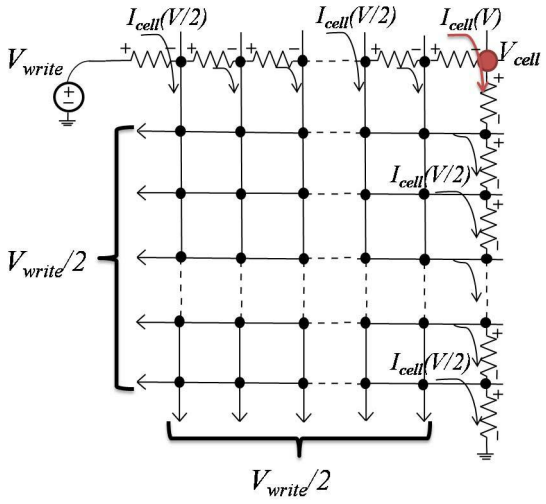

Fig. 3. Circuit model of a crossbar array during a write operation.

For the case where multiple devices are selected, as in the case of a read operation, the constraint on the driver resistance becomes more stringent. During a single read operation, all of the cells on the selected row are selected. Considering the worst case condition when all of the selected cells are in the ON-state, the driver resistance is

$$R_{\text{driver(read)}} = \frac{R_{\text{ON}}\left(\frac{V_{\text{driver}}}{V_{\text{cell}}} - 1\right)}{N}. \tag{3}$$

The driver resistance during a read operation is independent of the selector devices and inversely proportional to the size of the crossbar array.

B. Voltage Degradation Across Selected Cell

An important limitation on the size of a resistive crossbar array is the interconnect resistance. With interconnect scaling, the resistance per cell has drastically increased, reaching 2.5 Ω for the 22-nm node [12]. It is, therefore, crucial to consider the effects of parasitic resistance when executing an operation. The worst case selected cell is farthest from the driver on the selected row and farthest from ground on the selected column. For low nonlinearity factors, since the difference in resistance of a half-selected cell in the ON- and OFF-states remains significant, voltage degradation is data pattern dependent. To consider the worst case voltage degradation, all half-selected cells and the selected cell are assumed to be in the ON-state. The indicated cell shown in Fig. 1(a) is an example of a worst case cell for a 4×4 crossbar array during a write operation.

For writing, a circuit model of a crossbar array that includes the interconnect resistance along the selected row and column is considered. Furthermore, in this model, it is assumed that equal current flows through the half-selected cells between the selected row and the unselected columns, as shown in Fig. 3.

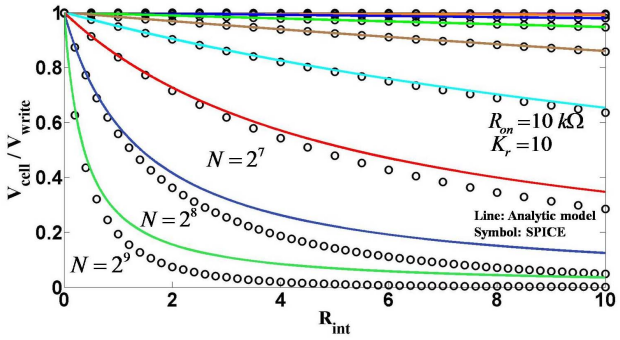

Fig. 4. Ratio of the voltage drop across the worst case selected cell to the driver voltage during a write operation.

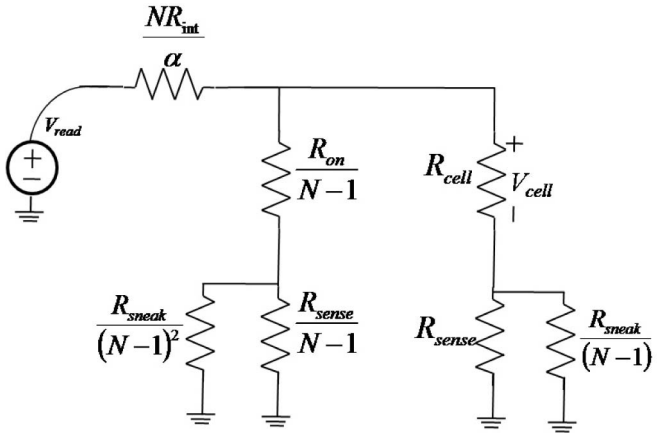

Fig. 5. Circuit model of the crossbar array during a read operation, where R_{sense} is the input resistance of the sense amplifier and R_{sneak} is the sneak path resistance of the resistive memory cells between the (un)selected column(s) and the unselected rows.

Based on this assumption, the voltage across the worst case selected cell is

$$\frac{V_{\text{cell}}}{V_{\text{write}}} = \frac{1}{\frac{NR_{\text{int}}}{R_{\text{ON}}}\left(\frac{N-1}{K_r}+2\right)+1} \tag{4}$$

where R_{int} is the interconnect resistance per cell. As shown in Fig. 4, (4) agrees with SPICE, exhibiting a maximum error of 6.5% for voltage ratios above 0.5. Increasing interconnect resistance per cell decreases the voltage across the selected cell due to IR losses. This degradation becomes more severe and nonlinear as the array size scales. This behavior is due to increased current flow into the selected row and column with increasing number of rows and columns. Since the number of half-selected cells increases with a larger array size, the total current flowing into both the selected row and column increases. Larger array sizes, therefore, exacerbate the voltage degradation across the selected cell due to increased current flow and interconnect resistance.

For reading, a circuit model of a crossbar array is shown in Fig. 5. The worst case cell for the read case is farthest from the driver on the selected row and farthest from the sense amplifiers on the selected columns. Since all of the cells in the same row are selected, any voltage degradation is data pattern dependent. The worst case condition occurs when all of the

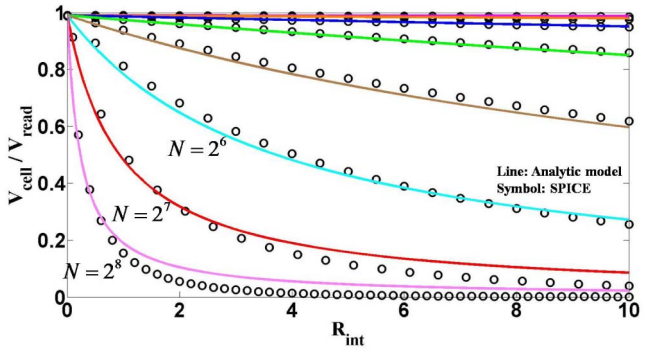

Fig. 6. Ratio of the voltage drop across the worst case selected cell to the driver voltage during a read operation.

TABLE I
PARAMETERS FOR READ OPERATION

Parameters	Values
R_{on}	10 kΩ
α	1.5
R_{sense}	100 Ω
R_{sneak}	$\frac{K_r}{2}\times R_{on}$
R_{off}	10 MΩ
K_r	2×10^3
R_{tran}	R_{on}

cells on the selected row are ON, including R_{cell}. Based on the circuit model shown in Fig. 5, the ratio of the worst case cell voltage to the read voltage is

$$\frac{V_{\text{cell}}}{V_{\text{read}}} = \frac{1}{\left(1+\frac{N^2R_{\text{int}}}{\alpha R_{\text{sel}(L)}}\right)\left(1+\frac{1}{R_{\text{ON}}\left(\frac{1}{R_{\text{sense}}}+\frac{N-1}{R_{\text{sneak}}}\right)}\right)} \tag{5}$$

where R_{sense} is the input resistance of the sense amplifier, R_{sneak} is the resistance of the cells between the (un)selected column(s) and the unselected rows, α is a fitting parameter, and $R_{\text{sel}(L)}$ is

$$R_{\text{sel}(L)} = R_{\text{ON}} + \left(\frac{R_{\text{sneak}}}{N-1}||R_{\text{sense}}\right). \tag{6}$$

Expression (5) agrees with SPICE, exhibiting a maximum error of 6.6% for voltage ratios above 0.25, as shown in Fig. 6 (based on the parameter values of R_{ON}, α, R_{sense}, and R_{sneak} listed in Table I). Similar to the degradation in cell voltage during a write operation, a larger interconnect resistance increases IR losses, which is further exacerbated with a larger array size. The degradation is more severe during a read operation, since the selection of a single row causes a full read voltage to drop across all of the cells in that row. All of the cells in the selected rows are, therefore, selected as opposed to selecting a single cell during a write operation.

Note that the value of R_{sneak} listed in Table I depends upon the voltage drop across the sense amplifier. It is assumed that the voltage drop is below the threshold voltage of the cell selector. The input resistance R_{sense} needs to be sufficiently low to maintain a low voltage at the sensing end of the columns, which is ideally grounded. This low input resistance

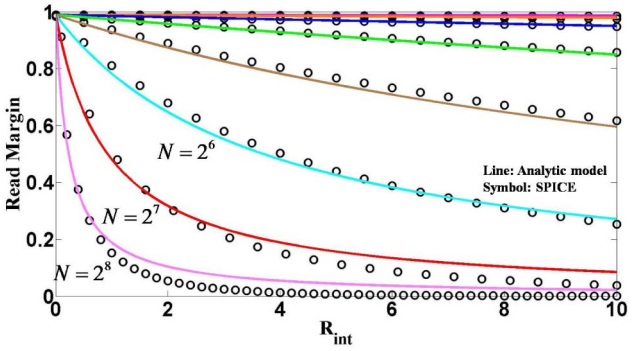

Fig. 7. Comparison of the read margin between the analytic model and simulation.

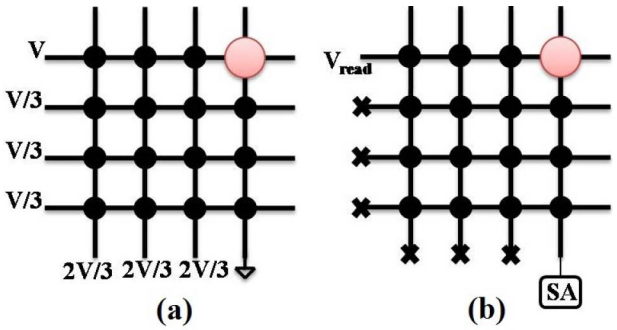

Fig. 8. Enhancing cell nonlinearity for (a) write operation with $V/3$ biasing scheme, and (b) read operation with floating biasing scheme.

requirement imposes a serious challenge on the design of the sense amplifiers.

C. Read Margin

An important figure of merit that determines the ability of a sense amplifier to distinguish between two states is the read margin. The read margin is

$$\text{Read margin} = \frac{(I_{\text{sense}(L)} - I_{\text{sense}(H)})R_{\text{tran}}}{V_{\text{read}}} \tag{7}$$

where R_{tran} is the transresistance of the sense amplifier, which is matched to R_{ON}, $I_{\text{sense}(L)}$ is the current flowing into the sense amplifier when the target cell is ON, and $I_{\text{sense}(H)}$ is the current flowing into the sense amplifier when the target cell is OFF. The worst case read margin occurs when reading an ON-state when all of the cells along the selected row are ON, and when reading an OFF-state when all of the cells along the selected row are OFF. In the worst case condition, the selected row is farthest from the sense amplifiers [see Fig. 1(b)]. Based on these worst case conditions and the circuit model shown in Fig. 5, $I_{\text{sense}(L)}$ and $I_{\text{sense}(H)}$ are described, respectively, as

$$I_{\text{sense}(L)} = \frac{V_{\text{read}}}{R_{\text{ON}}R_{\text{sense}}\left(\frac{1}{R_{\text{sense}}} + \frac{1}{R_{\text{ON}}} + \frac{N-1}{R_{\text{sneak}}}\right)\left(1 + \frac{N^2 R_{\text{int}}}{\alpha R_{\text{sel}(L)}}\right)} \tag{8}$$

$$I_{\text{sense}(H)} = \frac{V_{\text{read}}}{R_{\text{OFF}}R_{\text{sense}}\left(\frac{1}{R_{\text{sense}}} + \frac{1}{R_{\text{OFF}}} + \frac{N-1}{R_{\text{sneak}}}\right)\left(1 + \frac{N^2 R_{\text{int}}}{\alpha R_{\text{sel}(H)}}\right)} \tag{9}$$

where R_{OFF} is the resistance of a memory cell in the OFF-state, and $R_{\text{sel}(H)}$ is

$$R_{\text{sel}(H)} = R_{\text{OFF}} + \left(\frac{R_{\text{sneak}}}{(N-1)} || R_{\text{sense}}\right). \tag{10}$$

Expression (7), based on the expressions of $I_{\text{sense}(L)}$ and $I_{\text{sense}(H)}$ in, respectively, (8) and (9), agrees with SPICE, exhibiting a maximum error of 6.6% for read margins above 0.25 based on the parameter values listed in Table I, as shown in Fig. 7.

Note the degradation in voltage across the cell with increasing array size (or interconnect resistance), which can fall below the threshold voltage of the selector. The selector resistance can dominate the overall memory cell resistance, making the ON- and OFF-states indistinguishable. It is, therefore, crucial to consider the threshold voltage of the selector when estimating the read margin or voltage drop across a cell.

The results shown in Figs. 4, 6, and 7 illustrate the sensitivity of the write and read operations to increasing the interconnect resistance and the array size. This sensitivity is more acute for the read case, since cell nonlinearity at the selected row is not exploited due to selecting an entire row. For small array sizes, the interconnect resistance reduces the read margin due to IR losses across the interconnects and the ineffectiveness of the cell selectors in this particular biasing scheme. To reduce the effect of the interconnect resistance to mitigate both the read margin and the voltage degradation, higher nonlinearity factors are required. A different biasing scheme for read and write, therefore, needs to be considered. In Section III, the biasing scheme proposed in [4], based on floating unselected rows and columns of an array, is applied to the read operation, while the biasing scheme proposed in [10], based on applying one third of a write voltage across the unselected cells to enhance the nonlinearity factor, is applied to the write operation.

III. Enhancement of Nonlinearity Factor

Models for the driver resistance, worst case voltage drop, and read margin are provided in this section for the aforementioned floating scheme during a read operation [4] and $V/3$ during a write operation [10]. The biasing schemes are shown in Fig. 8. During a write operation, one third of the write voltage is applied to the unselected columns when grounding the selected column, and two thirds of the write voltage are applied to the unselected rows when applying a full write voltage to the selected row. The benefit of this biasing scheme is that only one third of the write voltage is across the half-selected cells during a write operation rather than half of the write voltage. The nonlinearity factor is, therefore, much higher and typically on the order of 10^3–10^4 [13]–[15]. A nonlinearity factor as high as 10^7 has been demonstrated [16]. Moreover, due to the decreased voltage across the half-selected cells [from $(V/2)$ to $(V/3)$], the write disturbance improves [17]. One third of the write voltage is across the remaining unselected cells, as compared with the previous case (ideally, zero voltage drop), possibly

increasing the leakage current. The current flowing through the unselected rows and columns is, however, greatly reduced due to the higher nonlinearity factor. The advantage of the $V/3$ biasing scheme is, therefore, only beneficial with high nonlinearity factors. A high nonlinearity factor needs to be sufficiently high to suppress the current flowing through the unselected rows and columns, ensuring that the effect of the interconnect resistance and, therefore, the IR losses is negligible.

During a read operation, a read voltage is applied to the selected row while connecting the selected column to the sense amplifier and floating the unselected rows and columns. The cell selectors effectively suppress the current flowing through the selected row, thereby reducing IR losses, since half of the read voltage is dropped across the unselected cells at the selected row and column. However, as compared with the grounded biasing scheme [see Fig. 1(b)], only a single cell can be read at a time.

In Sections III-A to III-C, models for the driver resistance, worst case voltage drop, and read margin are provided for the biasing schemes shown in Fig. 8. These models provide intuition while characterizing the limitations of the crossbar array and estimating the requirements for the device parameters (K_r, R_{ON}, and R_{OFF}).

A. Driver Size

For the same worst case conditions assumed for $R_{\mathrm{driver(write)}}$ and $R_{\mathrm{driver(read)}}$, as described in Section II, the driver resistance during a write operation under a $V/3$ biasing scheme and a read operation with a floating biasing scheme is, respectively

$$R_{\mathrm{driver(write\_}V/3)} = \frac{R_{\mathrm{ON}}\left(\frac{V_{\mathrm{driver}}}{V_{\mathrm{cell}}}-1\right)}{\frac{N-1}{K_{r(\mathrm{write})}}+1} \tag{11}$$

$$R_{\mathrm{driver(read\_float)}} = \frac{R_{\mathrm{ON}}\left(\frac{V_{\mathrm{driver}}}{V_{\mathrm{cell}}}-1\right)}{\frac{N-1}{K_{r(\mathrm{read})}}+1} \tag{12}$$

where $K_{r(\mathrm{write})}$ and $K_{r(\mathrm{read})}$ are, respectively

$$K_{r(\mathrm{write})} = \frac{I_{\mathrm{cell}}(V_{\mathrm{write}})}{I_{\mathrm{cell}}(V_{\mathrm{write}}/3)} = 3\times\frac{R_{\mathrm{ON}\ |V_{\mathrm{write}}/3}}{R_{\mathrm{ON}}} \tag{13}$$

$$K_{r(\mathrm{read})} = \frac{I_{\mathrm{cell}}(V_{\mathrm{read}})}{I_{\mathrm{cell}}(V_{\mathrm{read}}/2)} = 2\times\frac{R_{\mathrm{ON}\ |V_{\mathrm{read}}/2}}{R_{\mathrm{ON}}} \tag{14}$$

where $R_{\mathrm{ON}\ |V_{\mathrm{write}}/3}$ and $R_{\mathrm{ON}\ |V_{\mathrm{read}}/2}$ are the ON-state cell resistances when the voltage across the cell equals to, respectively, one third of the write voltage and half of the read voltage. Unlike the driver resistance for reading with the grounded biasing scheme, cell selectors are used. Moreover, since the read operation uses lower voltages as compared with the write operation, the nonlinearity factor is higher than K_r, as described by (2). Similarly, the driver resistance during a write operation under the $V/3$ biasing scheme is also greatly enhanced due to the increased nonlinearity factor. The degradation of the driver resistance with increasing array size is, therefore, not as severe as the biasing schemes described in Section II.

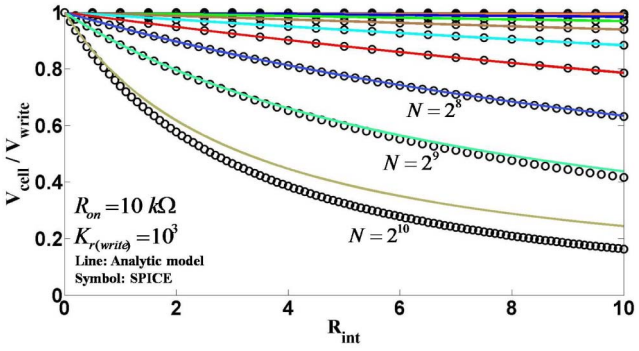

Fig. 9. Ratio of the voltage drop across the worst case selected cell to the driver voltage during a write operation under the $V/3$ biasing scheme.

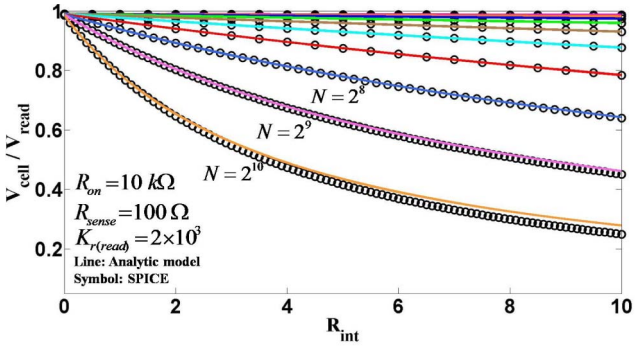

Fig. 10. Ratio of the voltage drop across the worst case selected cell to the driver voltage during a read operation under the floating biasing scheme.

B. Voltage Degradation Across Selected Cell

To determine the worst case voltage drop across the selected cell, the cell farthest from the write (read) voltage source at the selected row and farthest from the ground (sense amplifier) at the selected column is evaluated, as shown in Fig. 8. The voltage drop across the worst case selected cell during the write and read operation is, respectively,

$$\frac{V_{\mathrm{cell}}}{V_{\mathrm{write}}} = \frac{1}{\frac{NR_{\mathrm{int}}}{R_{\mathrm{ON}}}\left(\frac{N-1}{K_{r(\mathrm{write})}}+2\right)+1} \tag{15}$$

$$\frac{V_{\mathrm{cell}}}{V_{\mathrm{read\_float}}} = \frac{1}{1+\left(N\frac{R_{\mathrm{int}}}{R_{\mathrm{ON}}}\left(2+\frac{N-1}{K_{r(\mathrm{read})}}\right)\right)+\left(\frac{R_{\mathrm{sense}}}{R_{\mathrm{ON}}}\left(1+\frac{N-1}{K_{r(\mathrm{read})}}\right)\right)}. \tag{16}$$

The models provided in (15) and (16) are in good agreement with SPICE, exhibiting a maximum error of, respectively, 10% for voltage ratios above 0.5, and 6.6% for voltage ratios above 0.35, as shown, respectively, in Figs. 9 and 10.

As the nonlinearity factor decreases, the accuracy of these models also decreases. Hence, (4) is relatively less accurate as compared with (15) and (16). This inaccuracy is due to ignoring the parasitic interconnect resistance along the unselected rows and columns. As the nonlinearity factor increases, the current flow through those lines decreases, making the

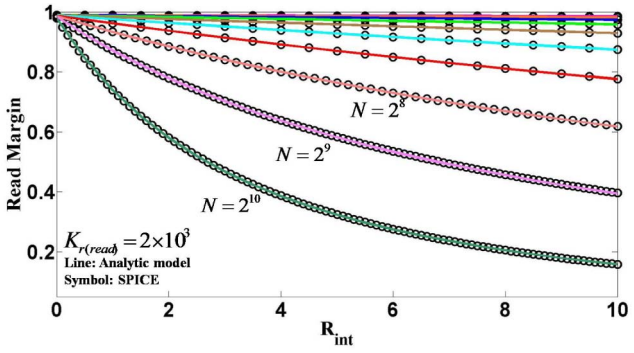

Fig. 11. Comparison of the read margin between the model and simulation for the floating biasing scheme.

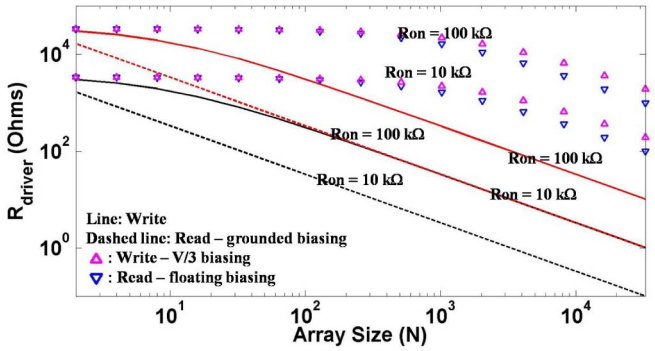

Fig. 12. Analytic model of driver resistance with respect to varying array sizes for $K_r = 10$, $K_{r(\text{write})} = 2 \times 10^3$, and $K_{r(\text{read})} = 10^3$ that satisfies $(V_{\text{driver}}/V_{\text{read}}) = (4/3)$.

parasitic interconnect resistance and, hence, the IR losses negligible.

C. Read Margin

Expression (7) is used to evaluate the read margin, where $I_{\text{sense}(L)}$ and $I_{\text{sense}(H)}$ are, respectively,

$$I_{\text{sense}(L)\_\text{float}} = \frac{V_{\text{read}}}{NR_{\text{int}} + R_{\text{sense}} + \frac{1}{\frac{1}{R_{\text{ON}}+NR_{\text{int}}} + \frac{N-1}{K_{r(\text{read})}R_{\text{ON}}}}} \quad (17)$$

$$I_{\text{sense}(H)\_\text{float}} = \frac{V_{\text{read}}}{NR_{\text{int}} + R_{\text{sense}} + \frac{1}{\frac{1}{R_{\text{OFF}}+NR_{\text{int}}} + \frac{N-1}{K_{r(\text{read})}R_{\text{ON}}}}}. \quad (18)$$

Assuming all of the cell selectors are OFF, the resistance is dominated by the selector resistance. The worst case condition becomes data pattern independent, since a single cell is selected, while the other cells are at a high resistance. Based on this condition, (17) and (18) exhibit good agreement with SPICE, exhibiting a maximum error of 0.12% (based on the parameters listed in Table I), as shown in Fig. 11.

IV. Design Requirements for Varying Array Size

An important aspect of these models is computational efficiency while providing physical intuition into crucial parameters, such as K_r, R_{ON}, R_{driver}, R_{int}, R_{sense}, and N during the design process of a crossbar array. The area of the drivers (R_{driver} dependent), process technology (R_{int} dependent), and device requirements (K_r and R_{ON} dependent) can be extracted for a target crossbar array size N. Moreover, these models describe the device and circuit requirements for scaled array sizes and interconnect resistance. In this section, design requirements for large arrays are projected.

A. Driver Resistance

The driver resistance during both read and write operations based on the biasing schemes described in Sections II and III for different array sizes is shown in Fig. 12.

From Fig. 12, the driver resistance during a read operation based on the grounded biasing scheme should be below 10 Ω for a large-scale crossbar array (>1 Mb) with an R_{ON} of 10,000 Ω for a V_{driver} to V_{read} ratio of 4/3. This severe degradation in driver resistance is due to the connection of N resistive devices in parallel with a full read voltage across them. This stringent constraint requires a large area dedicated to the peripheral circuitry, degrading the $4F^2$ density advantage of RRAM crossbar arrays. Due to the grounded biasing scheme during a read operation, the read voltage across a single cell selects all of the other cells on the same row, causing the input resistance of the selected row to be inversely proportional to the array size. By choosing the floating biasing scheme, shown in Fig. 8(b), the required driver resistance is greatly increased. Reading a single cell in a specific row does not require the other cells on that row to be read, since the untargeted cells are half selected and undisturbed due to the cell selectors.

During a write operation under the $V/2$ biasing scheme, due to the nonlinearity of the selector devices, the half-selected cell remains at a higher resistance. The input resistance is, therefore, much higher as compared with reading with the grounded biasing scheme. The input resistance, however, is much lower as compared with reading with the floating biasing scheme. This behavior occurs since the nonlinearity factor decreases when the operating voltage increases when switching from the read voltage to the write voltage. For the same reason, the driver resistance during a write operation under the $V/3$ biasing scheme becomes higher, since the nonlinearity factor increases due to the greater voltage difference between the unselected cells and the selected cells ($2V/3$) despite the higher write voltages.

B. Voltage Degradation and Device Nonlinearity

An implication of (15) and (16) is that a high nonlinearity factor is insufficient in large crossbar arrays. Nonlinearity factors are typically on the order of 10^3–10^4. Hence, a significantly high R_{ON} is essential for large crossbar arrays to maintain a reasonable ratio between the cell voltage and the read/write voltage. These qualities are shown in Fig. 13. A nonlinearity factor greater than 10^4 only slightly improves the voltage across the worst case selected cell. Beyond 10^4, a higher R_{ON} is required to produce a larger voltage across the selected cell.

C. Read Operation

Considering the read margin when using the grounded biasing scheme, the denominator of (5), (8), and (9) consists

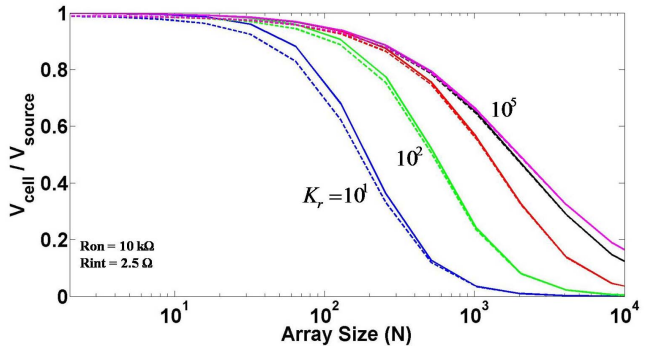

Fig. 13. Voltage degradation versus array size, where $V_{\text{source}} = V_{\text{write}}$ (solid lines) and $V_{\text{source}} = V_{\text{read}}$ (dashed lines). $R_{\text{sense}} = 100\ \Omega$.

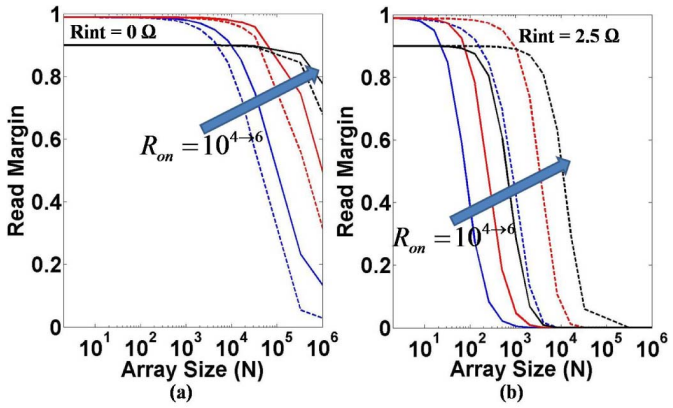

Fig. 14. Read margin with respect to array size based on the parameters listed in Table I for (a) $R_{\text{int}} = 0\ \Omega$, and (b) $R_{\text{int}} = 2.5\ \Omega$. The solid lines describe the grounded biasing scheme, whereas the dashed lines describe the floating biasing scheme.

of two different parts. One part considers the loss due to the interconnect resistance, while the other part considers the loss due to sneak path currents. The resistance between the selected column and unselected rows R_{sneak} creates a sneak path. Since a voltage exists at the node that connects the column to the sense amplifier, the current flowing through the selected cell is partially lost due to the current flow through R_{sneak}. This loss caused by the sneak path, however, has a negligible effect on the read margin, since R_{sneak} remains at a high resistance due to the small voltage across the sense amplifier. Degradation in the read margin is, therefore, primarily due to IR losses across the interconnect rather than sneak current paths. When using the open-circuit biasing scheme, however, any degradation in the read margin is primarily due to sneak path leakage current rather than due to IR losses, as shown in Fig. 14. Since the sneak current path is the dominant factor for read margin degradation under the open-circuit biasing scheme, for negligible interconnect resistances, the grounded biasing scheme performs better [see Fig. 14(a)]. For significant interconnect resistance, however, since IR losses is the dominant factor for read margin degradation under the grounded biasing scheme, the open-circuit biasing scheme performs better. With the open-circuit biasing scheme, the read margin increases by 3.4 times for a small array size ($N = 128$), and as much as 85 times for larger array sizes ($N = 1024$) for $R_{\text{ON}} = 10,000$, as compared with the grounded biasing scheme [see Fig. 14(b)].

TABLE II
DESIGN PARAMETERS

Values from [13]		Circuit level choices	
Parameters	**Value**	**Parameters**	**Value**
R_{on}	24 kΩ	R_{sense}	100 Ω
R_{off}	1.5 MΩ	R_{tran}	R_{on}
$K_{r(read)}$	1000	Tolerable Read Margin	0.5
$K_{r(write)}$	1100	Tolerable $\frac{V_{cell}}{V_{write}}$	0.75
R_{int} [18]	8 Ω	Tolerable $\frac{V_{driver}}{V_{cell}}$	$\frac{4}{3}$

TABLE III
VARYING ARRAY SIZES TO SATISFY $V_{\text{cell}}/V_{\text{write}} = 0.75$

	R_{on}		
Array Size (N)	24 kΩ	36 kΩ	72 kΩ
$R_{int} = 2.5\ \Omega$ (22 nm)	1075	1448	2331
$R_{int} = 4\ \Omega$	746	1024	1695
$R_{int} = 8\ \Omega$ (14 nm)	420	591	1024

V. DESIGN OF A CROSSBAR ARRAY BASED ON THESE MODELS

The design of an example crossbar array using these models is demonstrated in this section. A resistive cell based on the RRAM described in [13] with a 14-nm metal1 half pitch is considered. Moreover, the $V/3$ biasing scheme and the floating biasing scheme are used, respectively, for the write and read operations. Based on these assumptions and decisions, the extracted device and interconnect parameters together with the assumed circuit parameters are listed in Table II. This analysis focuses on megabit capacity array sizes.

For the parameters listed in Table II, the maximum array size (N) is 420 (176.4 kb) and is limited due to the voltage degradation across the worst case selected cell during a write operation. Increasing the nonlinearity factor has a negligible effect. Two options, therefore, remain to mitigate this voltage degradation and enhance the device to provide a higher R_{ON} or place the crossbar array within the higher metal levels to decrease R_{int}. In Table III, the effect of different values of R_{int} and R_{ON} on the array size N is listed. From a driver area perspective, it is beneficial to increase R_{ON} rather than decrease R_{int}. While the output resistance of the driver should be 4 kΩ for $R_{\text{ON}} = 24$ kΩ, this resistance increases to 12 kΩ for $R_{\text{ON}} = 72$ kΩ. If R_{ON} and R_{int} cannot be changed, increasing the write voltage is preferable. This method can, however, consume significant power and limits the usage of more advanced technology nodes due to low breakdown voltages of sub-45-nm MOS transistors (below 1.1 V) [12]. To overcome low breakdown limitations of thin oxide MOS transistors, cascoded topologies as well as breakdown voltage multiplying circuits have been demonstrated [19]. These circuits, however, require increased driver area, exacerbating the area efficiency of a crossbar array.

VI. CONCLUSION

Design models for three important metrics in crossbar arrays are provided, such as the driver resistance, voltage across

the worst case cell (during both writes and reads), and read margin. These metrics provide intuition into the design of resistive crossbar arrays with unipolar or bipolar memory elements. The models exhibit good accuracy as compared with simulations and can be used to project the performance characteristics of large crossbar arrays. For nonlinearity factors greater than 10^4, the voltage degradation during a write and read operation can no longer be mitigated for, respectively, the $V/3$ biasing and floating biasing schemes. Thus, R_{ON} needs to be increased to prevent voltage degradation due to IR losses. For the read margin, under the grounded biasing scheme, sneak path leakage current is not the primary source of signal degradation but rather the interconnect resistance. For a read operation under the floating biasing scheme, the primary source of signal degradation is sneak path leakage current. Moreover, a write operation under the $V/3$ biasing scheme can be advantageous as compared with the $V/2$ biasing scheme if the cell selectors provide a significantly higher nonlinearity factor for a smaller voltage drop across the unselected cells. These models demonstrate that a higher R_{ON} can greatly benefit all three critical metrics that limit the size of crossbar arrays.

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