Stability of On-Chip Power Delivery Systems With Multiple Low-Dropout Regulators

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***Abstract*— Low-dropout (LDO) voltage regulators have become prominent elements of on-chip power delivery systems due to the increasing importance of separate voltage domains, fast dynamic voltage scaling, and the need for high-quality power. As the number of LDOs sharing a common power network increases, the stability of the power grid can degrade if the resonance frequency due to the off-chip parasitic impedances is not sufficiently separated from the unity gain frequency of the regulator. In this paper, this source of instability in power delivery networks, consisting of multiple LDO regulators with a balanced load, is described. The effect of the number of LDOs on the resonance frequency of the power delivery network is evaluated to determine the stability of the system when the LDOs operate under similar load conditions.**

***Index Terms*— Low dropout (LDO), on-chip voltage regulator, parasitic impedance, power delivery network, resonance, stability.**

I. Introduction

VOLTAGE regulators are fully integrated on-chip to enable granular power management without communicating off-chip and to reduce power consumption with fast dynamic voltage scaling [1]. In addition, a wide range of heterogeneous voltages can be generated on-chip without increasing the off-chip board area [2]. These benefits have led to many industrial products that incorporate different types of on-chip voltage regulators [3]–[6], containing as many as 64 regulators in a single power domain [3].

Fully integrated linear regulators as well as switching converters deliver on-chip power [4], [7]–[9]. While switching and switched capacitor regulators occupy significant space due to the bulky inductors and capacitors, capacitorless LDOs occupy the small area at the expense of lower power efficiency, thereby supporting the deployment of a larger number of on-chip regulators [10]. Due to the low integration overhead of linear regulators, capacitorless low-dropout (LDO) regulators are widely preferred over fully integrated switching converters [7], [9], [11].

A power delivery system that contains multiple on-chip LDO regulators can exhibit instability [12]–[16]. This phenomenon is a result of the interaction between the resonance of the off-chip parasitic network and the actively regulated on-chip power grid. One of the primary requirements of on-chip capacitorless LDOs is ensuring stability in the absence of a large output capacitor. Conventionally, satisfying stability requirements under light load conditions ($<$1 mA) is sufficient to ensure stability for a wide range of load variations [17], [18]. The general assumption is once the regulator is stable under light load conditions, the stability is guaranteed as long as the regulator operates above the minimum load condition for a range of output capacitance. Ensuring stability under light loads, however, does not guarantee stability when multiple LDO regulators operating under similar load conditions share the same power delivery network (as discussed in Section II). In this paper, this second source of instability is described. The effect of the resonance due to the parasitic impedances of the power delivery network is shown to depend on the number of voltage regulators, thereby affecting the stability of the system.

In Section II, instability due to the increasing number of LDOs is described. In Section III, a summary of the relevant literature is provided. In Section IV, the relationship between grid stability and the number of LDOs is explored. In Section V, the effect of certain circuit design parameters on the stability of the power grid is discussed. In Section VI, some conclusions are offered.

II. Stability of Parallel Connected LDOs

A conventional LDO architecture consisting of a single closed loop with an error amplifier and a pass transistor is considered here to simplify the stability analysis and produce an analytic relationship between the system stability and the number of LDOs, as shown in Fig. 1. The error amplifier is a two-stage operational transconductance amplifier with Miller compensation incorporating a nulling resistor [19]. These conventional LDOs are typically modified to support higher phase margin under light load conditions (1 mA) since a fully integrated regulator does not incorporate a large output capacitor, producing a nondominant output pole [20]. To separate the stability concerns under light load conditions

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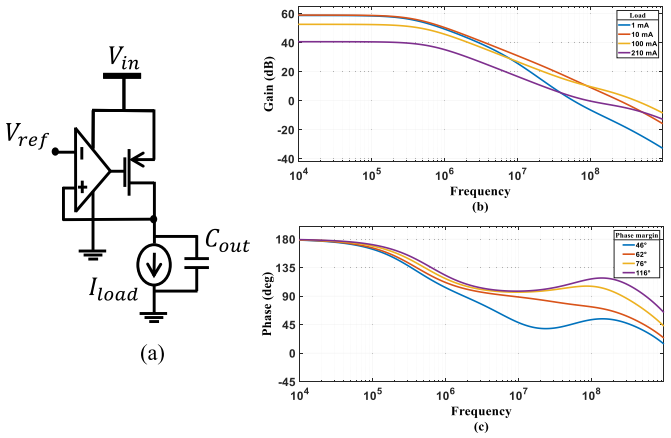

Fig. 1. Linear regulator used to analyze the stability of multiple connected LDOs. (a) Conventional LDO regulator. (b) Bode plot of a regulator under different load conditions.

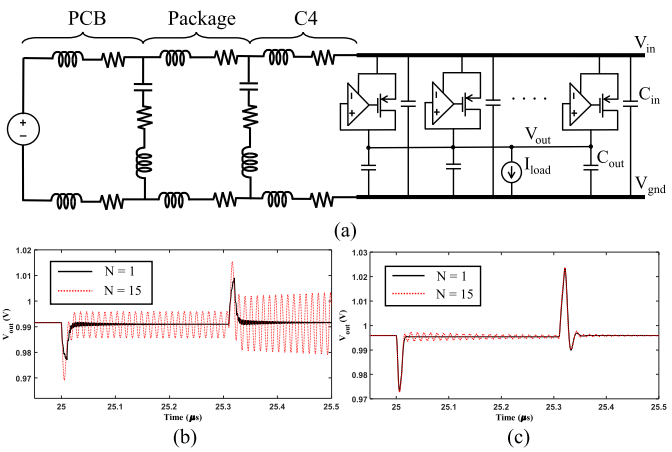

Fig. 2. Comparison of a single LDO to multiple connected LDOs sharing a common power grid. (a) Power delivery network with an input voltage of 1.2 V and an output voltage of 1 V. (b) Transient response to a load varying from 175 to 210 mA in 10 ns considering 1 and 15 LDOs. (c) Transient response to a load varying from 1 to 3 mA in 10 ns considering 1 and 15 LDOs. The parasitic impedances are listed in Table I in the Appendix. The input and output capacitances per LDO are, respectively, 1 nF and 50 pF. The load current as well as the input and output capacitors proportionally increase with the number of regulators. Each regulator therefore operates under the same load conditions and ac characteristics [see Fig. 1(b)].

from the stability concerns when considering multiple LDOs, a heavy load condition is assumed (on the order of a few hundred mA). The standalone regulator exhibits a highly stable system, as shown in Fig. 1(b). The phase margin is as low as 46° at 1 mA and as high as 116° at 210 mA considering a 50-pF output capacitance.

The LDO regulator produces a stable transient response to a step load variation from 175 to 210 mA when considered alone. The same regulator coexisting with 14 other LDOs sharing the same input grid, however, yields an unstable system, as shown in Fig. 2. Note that a single LDO, exhibiting a stable transient response, produces an oscillatory response when operating under the same conditions with a larger number of LDOs. This phenomenon is due to the additional LDOs, which exacerbate the interactions with the off-chip parasitic impedances. Specifically, the parasitic impedance at the input of each LDO changes with an increasing number of LDOs, shifting the resonant frequency, thereby increasing the phase shift of the regulator and producing an unstable power grid (see Section IV-A). Moreover, the power delivery system is stable under light load conditions and unstable under heavy load conditions despite lower phase margins under light load conditions [see Fig. 1(b)]. The phase margin of a standalone LDO without considering the power delivery network is therefore not an appropriate stability metric.

III. Existing Work

Most of the existing work on the stability of capacitorless on-chip LDOs consider a single-LDO system [17]. One exception is [15], where the effect of multiple on-chip LDOs on grid stability is reported. The inductive off-chip network used in the analog power delivery system produces an unstable grid when shared with 16 LDO regulators, each operating under a load of 20 mA. This paper, however, does not explain the reason for the degradation in stability with an increasing number of on-chip LDO regulators.

In [12], the stability of six distributed LDOs sharing a common grid is considered. A passivity-based stability criterion based upon the output impedance of the LDOs is proposed. This paper, however, assumes an ideal voltage supply at the input of the on-chip regulators, disregarding the parasitic effects of the off-chip power delivery network. The source of instability is described as due to the particular load conditions that the regulators are exposed to under unbalanced current sharing, causing the LDOs to exhibit low or negative phase margin. The source of grid instability with multiple on-chip regulators is, however, not due to unbalanced current sharing if the regulators exhibit positive phase margin across any load condition. Stable capacitorless on-chip LDOs have been reported under no-load conditions (0 A) [18] where most of the capacitorless LDOs exhibit increasing phase margin with increasing load. Since maintaining sufficient phase margin under any load condition is a primary design requirement, unbalanced current sharing in the presence of on-chip regulators cannot, by itself, cause grid instability, as long as the regulators retain a minimum phase margin under stringent load conditions.

The analyses proposed in [13] consider the parasitic network of the off-chip as well as the on-chip interconnects and provide a comprehensive discussion on the evaluation and optimization of grid stability with multiple digital LDO regulators. A complex power grid consisting of multiple digital LDOs is evaluated based on the signal flow graph of the entire system. The stability is evaluated based on a transfer function constructed from a signal flow graph of the grid system using Mason's gain formula. In [14], a stability checking methodology based on a hybrid stability constraint is provided, which considers a comprehensive power delivery network including parasitic impedances. A hybrid stability margin based on the hybrid passivity and finite gain stability theorem is established to evaluate the stability of a power grid. This stability constraint can be separately considered for each

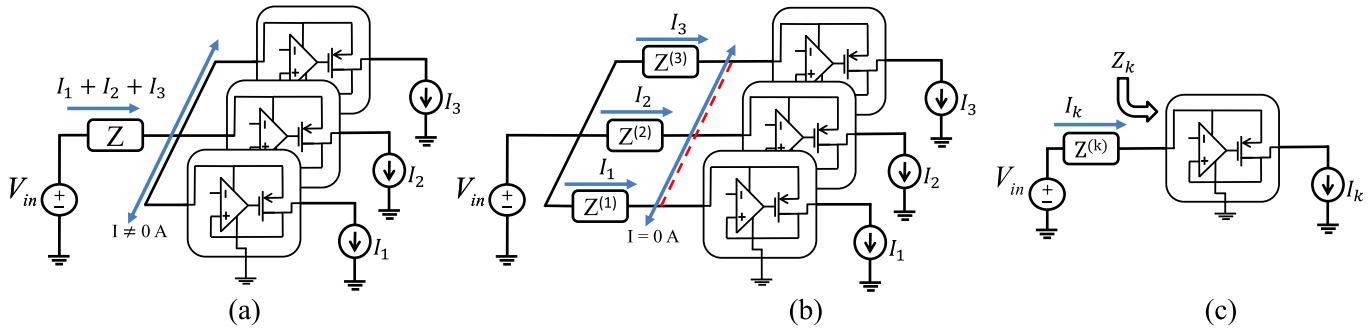

Fig. 3. Model of a power delivery system with parallel connected LDOs. The impedance of the power delivery network observed from the input of the LDOs is represented as a lumped impedance Z. (a) Multiple LDOs attached to the same power grid. (b) Grid impedance split per LDO. (c) Each LDO is separated based on the corresponding grid impedance at the input of the LDO.

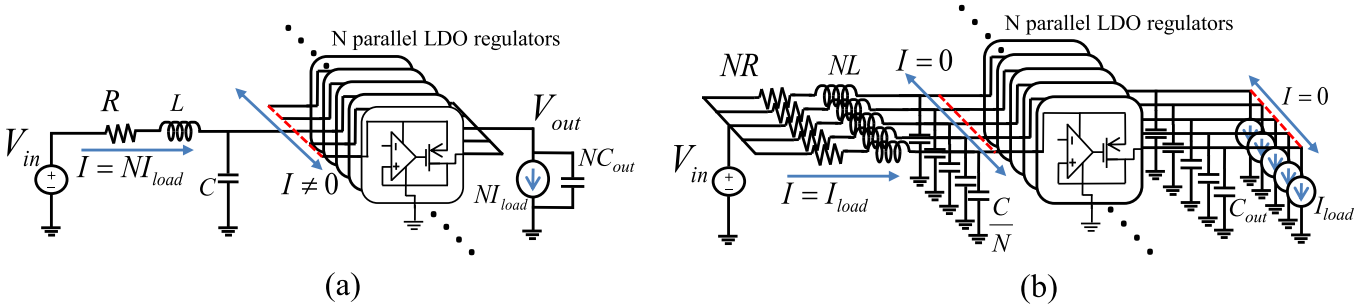

Fig. 4. Model of a power delivery system with parallel connected LDOs: (a) with an off-chip parasitic impedance and (b) distribution of the parasitic impedance when the LDOs operate under the same load conditions [22]. The quiescent current of the LDOs is assumed to be negligibly small.

LDO, enabling the LDOs to be individually tuned to enhance the stability of the grid. In [21], the hybrid stability constraint is considered to explore the relationship between different circuit-level parameters and the stability of the power grid. The effect of different LDO topologies, LDO parameters such as the unity gain frequency (UGF), and decoupling capacitors on grid stability is evaluated.

In this paper, the phenomenon of a decreasing resonant frequency due to an increasing number of LDOs is described using a different approach. By separating the individual LDOs sharing a common input grid while considering the impedance of the power delivery network, the open-loop characteristics are evaluated in terms of the number of LDOs. Furthermore, a passivity-based stability criterion similar to [12] is used to evaluate the relationship between the phase margin and the stability of a power grid. The degradation in the resonant frequency caused by the off-chip parasitic impedances is shown to be a critical factor affecting the stability of a grid with multiple LDOs operating under a balanced load condition.

IV. Evaluating the Stability of Multiple LDOs

To evaluate the stability of a power grid, the parasitic impedance of the power delivery network needs to be considered. To use the classical phase margin of an open-loop, single-input-single-output (SISO) system, the power delivery network is separated, as shown in Fig. 3. To detach an LDO from the grid while including the impedance of the power grid, the impedance of the power delivery network is split per each regulator. For example, considering the three LDOs shown in Fig. 3 with an input grid impedance Z, the impedances at the input of the LDOs are

$$Z^{(1)} = \frac{Z_1 Z}{Z_{123}},\quad Z^{(2)} = \frac{Z_2 Z}{Z_{123}},\quad Z^{(3)} = \frac{Z_3 Z}{Z_{123}} \tag{1}$$

$$Z_{123} = Z_1 || Z_2 || Z_3 \tag{2}$$

where $Z^{(k)}$ is the impedance of the power delivery network observed from the input of an LDO (k) and Z_k is the input impedance of an LDO (k). For N LDO regulators sharing a common input grid, the impedance at the input of an LDO is

$$Z^{(k)} = \frac{Z_k Z}{Z_{123\ldots N}} \tag{3}$$

$$Z_{123\ldots N} = Z_1 || Z_2 || \ldots || Z_N. \tag{4}$$

Note that the impedance at the input of each LDO depends upon the parasitic impedance of the power delivery network and the input impedance of each LDO. The open-loop response and the phase margin of the SISO LDO system considering the input impedance $Z_{(k)}$ produce useful insight into the relationship between the number of LDOs and the stability of the power grid. To intuitively relate the number of LDOs to the grid stability, multiple LDOs consisting of the same topology and bias conditions are considered. Note that under these conditions, the impedance at the input of each LDO simplifies to $N \times Z$, where N is the number of LDO regulators.

A. Effect of the Number of LDOs on Grid Stability

To evaluate the stability of a grid composed of multiple LDOs, the circuit shown in Fig. 4(a) is considered. The input

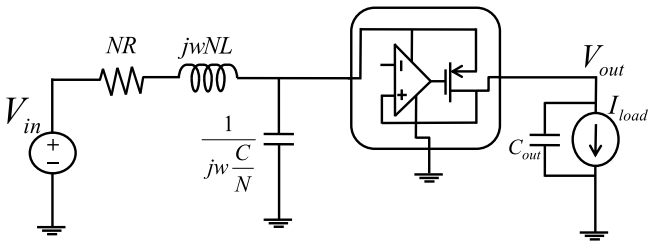

Fig. 5. Reduction of parallel connected LDOs operating under the same load conditions [22].

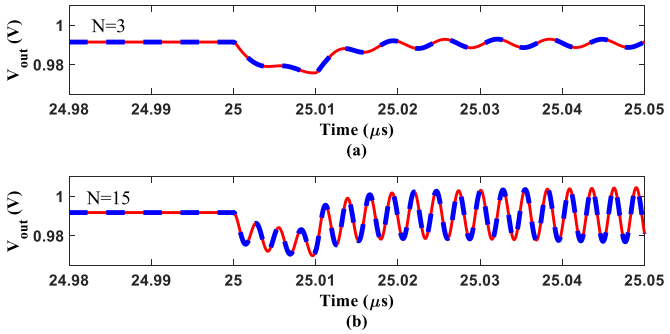

Fig. 6. Transient simulation of multiple connected LDO regulators, where the solid line describes the circuit shown in Fig. 4(a) and the dashed line describes the circuit shown in Fig. 5. (a) Three LDOs. (b) 15 LDOs.

to a number of parallel connected LDOs is loaded with an RLC network characterizing the parasitic impedances. A circuit composed of multiple LDOs sharing a common grid can be simplified under the condition that each regulator is symmetric and operates under balanced current sharing, as shown in Fig. 4(b). Under this condition, the parasitic impedance can be divided into N sections, where N is the number of LDO regulators, each conducting the same current. As a result, each section of impedance is directly connected to an LDO and detached from the rest of the circuit, leading to the circuit shown in Fig. 5. Note that this circuit produces an identical response to load variations if the system with multiple LDOs remains balanced, regardless of whether the output load is shared or located across separated grids, as shown in Fig. 6.

The instability due to the increasing number of LDOs can therefore be evaluated by this simplified single-loop system consisting of a single LDO using phase margin as a metric. Note that although this condition reflects a constrained case for regulators in different blocks, the condition of balanced loads is more common in shared output grids. In the remainder of this section, this system is used to provide intuition behind the degradation in the stability of a multi-LDO system, providing insight into the relationship between the grid stability and the number of LDO regulators.

B. Source of Instability

The stability of a system depends upon the open-loop gain and phase of that system. The system becomes unstable if the open-loop gain is greater than unity when the phase shift is greater than 180°. To evaluate the stability, a small-signal model of the simplified circuit shown in Fig. 7 is used.

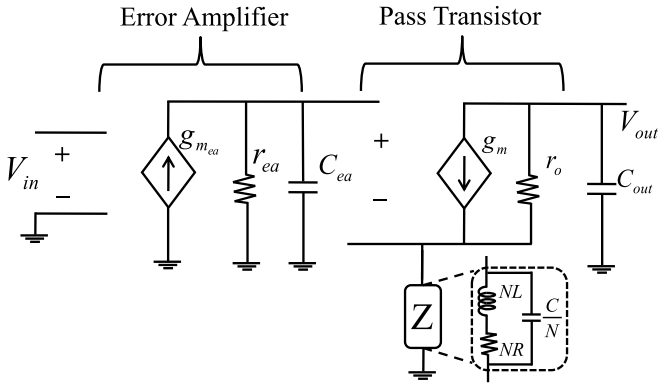

Fig. 7. Small-signal model of the simplified circuit shown in Fig. 5 [22].

The LDO is modeled as a two-pole system [23]. The dominant pole is generated by the error amplifier, whereas the second pole is due to the output capacitor C_{out} of the LDO regulator. The open-loop gain of the LDO regulator is

$$H(s) = \frac{V_{\text{out}}}{V_{\text{in}}}(s) = \frac{-A_{\text{ol}}}{(1+\text{sC}_{\text{ea}}r_{\text{ea}})(1+sC_{\text{out}}(r_o+g_m r_o Z+Z))} \tag{5}$$

$$A_{\text{ol}} = g_m r_o A_{\text{ea}} \tag{6}$$

$$A_{\text{ea}} = g_{m_{\text{ea}}} r_{\text{ea}} \tag{7}$$

$$Z = \frac{\text{NR}+\text{sNL}}{1+\text{sRC}+s^2\text{LC}} \tag{8}$$

where R, L, and C are, respectively, the parasitic resistance, inductance, and capacitance at the input, and A_{ol} and A_{ea} are, respectively, the open-loop gain of the LDO regulator and the error amplifier over the midband frequency range. The parasitic impedance at the input of the LDO regulator adds two additional poles and zeros, producing a biquad characteristic. The open-loop transfer function can be rewritten as

$$H(s) = \frac{V_{\text{out}}}{V_{\text{in}}}(s) \approx \frac{-A_{\text{ol}}(1+\text{sRC}+s^2LC)}{(1+sC_{\text{ea}}r_{\text{ea}})(1+sC_{\text{out}}r_o)\left(1+\frac{s}{w_o Q}+\frac{s^2}{w_o^2}\right)} \tag{9}$$

$$w_o \approx \frac{1}{\sqrt{L(C+\text{NC}_{\text{out}})}} \tag{10}$$

$$Q \approx \frac{\sqrt{L(C+\text{NC}_{\text{out}})}}{\text{RC}+C_{\text{out}}(\text{NR}+r_o)} \tag{11}$$

where w_o and Q are, respectively, the resonant angular frequency and the quality factor of the complex poles, produced by the interaction between the LC impedances and the LDO.

The complex poles due to the RLC impedances produce a resonant spike in the open-loop characteristic of the regulator, as shown in Fig. 8. Note that the resonant peak changes with the number of LDOs. As the number of regulators that share a common input grows from one to ten, the gain at the resonant frequency increases beyond 0 dB above the initial UGF, thus resulting in multiple zero crossings. The significant reduction in phase at the resonant frequency therefore produces an unstable system when the number of LDOs is sufficiently high

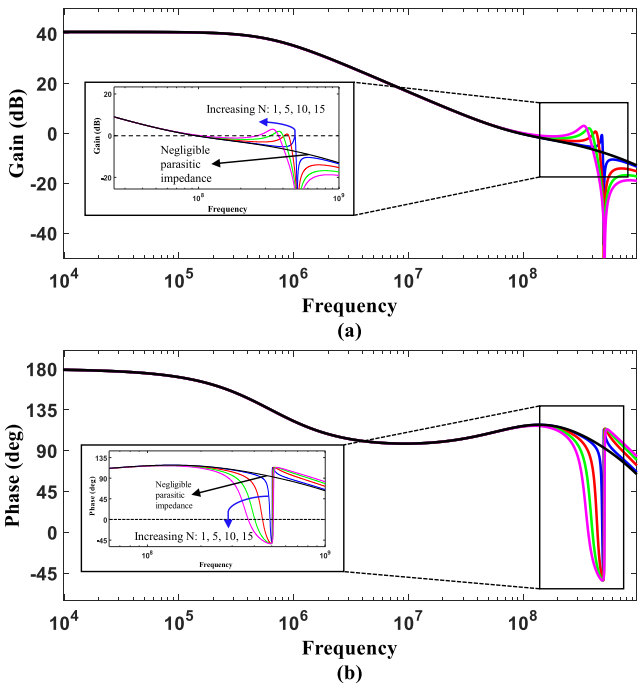

Fig. 8. Bode plot of a circuit model shown in Fig. 5. The effect of an increasing number of parallel LDOs: (a) open-loop gain and (b) phase. With five parallel LDOs, the open-loop gain rises above 0 dB beyond the initial UGF, producing an unstable system. $C = 1$ nF, $L = 100$ pH, $R = 100$ $\mu\Omega$, $C_{\text{out}} = 50$ pF, and $I_{\text{load}} = 210$ mA per LDO.

to shift the resonant frequency close to the UGF of the LDO. If the resonant frequency is not sufficiently separated from the UGF, the stability of the system will degrade even under heavy load conditions (>1 mA) This behavior is noted when the LDOs operate under similar load conditions.

Note that this effect resembles the resonant behavior stemming from the high quality factor under light load conditions [17]. Depending upon the circuit architecture, the LDO can exhibit complex poles under light load conditions (<1 mA), potentially producing a high quality factor (>0.707), degrading the stability. Since a heavy load is assumed, the biquad characteristic is due to the parasitic impedance at the input of the LDO (210 mA). Under this condition, the LDO exhibits single-pole behavior below the UGF when the input parasitic impedance is neglected (see Fig. 8). The resonant behavior is therefore due to the RLC impedance of the power grid.

C. Degradation of Resonant Frequency

The resonant frequency and quality factor of parasitic impedance are, respectively,

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{\text{LC}}} \tag{12}$$

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}}. \tag{13}$$

These standard parameters characterizing a power grid remain constant irrespective of the number of LDOs. When the parasitic impedance of the power grid is combined with the LDO regulators, however, the resonant frequency as well as the quality factor changes with respect to the number of LDOs. The spike in the resonant frequency shifts to a lower frequency when the number of LDOs increases, degrading the grid stability.

The variation in the resonant frequency is due to the output capacitance of the LDOs that interacts with the input power grid.[1] Note that if the output capacitance is negligible, the transfer function does not exhibit any complex poles (thus, no resonant peak), as described in (9) and (11). To understand the interaction of the output capacitance with the input power grid, the input impedance of the small-signal model (see Fig. 7), described in (14)[2] shown at the bottom of this page, is considered. The magnitude of the input impedance $|Z_{\text{in}}|$ is shown in Fig. 9(c). Note that the input impedance simplifies to $(1/sC_{\text{out}}) + (r_o||(1/g_m))$ under high frequencies (above the corner frequency of $|Z_{\text{in}}|$). The LDO shown in Fig. 9(a) can be represented as an RC circuit from the input port, as shown in Fig. 9(b). Under heavy load conditions, since the pass gate enters the linear region, the input resistance of the pass transistor (from the source terminal, $r_o||(1/g_m)$) significantly decreases. As a result, the input of the LDO is exposed to the output capacitance. The capacitance at the input of the grid therefore increases with additional LDOs (due to the increased output capacitance), shifting the resonant frequency when the corner frequency of $|Z_{\text{in}}|$ is below the resonant frequency (12).

The effective resonant frequency based on the small-signal model described by (9) is approximately

$$f_{\text{res\_eff}} \approx \frac{1}{2\pi\sqrt{L(C + NC_{\text{out}})}}. \tag{15}$$

This expression is consistent with the remarks describing the interactions between the input and output capacitance of the LDO under balanced load conditions. When the input power grid is exposed to the output capacitors, the input capacitance with N LDOs increases from C to approximately $C + NC_{\text{out}}$, leading to the new resonant frequency described in (15). The relationship between the number of on-chip LDOs and the

[1]The on-chip power delivery network consists of the input and output power grids. The input power grid connecting the off-chip power network to the inputs of the LDOs is shared among all the regulators. The output power grid delivers the output voltage from the individual regulators to the distributed loads across the integrated circuit.

[2]A parallel resistor R_{ea} is considered to account for the additional path to ground through the error amplifier.

$$Z_{\text{in}}(s) = \frac{(1+g_m r_o g_{m_{\text{ea}}} r_{\text{ea}}) + s(r_{\text{ea}}C_{\text{ea}} + r_o C_{\text{out}}) + s^2(r_{\text{ea}}C_{\text{ea}} r_o C_{\text{out}})}{\left(\frac{1}{R_{\text{ea}}} + \frac{1}{R_{\text{ea}}} g_m r_o g_{m_{\text{ea}}} r_{\text{ea}}\right) + s\left(\frac{1}{R_{\text{ea}}} r_{\text{ea}}C_{\text{ea}} + \frac{1}{R_{\text{ea}}} r_o C_{\text{out}} + C_{\text{out}} + C_{\text{out}} g_m r_o\right) + s^2\left(\frac{1}{R_{\text{ea}}} r_{\text{ea}}C_{\text{ea}} r_o C_{\text{out}} + r_{\text{ea}}C_{\text{ea}}C_{\text{out}} + r_{\text{ea}}C_{\text{ea}}C_{\text{out}} g_m r_o\right)} \tag{14}$$

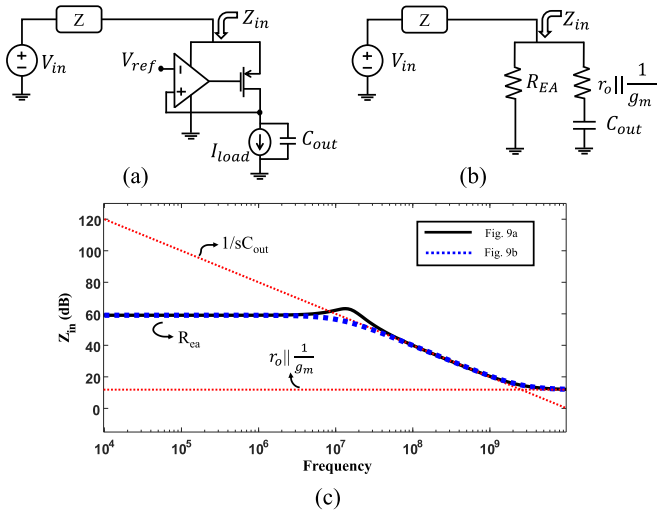

Fig. 9. Input impedance: (a) considering the LDO regulator, (b) model of the input impedance as an RC circuit, and (c) comparison of the magnitude of the input impedances.

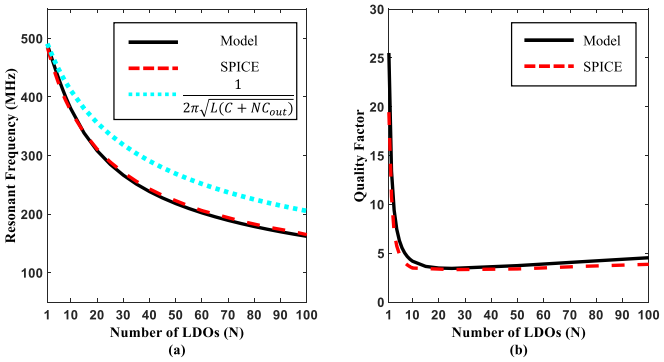

Fig. 10. Effect of the different number of LDO regulators: (a) resonant frequency and (b) quality factor based on the circuit characteristics considered in Fig. 8. The model is based on the small-signal circuit shown in Fig. 7.

resonant frequency and quality factor [based on (9) and (15)] is shown in Fig. 10.

Note that increasing the number of LDOs from one to ten lowers the resonant frequency by roughly 100 MHz when considering an input capacitance of 1 nF and an output capacitance of 50 pF (per LDO).

The degradation in resonant frequency causes instability, particularly in wide bandwidth LDOs [18], [24] where the closed-loop UGF of the circuit is on the order of tens to hundreds of MHz (see [18], [25]–[29]). Low-bandwidth LDOs are therefore resilient to instability caused by an increasing number of LDOs. LDOs with high UGF are used in applications such as microprocessors where fast response times are necessary [18] or analog circuits requiring high-power supply rejection across a wide range of frequencies [28], [29]. In these applications, careful design of the power network is necessary to ensure sufficient separation between the LDO UGF and the resonant frequency of the network.

D. Condition for Stability

The traditionally assumed worst case stability condition of an LDO under light load conditions changes when the input of an LDO is coupled to an LC network. The complex poles due to the input impedances increase the phase shift by 180°, significantly lowering the phase margin if the resonant frequency is close to the UGF.

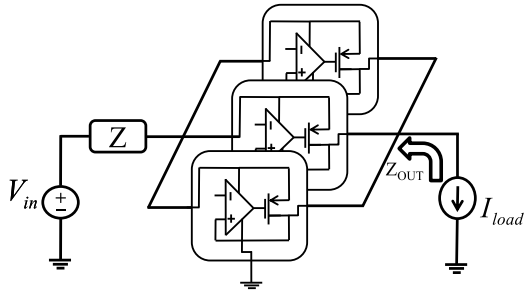

Fig. 11. Output impedance of multiple LDOs sharing a common load.

If the resonant frequency is close to the UGF, the open-loop characteristics of the LDO produce a nonmonotonic response (see Fig. 8). At the resonant frequency, the gain increases while lowering the phase below 0°. As a result, multiple zero crossings are observed. With the nonmonotonic behavior of the loop gain, a positive phase margin at the initial UGF does not guarantee system stability. To ensure stability, sufficient phase margin is required at the last 0-dB crossing of the Bode diagram. Equivalently, the following condition must be satisfied:

$$\angle H(\max\{f_{0\,\mathrm{dB}}\}) > 0 \tag{16}$$

where $H(f)$ is the open-loop transfer function of the LDO and $\max\{f_{0\,\mathrm{dB}}\}$ is the highest UGF (i.e., last 0-dB crossing).

If the phase margin is nonpositive, the power grid is unstable. This conclusion is based on the passivity-based stability criterion in [12], considering the following two observations proved in [30] and [31].

1) An linear time-invariant system, when coupled to a passive system, is stable if and only if the driving point impedance is passive [30].
2) An impedance $Z(s)$ cannot be passive if $Z(s)$ exhibits imaginary or right half-plane (RHP) poles [31].

Note that the second condition also implies the bounded-input-bounded-output (BIBO) stability, i.e., a passive impedance $Z(s)$ is bounded for all bounded inputs [31]. Hence, the output impedance Z_{out} of N parallel LDOs, as shown in Fig. 11, needs to satisfy the BIBO stability, exhibiting no RHP poles.

The output impedance $Z_{\mathrm{out}}(s)$ of N LDOs sharing a common output under balanced loads is

$$Z_{\mathrm{out}}(s) = \frac{\left(\frac{1}{N}\right)(r_o + Zg_m r_o + Z)(1 + sr_{\mathrm{ea}}C_{\mathrm{ea}})}{A_{\mathrm{ol}} + (1 + sr_{\mathrm{ea}}C_{\mathrm{ea}})(1 + sC_{\mathrm{out}}(r_o + Zg_m r_o + Z))}. \tag{17}$$

To relate the open-loop phase margin to the passivity constraints, Z_{out} is rewritten as

$$Z_{\mathrm{out}}(s) = Z'_{\mathrm{out}}(s)\frac{1}{|H(s)|e^{j(\pi+\theta(s))} + 1} \tag{18}$$

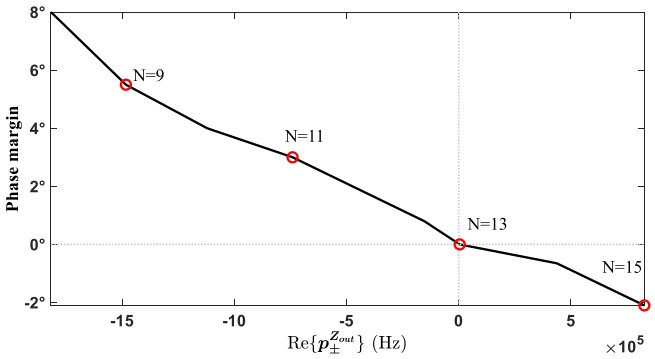

Fig. 12. Decreasing the phase margin shifts the complex poles of the output impedance $p_{\pm}^{Z_{\text{out}}}$ to the RHP.

where $\theta(s)$ is the phase of the open-loop transfer function ($\angle H(s)$), and $Z'_{\text{out}}(s)$ is

$$Z'_{\text{out}}(s) = \frac{\left(\frac{1}{N}\right)(r_o + Zg_m r_o + Z)}{(1 + sC_{\text{out}}(r_o + Zg_m r_o + Z))}. \tag{19}$$

Evaluating (18) at the UGF yields

$$Z_{\text{out}}(\text{jw}_{\text{UGF}}) = Z'_{\text{out}}(\text{jw}_{\text{UGF}}) \frac{1}{1 \cdot e^{j(\pi + PM)} + 1} \tag{20}$$

where the phase margin PM is

$$\text{PM} = 180^\circ - \Delta\theta(\text{jw}_{\text{UGF}}). \tag{21}$$

Note that when the phase margin decreases to 0, the output impedance diverges to infinity, violating the passivity criterion and producing an unstable power grid. The effect of a decreasing phase margin on the complex poles of the output impedance is shown in Fig. 12.

When the phase margin is nonpositive, the complex poles exhibit nonnegative real parts, producing an unstable power grid. A positive phase margin of an open-loop LDO when considering the input impedance is therefore a necessary condition to ensure a stable power delivery network.

Under unbalanced load conditions, the output impedance and open-loop characteristics cannot be described in terms of N since the internal parameters (g_m, r_o, and A_{ol}) of the LDOs differ, affecting the impedance $Z^{(k)}$ at the input of each LDO. This impedance would need to be determined for each LDO using (3) to characterize the LDO output impedance and the open-loop transfer characteristics.

V. Effect of Design Parameters on Grid Stability

In this section, the relationship between the circuit-level parameters and the stability of the power delivery network is explored. In Section V-A, the LDO design parameters, such as the UGF, output capacitance, and input impedance, and in Section V-B, the power grid design parameters, such as the input parasitic impedances, are considered.

A. LDO Design Parameters

The effect of several LDO design parameters on the stability of a power grid is explored. The output capacitance, UGF, and input impedance of the LDO are considered, respectively, in Sections V-A1–V-A3.

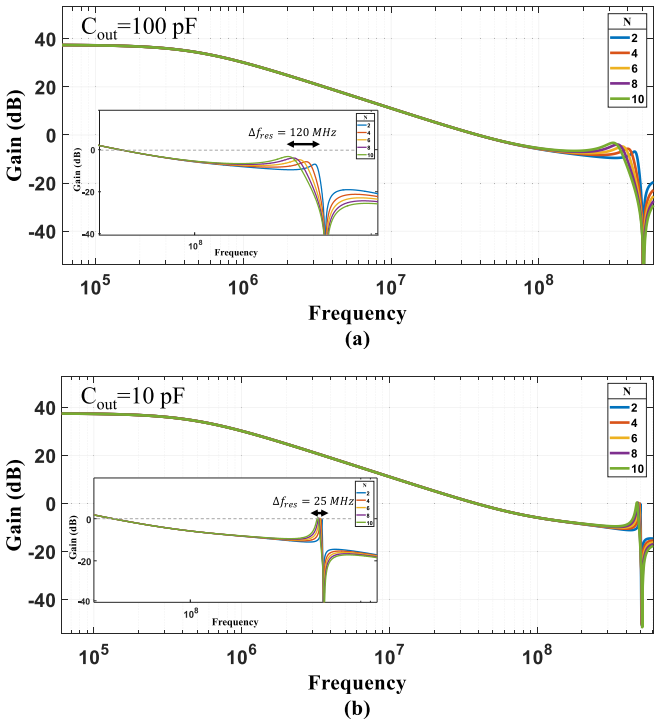

Fig. 13. Open-loop transfer characteristics of an LDO assuming the simulation setup shown in Fig. 8. (a) Large output capacitance. (b) Small output capacitance.

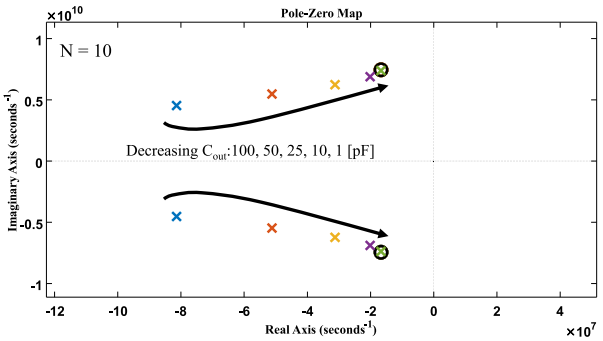

Fig. 14. Complex poles of the open-loop transfer function $H(s)$ become equal to the complex zeros with decreasing output capacitance.

1) Output Capacitance: The effective resonant frequency is influenced by the output capacitance C_{out}, as described in (15). A small output capacitance reduces the variations in the resonant frequency, while a large output capacitance increases the variations with respect to the number of LDOs, as shown in Fig. 13. Variations in the resonant frequency become negligible when $C \gg NC_{\text{out}}$. While a smaller output capacitance may be desired for this reason, decreasing the output capacitance C_{out} can increase the quality factor, exacerbating the peak resonant frequency. This effect is due to the complex poles of the open-loop circuit [see (9)] merging with the complex zeros with decreasing C_{out}, as shown in Fig. 14.

Note that if the output capacitance is zero, the complex poles and zeros are equal, thereby canceling [see (11)]. For zero output capacitance, the input impedance has therefore no effect on the open-loop transfer characteristics, as noted in (9).

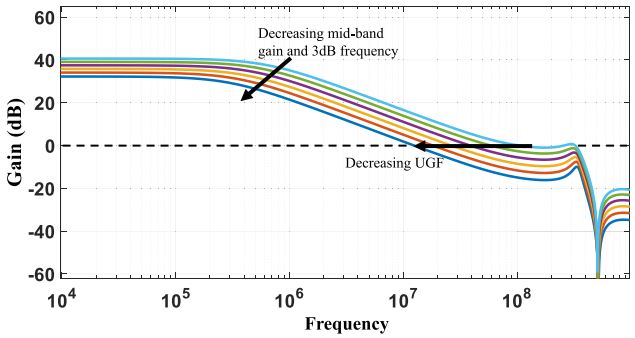

Fig. 15. Reduction in the open-loop gain of an LDO significantly lowers the UGF. Decreasing the midband gain from 40 to 32 dB reduces the UGF (considering the first 0-dB crossing) from 100 to 12 MHz.

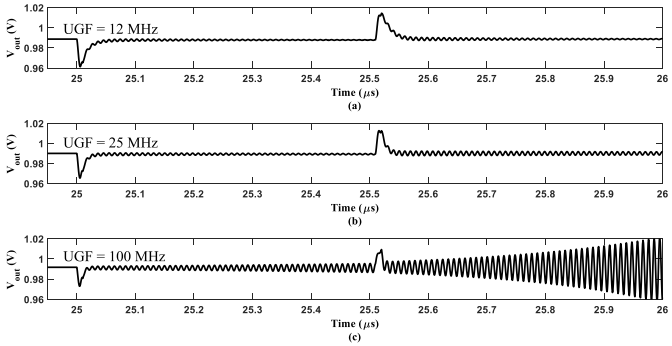

Fig. 16. Effect of the UGF on the output power grid shared by ten LDOs. (a) UGF at 12 MHz. (b) UGF at 25 MHz. (c) UGF at 100 MHz. An output capacitance of 100 pF and an input capacitance of 1 nF per LDO are considered with the off-chip power grid described in the Appendix. A total load variation from 1.75 to 2.1 A is assumed (equally divided among the LDOs).

Under this ideal condition, the stability of the power grid does not decrease with an increasing number of LDOs. Since some output capacitance is always present, however, to either reduce the voltage droop or due to the parasitic capacitance of the load, the resonance effect needs to be considered.

2) Unity Gain Frequency: Sufficient separation between the UGF and the resonant frequency is necessary to ensure a stable power delivery network. Under a fixed resonant frequency, the LDOs can be designed for a lower UGF to increase this separation. For instance, the gain or 3-dB frequency can be decreased to reduce the UGF, as shown in Fig. 15. Note that a sufficient reduction in gain lowers the resonant spike below 0 dB at a cost of lower load regulation. Furthermore, the lower the UGF, the slower the response time of the LDO, thereby increasing the voltage droop. A tradeoff therefore exists between the power grid stability and the power noise due to voltage droops.

The effect of a decreasing UGF on the voltage of the power delivery network is shown in Fig. 16. Note that as the UGF decreases, the output response of the regulators becomes more stable. This effect is due to improved phase margins, as the peak resonant frequency falls below the unity gain of the regulator, farther from the UGF.

3) Input Impedance: The resonant frequency of the input power grid changes with respect to the number of LDOs

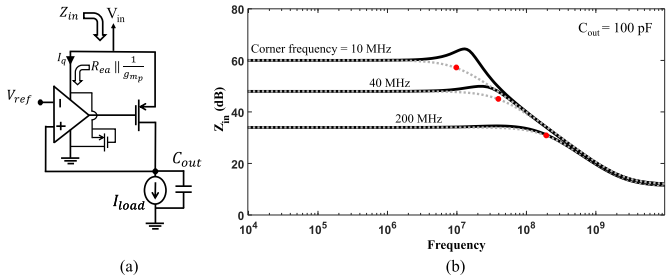

Fig. 17. Increasing the corner frequency of $|Z_{\text{in}}|$ reduces the interaction between the input and output power grids over a wider range of frequencies. (a) LDO with an additional pull-up transistor to reduce the resistance of the error amplifier R_{ea} observed from the input power network. (b) Different corner frequencies of $|Z_{\text{in}}|$ under a fixed output capacitance by increasing the quiescent current I_q of the LDO.

due to the interactions between the input power grid and the output capacitors of the LDOs, as described in Section IV-C. The input impedance of an LDO Z_{in} is equal to the output capacitance above the corner frequency of $|Z_{\text{in}}|$ under heavy load conditions, thus increasing the total capacitance on the input power grid (from C to $C + NC_{\text{out}}$) and decreasing the resonant frequency with an increasing number of LDOs. To prevent the degradation of the resonant frequency with additional LDOs, the corner frequency of $|Z_{\text{in}}|$ is increased, as shown in Fig. 17. The corner frequency is

$$f_{\text{corner}} \approx \frac{1}{2\pi R_{\text{ea}} C_{\text{out}}} \tag{22}$$

where R_{ea} is the resistance of the path to ground through the error amplifier (see Fig. 9). Note that R_{ea} (and therefore, the corner frequency of Z_{in}) depends upon the topology and quiescent current of the error amplifier. To evaluate the relationship between the corner frequency of $|Z_{\text{in}}|$ and the stability of the power grid, a pull-up transistor is placed in parallel to the error amplifier, as shown in Fig. 17(a). For a fixed output capacitance, R_{ea} is decreased to increase the corner frequency. The size of the pull-up transistor is increased to reduce R_{ea} at a cost of higher quiescent current I_q.

The additional path to ground supplied by the error amplifier limits the frequency range where the input impedance of the LDO is equivalent to the impedance of the output capacitance, preventing the input power grid to be loaded by the output capacitor of the LDOs. Therefore, increasing the corner frequency f_{corner} mitigates the stability of the power grid, as shown in Fig. 18. The stability of the power grid improves as the corner frequency increases from 20 to 60 MHz at a cost of higher I_q. A tradeoff therefore exists between the current efficiency and the stability of the power delivery network.

B. Power Grid Parameters

A power delivery network can support a more stable multi-LDO system by exploiting the strong dependence between the grid stability and the parasitic impedance of the power delivery network. A complex power delivery network typically consists of the parasitic board and package impedances as well as the impedance of the controlled collapse chip connections (C4s), as shown in Fig. 22. While the

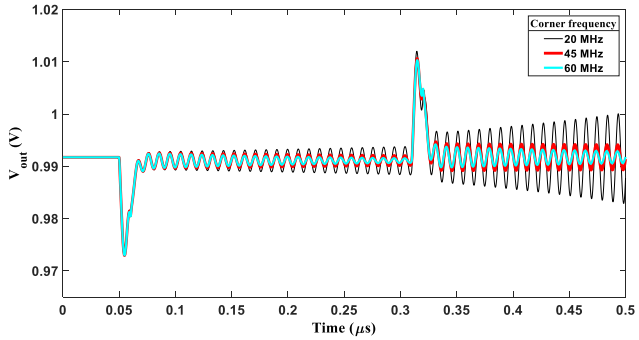

Fig. 18. Increasing the corner frequency of Z_{in} reduces the interaction of the output capacitance with the input power grid, improving the stability of the power delivery network. The same power delivery network described in Fig. 15 is assumed with a UGF of 100 MHz.

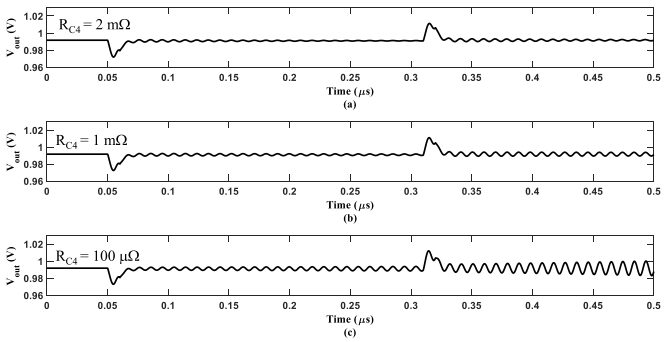

Fig. 19. C4 parasitic resistance R_{C4} is increased to reduce the quality factor and improve the stability of the power grid. Transient response of the output grid considering (a) $R_{C4} = 2$ mΩ, (b) $R_{C4} = 1$ mΩ, and (c) $R_{C4} = 0.1$ mΩ. The power delivery network and the parasitic impedances are listed in the Appendix with a load variation of 1.75 to 2.1 A, evenly distributed among the ten LDOs. The resonant frequency is 112 MHz.

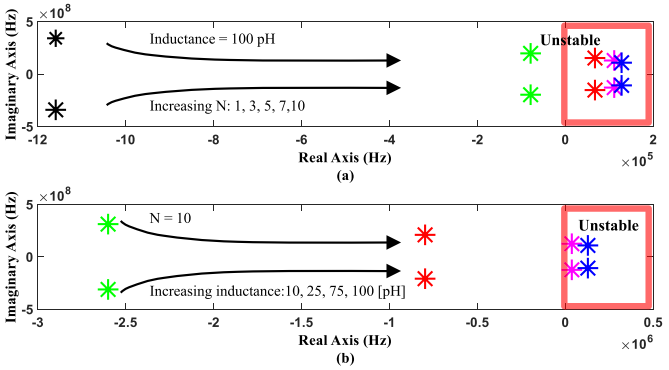

Fig. 20. Pole movement of the output impedance at the driving point (a) considering single and multiple LDOs and (b) several C4 parasitic inductances.

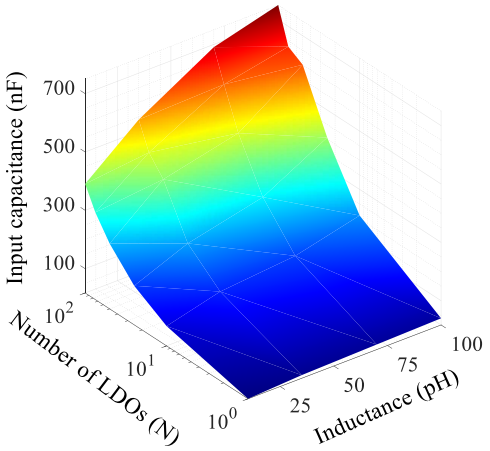

Fig. 21. Effect of inductance and the number of LDOs on the input capacitance required to prevent a phase shift of more than 45° at the resonant frequency (considering the circuit characteristics used in Fig. 5).

package and board impedances have a small effect on the system stability due to the large off-chip capacitors (typically tens to hundreds of microfarads), the resonance produced by the C4 inductance and the on-chip capacitance is often significant [32]–[34]. This resonance, typically a few hundred megahertz, exhibits a higher quality factor due to the small on-chip capacitance (from tens to hundreds of nanofarads). In this section, the power delivery network described in the Appendix is considered. The number of LDOs N is ten, and the UGF is 100 MHz [see Fig. 1(b), assuming a load condition of 210 mA]. The input capacitance is 1 nF per LDO. The resonant frequency due to the C4s is 112 MHz.

To improve the stability of the power grid, either the quality factor is reduced to increase the system damping or the resonant frequency is increased to further separate the UGF of the LDOs. One approach to increase the damping is using a more resistive power delivery network. Resistive power grids are more stable at a cost of greater power noise, as shown in Fig. 19.

Note that increasing the C4 parasitic resistance by an order of magnitude stabilizes the power grid. This effect is due to the quality factor Q that is inversely proportional to the resistance, as described in (11). This approach is suitable in those systems with low-current demand (e.g., 1 to 2 A) where the IR drop is negligible.

Alternatively, reducing the C4 parasitic inductance L_{C4} improves the grid stability. The benefits of decreasing L_{C4} are twofold. A lower parasitic inductance increases the resonant frequency, thereby increasing the separation with the UGF. Moreover, the lower the inductance, the smaller the quality factor. Power delivery networks that are less inductive can therefore support a greater number of LDOs, as shown in Fig. 20.

For a parasitic inductance of 100 pH, five LDOs sharing the same power grid are sufficient to produce RHP poles and destabilize the power grid. Moreover, to support ten LDOs, this parasitic inductance needs to be reduced to a few tens of pH or less. The LDOs operating with a UGF of 100 MHz are exposed to a resonant frequency of approximately 110 MHz when $L_{C4} = 100$ pH and $N = 10$. Reducing the inductance to 10 pH increases the resonant frequency to 350 MHz, improving the stability of the power delivery network.

Finally, adding on-chip capacitance to the input power grid reduces the quality factor. Due to the weak relationship between the quality factor and the input capacitance ($Q \propto 1/\sqrt{C}$), a large input capacitance is needed to increase the

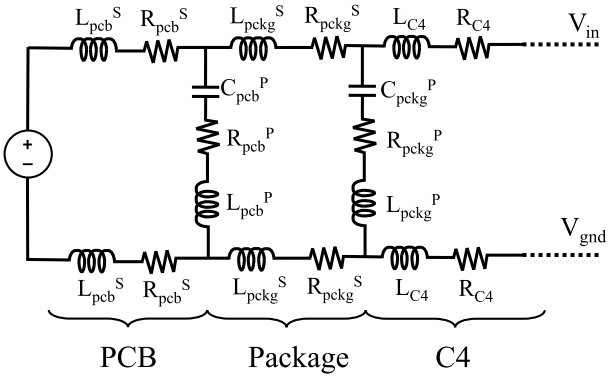

Fig. 22. Off-chip power delivery network model considered in Sections II and V [33].

TABLE I
OFF-CHIP PARASITIC IMPEDANCES

Parameters	Value	Parameters	Value
${L_{pcb}}^S$	21 pH	${C_{pcb}}^P$	240 μF
${R_{pcb}}^S$	94 $\mu\Omega$	${R_{pcb}}^P$	165.4 $\mu\Omega$
${L_{pckg}}^S$	120 pH	${L_{pcb}}^P$	33.92 nH
${R_{pckg}}^S$	1.1 mΩ	${C_{pckg}}^P$	26.4 μF
L_{C4}	100 pH	${R_{pckg}}^P$	541.5 $\mu\Omega$
R_{C4}	100 $\mu\Omega$	${L_{pckg}}^P$	4.61 μH

damping characteristics. Note that increasing the capacitance decreases the resonant frequency. The input capacitance therefore needs to be sufficiently high to not exacerbate the grid stability. Specifically, if $C \gg NC_{\text{out}}$, the complex poles and zeros are approximately similar, reducing the phase roll-off at the resonant frequency. The required input capacitance in terms of the number of LDOs and input parasitic inductance is shown in Fig. 21. Note that the required capacitance at the input of the regulators reaches a few tens of nanofarads per LDO when the number of regulators is more than ten. Reducing the parasitic inductance significantly lowers the required input capacitance since the difference between the complex poles and zeros decreases with a smaller inductance. The overhead of a large input capacitance can therefore be mitigated by reducing the parasitic inductance.

VI. CONCLUSION

The stability of a power delivery system composed of multiple on-chip LDO regulators is explored under balanced load conditions. Ensuring stability under light load conditions is insufficient to guarantee the stability of a power delivery system shared by multiple LDO regulators. The stability of a power network is shown to degrade as the number of regulators operating under similar loads increases due to the resonance generated by the RLC parasitic impedances. With a greater number of LDOs, the resonant frequency decreases, degrading the stability of the power grid when the unity gain of the regulator and the resonant frequency of the input grid are insufficiently apart. Ensuring sufficient separation between the UGF and the resonant frequency is critical to maintain a stable power grid when supporting a large number of on-chip LDOs.

APPENDIX

The off-chip power delivery network considered in Sections II and V is shown in Fig. 22. The value of the individual impedances is listed in Table I. The value of the board and package impedances is from [33]. The lumped parasitic inductance and resistance connecting the package to the integrated circuit (e.g., using C4s) are assumed to be, respectively, 100 pH and 100 $\mu\Omega$.

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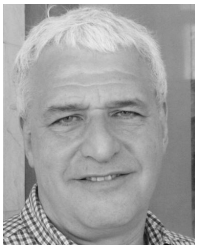

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