Design Methodology for Distributed Large-Scale ERSFQ Bias Networks

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***Abstract*— Rapid single-flux quantum (RSFQ) circuits have recently attracted considerable attention as a promising cryogenic beyond CMOS technology for exascale computing. Energy-efficient RSFQ (ERSFQ) is an energy-efficient, inductive bias scheme for RSFQ circuits, where the power dissipation is drastically lowered by eliminating the bias resistors, while the cell library remains unchanged. An ERSFQ bias scheme requires the introduction of multiple circuit elements—current limiting Josephson junctions, bias inductors, and feeding Josephson transmission lines (FJTLs). In this article, parameter guidelines and design techniques for ERSFQ circuits are presented. The proposed guidelines enable more robust circuits resistant to severe variations in supplied bias currents. Trends are considered, and advantageous tradeoffs are discussed for the different components within a bias network. The guidelines provide a means to decrease the size of an FJTL and, thereby, reduce the physical area, power dissipation, and overall bias currents, supporting further increases in circuit complexity. A distributed approach to ERSFQ FJTL is also presented to simplify placement and minimize the effects of the parasitic inductance of the bias lines. This methodology and related circuit techniques are applicable to automating the synthesis of bias networks to enable large-scale ERSFQ circuits.**

***Index Terms*— Single-flux quantum (SFQ), superconductive digital electronics, superconductive integrated circuits.**

I. Introduction

With the slower scaling of conventional CMOS circuits, considerable research efforts have been expended to determine a suitable technology replacement or supplement for a variety of compute-intensive applications [1]. For high-performance supercomputers, cloud computing, and quantum computation, superconductive electronics (SCE) is a promising beyond CMOS technology [2]. Although cryogenic refrigeration is necessary to operate these circuits, the energy per bit for SCE-based supercomputers, including the refrigeration expenses, is one to three orders of magnitude smaller than typical CMOS levels [3].

Multiple SCE logic families exist with a different organization of basic gates, bias networks, and signaling methodologies. The focus of this article is on the original and most mature of these families, rapid single-flux quantum (RSFQ) [4], and, in particular, a recently introduced energy-efficient version, energy-efficient RSFQ (ERSFQ) [5].

A major obstacle to improving the large-scale integration of RSFQ circuits is the lack of electronic design automation (EDA) tools [6]. Current research is aimed at adapting existing CMOS-based industrial tools [7] while developing novel algorithms and circuit techniques specifically targeted for SFQ technology [8]. RSFQ gates are current biased and, unlike CMOS, require a precise bias current to maintain correct functionality. Both overbiased and underbiased gates can produce logic errors. Proper distribution of the bias currents within SFQ circuits is, therefore, critical for continuing the integration of SFQ circuits toward LSI and VLSI levels of complexity. As the bias lines in SFQ circuits are lossless and inductive, EDA tools require a novel set of guidelines, heuristics, and algorithms for the automated generation of bias networks for SFQ-based VLSI circuits.

Multiple guidelines and design techniques exist for ERSFQ bias networks [9]–[13]. In this article, a semiautomated analysis methodology is used to develop novel parameter guidelines, as well as expand and clarify some existing guidelines. In addition, an ERSFQ topology utilizing multiple clock domains—an extension of the approach proposed in [12]—is described. Some of the guidelines described in this article are also briefly discussed in [14].

This article is organized as follows. In Section II, a brief overview of RSFQ technology is provided, with a focus on the bias networks and related energy-efficient modifications. In Section III, a semiautomated analysis methodology is presented. This methodology is used to develop design guidelines for ERSFQ bias networks, as described in Section IV. In Section V, a distributed placement methodology for ERSFQ bias networks is presented. In Section VI, some conclusions are offered.

II. Background

In this section, a brief background on RSFQ circuit structures, operation, and biasing is provided. In Section II-A, RSFQ circuits and related operational principles are reviewed. In Sections II-B and II-C, respectively, RSFQ bias networks are described, and related energy-efficient circuit modifications are discussed.

A. RSFQ Circuit Operation

RSFQ technology [4] is a logic family for cryogenic superconductive computing based on Josephson junctions (JJs)

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and niobium interconnect, which exhibits superconductivity at 4.2 K—the standard operational temperature for these circuits, typically cooled by liquid helium. Magnetic flux within a superconductive loop is quantized. In an RSFQ logic family, information is represented as single-flux quantum (SFQ) pulses—voltage pulses with a quantized area of $\Phi_0 \approx 2.07$ mV·ps. The occurrence or absence of an SFQ pulse during a specific clock period represents, respectfully, a logic one and zero state. RSFQ gates are composed of different combinations of superconductive loops storing and not storing a magnetic flux quantum depending upon the target function. These gates are typically clocked, where a logic zero is represented as the absence of an SFQ pulse within a clock period.

Each SFQ pulse corresponds to a shift in the superconductive phase difference across a critically damped (shunted) [15] JJ by 2π—an event referred to as switching a JJ. SFQ pulses are transferred across a circuit by two distinct types of transmission lines—active Josephson transmission lines (JTLs) and passive transmission lines (PTLs) [16]. Multiple advantages and disadvantages exist for each type of transmission line [17]; both types of transmission lines are commonly used as interconnect in RSFQ circuits. Bias structures in ERSFQ primarily utilize JTLs, as described in Section II-C.

A JTL is a chain of grounded, shunted, and biased JJs connected in parallel by small inductors. The phase of these JJs changes by 2π upon the arrival of an SFQ pulse, regenerating and passing the pulse along. As the inductance between JJs is typically fixed, the length of a JTL is the number of stages (or JJs) within a transmission line.

B. Bias Distribution in RSFQ Circuits

The primary parameter of a Josephson junction is the critical current I_c. This current corresponds to the transition between the superconductive state and the voltage state of a JJ and is directly related to the physical area of the JJ. The JJs within an RSFQ circuit are directly or indirectly biased to a specific fraction of I_c to maintain proper operation [4]. Local bias distribution within each gate is performed by an inductive network, consisting of inductors and JJs, with one or two bias network connections per gate. Each gate is typically individually optimized—the inductance and critical current of the JJs are chosen to produce robust operation and small delay.

The objective of a bias distribution network within a complex RSFQ circuit is to supply a precise bias current to each gate. In conventional RSFQ circuits, the bias current is distributed and regulated by a resistive tree network [4]. The current is typically supplied off-chip and transferred to the gates by superconductive wires, where each cell contains a bias resistor. Unlike CMOS bias networks, which exhibit some distributed resistance per length, an RSFQ bias network is lossless until the point of load [5]. Within each cell, the bias current is distributed by inductive current division, where the nonlinear inductance of the JJs is also considered.

The resistors within the gates dissipate significant static power, approximately 60 times greater than the dynamic power dissipated during a JJ switching event at a clock frequency of 20 GHz ($P_D = I_b * \Phi_0 * f_s$, ~13 nW per gate) [18]. Moreover, most of this power dissipation occurs close to the thermally sensitive superconductive elements.

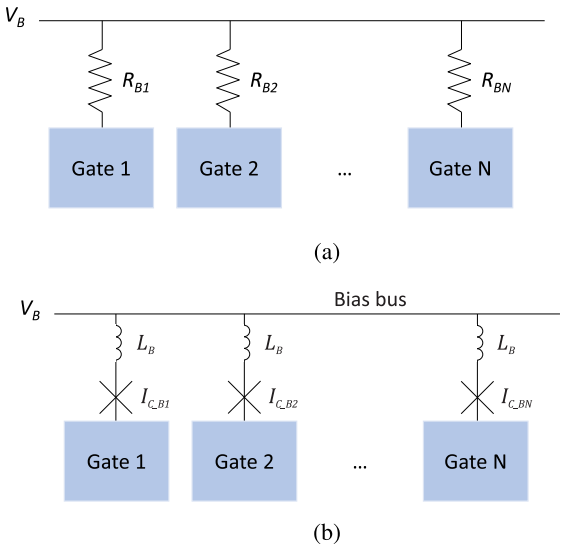


Fig. 1. Bias schemes. (a) Conventional RSFQ. (b) ERSFQ.

Multiple solutions have been proposed to lower static power dissipation in RSFQ circuits. One approach requires modifying the bias distribution elements and bias voltages [19]. Dual-rail RSFQ changes the topology of the gates and signaling scheme to enable inductive current distribution [20]. Alternative superconductive logic families have been proposed, such as quantum flux parametron (QFP) logic [21] and reciprocal quantum logic (RQL) [22]. These logic families utilize an ac signal for both clock and bias, thereby eliminating any static power dissipation within the cryogenic environment. In this article, only ERSFQ [5] is considered.

All these issues and concerns emphasize the importance of the correct and efficient distribution of the bias currents within large-scale SFQ circuits. These bias distribution structures need to be synthesizable by prospective SFQ EDA tools to support the increasing complexity of RSFQ circuits. In this article, guidelines, tradeoffs, and techniques for efficient current bias networks are presented.

C. Energy-Efficient SFQ

In ERSFQ circuits [5], the dissipative resistors within RSFQ are replaced with JJs and superconductive inductors. This modification eliminates any static power dissipation, thereby reducing the total dissipated energy by two orders of magnitude [18]. These JJs function as current limiters—when the current passing through these bias JJs approaches the critical current I_c, the inductance of the JJ rapidly increases. If the current exceeds I_c, the bias JJ momentarily transitions into a voltage state, diverting any additional current within the bias network. Conversion between RSFQ and ERSFQ gates does not require any changes to existing cell libraries, only affecting the bias distribution elements [23]. These bias schemes are schematically depicted in Fig. 1.

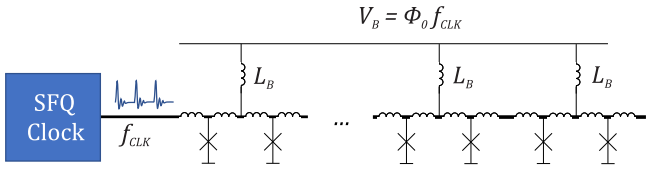


Fig. 2. FJTL connected to an SFQ clock line acting as a voltage reference.

Multiple modifications are necessary to support inductive bias distribution. Switching the bias JJs produces current fluctuations on the order of Φ_0/L_B, where L_B is the bias inductance connected in series with the bias JJ [5]. A large L_B, therefore, reduces the bias current ripple although a large inductor (hundreds of pH) requires significant area. This tradeoff has led to modifications in some fabrication processes, for example, the introduction of a high kinetic inductance layer [24].

The average voltage for a gate switching at a frequency f_s is $\Phi_0 * f_s$. To prevent current redistribution, the voltage on the bias bus should be higher than any gate voltage within the circuit. This constraint is achieved by connecting the bias bus to the clock line—the average voltage on the clock line is guaranteed to be equal or greater than any gate voltage since the clock operates at the highest frequency in a circuit. The clock line is connected to a structure called a feeding JTL (FJTL) to increase both the stability of the voltage reference and the bias margins.

An FJTL is schematically depicted in Fig. 2. An FJTL is a JTL consisting of multiple stages, where each stage is connected to the bias bus by a large inductor L_B. This JTL is typically terminated, and the output is not utilized. The FJTL establishes a robust voltage reference for the bias bus of an ERSFQ circuit and improves the margins of operation by supplying additional or receiving excess bias current.

Some commonly used *ad hoc* design approaches [9], [10] and guidelines [11]–[13] currently exist on the proper design of ERSFQ bias networks. One rule of thumb is related to the size of the FJTL, which is typically chosen to ensure that the FJTL bias current is about 25% to 30% of the load bias current. The dependence of the margins on the operating frequency of an FJTL has also been considered [9].

The importance of the parasitic inductance of the bias bus is emphasized in [12], where different bias inductances produce different current distributions. This dependence is discussed in Section IV-E, where design guidelines for increasing the robustness of the bias network are provided. Techniques to reduce current deviations in ERSFQ bias networks have been proposed in [13], along with some guidelines on FJTL size. Another study has suggested optimal values for certain ERSFQ component parameters, such as the bias inductance and size of the FJTL [11]. The effect of the size of the FJTL on the operational range of the ERSFQ bias networks is discussed here, and design guidelines for a preferable FJTL size are provided. Among the issues first discussed here are the optimal

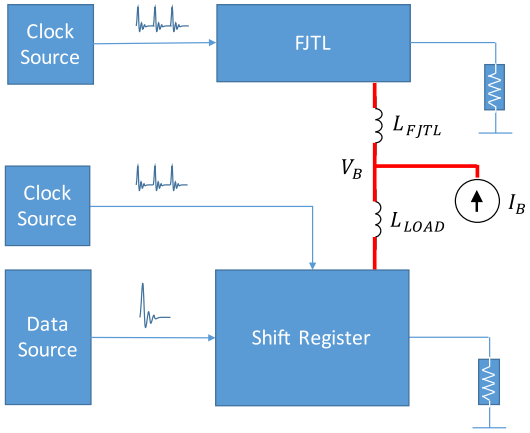


Fig. 3. Example topology of the ERSFQ biased circuit used in this analysis.

topology of the FJTL stage and the effect of the FJTL bias margins on the bias margins of the circuit.

As the size and topology of the FJTL affect the physical area and bias currents, additional guidelines are required to integrate ERSFQ circuits into an industrial design flow. These design guidelines are further discussed in Section IV.

III. Example Circuit and Analysis Methodology

An ERSFQ bias network is composed of a variety of different elements, where each gate contains a highly nonlinear JJ as a current regulator. This structure makes infeasible the development of closed-form analytic expressions characterizing the behavior of a bias network. An analysis of the bias network is, therefore, limited to observations of trends and the effects of different component parameters on circuit behavior.

For this analysis, a semiautomated script is used to perform multiple circuit simulations in the WRSpice simulator [25] to extract behavioral trends. Two primary circuit components of an ERSFQ bias network are the load, which requires a bias current I_B and an FJTL, which functions as a voltage source with a maximum average voltage V_B. This topology, schematically shown in Fig. 3, is used to monitor the bias current within the load and extract parametric trends.

A general ERSFQ circuit is used as a standard load, especially a shift register composed of multiple D flip-flops chained together with JTLs. A shift register, a common topology in complex ERSFQ circuits, is extendable, robust, and exhibits wide parameter margins. The shift register is synchronized by an H-tree clock distribution network consisting of a binary splitter tree buffered by JTLs. In this analysis, 16-, 32-, and 64-stage registers are used to manage the simulation time. An H-tree clock network is chosen due to wide parameter margins and to increase the size of the load.

A chain of JTL stages is used as an FJTL. The number of stages is varied, and the results presented in Section IV are described in terms of the total FJTL bias current. The FJTL can ideally operate at the same clock frequency as the rest of the circuit. This approach dissipates minimal power while maintaining ERSFQ operation. The range and robustness of such an operation, are, however, reduced. Higher FJTL frequencies, although beneficial for system bias

margins, dissipate more power. In this analysis, the system clock frequency is 10 GHz, while the FJTL frequency is 12.5 GHz.

The data source generates a train of SFQ pulses with a specific pattern, representing the input data. This pattern affects the activity factor of the load, directly changing the gate voltage (V_{GATE} in Fig. 1), and, therefore, the behavior of the bias network. The clock sources generate a train of SFQ pulses representing the primary system clock signal. The output of both the chain of FJTL stages and the shift register is terminated by a resistive load. All circuits are from the Stony Brook Cell Library and [4]. As the Stony Brook Cell Library utilizes normalized parameter values, the standard critical current of the JJs is 250 μA. The bias margins of the FJTL are varied, as described in Section IV-C, but are generally above $\pm$40%. The bias margins of the shift register are above 30%.

The input and output data streams of the shift register are compared to verify circuit operation. The output of the WRSpice simulation is parsed to extract all 2π phase transitions of the input and output JJs. These transitions are aligned with the transitions of the JJs within the clock network, where the clock transitions are measured at the sinks of the network. The resulting bit patterns are compared. This methodology supports a bias margin analysis, where the bias current is either swept linearly or modified in a binary search pattern, and the upper/lower bounds that ensure correct operation are determined.

The primary metric of the robustness of operation in RSFQ circuits is the bias margins. The bias margins are a measure of the additional or absent bias current tolerated by a circuit. The ERSFQ bias networks affect the bias margins due to dynamic redistribution of the bias currents between the FJTL and the many loads. The ERSFQ bias margins are limited, however, by the intrinsic bias margins of a properly biased and optimized RSFQ circuit. These margins typically do not exceed 20% for circuits of intermediate complexity and are often lower for more complex circuits [26]. It is, therefore, infeasible to optimize an ERSFQ bias network within a large circuit to achieve margins of operation wider than 20%–30%. In this range, the overall bias margins of a system containing an ERSFQ load and an FJTL primarily depend upon the actual bias current supplied by the bias network to the load. The average magnitude and variation of the different currents within a circuit are therefore extracted to observe behavioral trends and more efficiently estimate the resulting bias margins.

Under ideal conditions, an FJTL is only used to establish a voltage reference. In nonideal conditions, an FJTL compensates for the bias current in the load by redistributing (sacrificing) bias current to the load. To investigate these capabilities, an ERSFQ bias network is evaluated in both overbiased and underbiased conditions.

The underbiased condition corresponds to the case where the supplied bias current is lower than the target design objective. In the underbiased condition, reduced bias current in the FJTL does not initially affect the operation of the FJTL until the bias current is below the lower bias margin. At this current, the FJTL ceases to function properly (missed SFQ pulses or the absence of any switching in the FJTL). This underbiased FJTL produces a bias voltage that is lower than necessary. While several skipped pulses may not significantly change the bias voltage, a sufficiently underbiased FJTL terminates operation, making a reliable voltage reference no longer available. The underbiased load, depending upon the bias current, either exhibits increased delay or ceases operation.

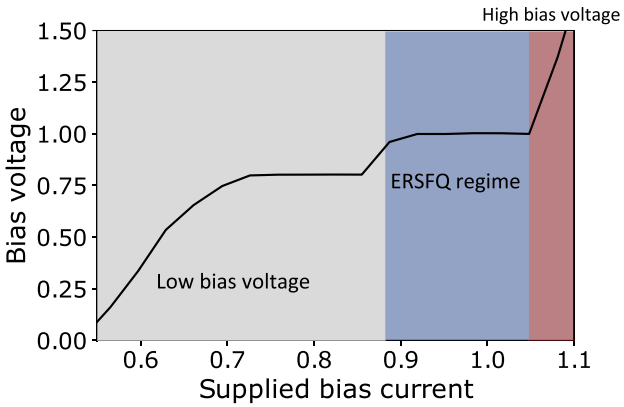


Fig. 4. Regions of operation of the ERSFQ system.

The overbiased condition occurs when the supplied bias current exceeds the target design objective. In the overbiased condition, increased bias current in the FJTL does not affect the operation of the FJTL until the bias current is above the upper bias margin. At this current, the FJTL increases the switching rate, producing additional SFQ pulses. This overbiased FJTL produces a bias voltage that is higher than necessary. While this regime of operation does not affect the proper operation of the load, this system is highly energy inefficient. This inefficiency is due to the additional switching of the JJs in both the FJTL and the bias JJs within the load. The overbiased load, depending upon the bias current, exhibits either a slightly decreased delay or operates incorrectly.

A range of ERSFQ operation exists where the FJTL regulates the voltage and load current. While the circuit can operate outside of this range, the circuit will exhibit either suboptimal timing characteristics (the underbiased case) or is energy inefficient (the overbiased case).

This operational range is illustrated in Fig. 4 for a simple example—an FJTL connected to two JTL loads: one constantly switching due to the incoming data pulses and another not switching. The operation of a similar system had been modeled in [12]. In this figure, the dependence of the bias voltage on the supplied bias current is shown. The bias voltage is normalized to 25.85 μV ($\Phi_0 \times 12.5$ GHz)—a nominal bias voltage. The bias current is normalized to the target bias current of the system. The plateau around the bias current normalized to one (1.0) corresponds to the optimal range of operation of the ERSFQ biased system. A higher bias current rapidly increases the bias voltage, expending significant energy. A lower bias current first produces another plateau, corresponding to the absence of switching in the FJTL. In this regime, the switching part of the load produces a lower bias voltage. Finally, if the bias current is further lowered, the load ceases to operate. In Section IV, similar

underbiased and overbiased conditions are evaluated for different design parameters that would increase the range of ERSFQ operation.

IV. Trends and Guidelines of ERSFQ Bias Networks

In this section, certain parametric trends characterizing a bias network are discussed, and guidelines for ERSFQ bias network design tools are proposed. The system evaluated in this section is described in Section III and shown in Fig. 3. A metric frequently used in this section to evaluate these parametric trends is the dependence of the bias current supplied to the load on the bias current supplied to the system. The actual load bias current, in this case, is normalized to the design (target) load bias current—the sum of the critical currents of all of the bias JJs within the load. This normalization enables a comparison of the actual bias current to the bias margins of the load. The bias current supplied to the system is normalized to the sum of the target load bias current and the target FJTL bias current—the sum of the bias currents of all of the FJTL JJs when biased at 0.7 of the critical current. This approach enables the simulation of the underbiased/overbiased condition of the entire ERSFQ-biased system to be normalized. The primary focus of this section is to evaluate the behavior of the FJTL in terms of these parametric trends; slight variations in the extracted bias current are due to redistribution of the bias current from the load to the FJTL. In Section IV-A, the effect of the bias inductance on current variations is compared with theoretical expectations. In Section IV-B, two different topologies of an FJTL stage are considered in terms of the bias distribution and energy efficiency. In Section IV-C, the effect of the bias margins of an FJTL on the overall system-wide bias margins is discussed. In Section IV-D, the effect of the size of the FJTL on the bias distribution network is evaluated, and design guidelines for the preferable size of the FJTL are suggested. In Section IV-E, the effect of the inductance of the source-to-FJTL path and source-to-load path on the supplied current in the presence of transient supply variations is described, and an approach to increase the inductance of the source-to-FJTL path is discussed.

A. Bias Inductance

ERSFQ gates are connected to a bias bus through large bias inductors. These inductors filter the high-frequency current variations and reduce the amplitude of the bias current ripple, thereby reducing the probability of erroneously switching the JJs within the logic gates. A comparison of an analytic expression of the magnitude of the current ripple to simulations is described in this section to verify the correctness of the analysis process.

The dependence of the current variations on the bias inductance is illustrated in Fig. 5, where zero on the vertical axis is the average bias current. The overlapping plots depict the deviation from the average current for three different FJTL sizes. As noted in Fig. 5, the simulated variations in bias current are in good agreement with the theoretical value of Φ_0/L_B [5] and with the simulation results described in [11]. Similar to [11], any additional inductance more than

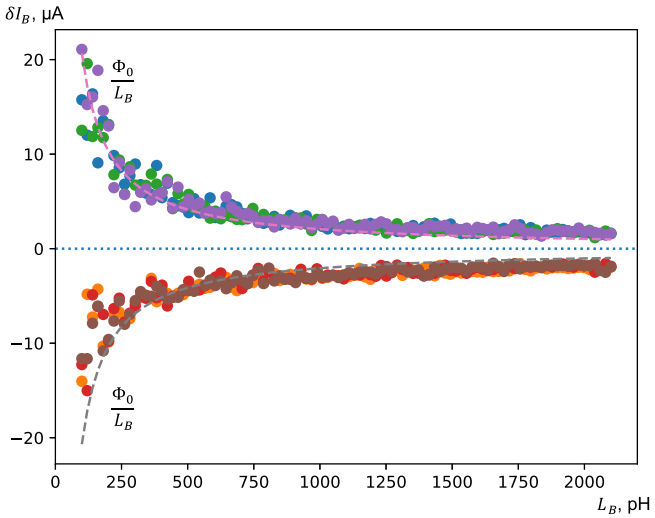


Fig. 5. Dependence of current variations on the bias inductance. The dashed line is the analytic expression.

200–300 pH produces a negligible decrease in bias variations as compared with a typical bias current of an RSFQ gate. This example supports the application of this simulation analysis methodology to more complex parametric analyses.

B. Topology of FJTL Stage

One of the primary decisions in the automated synthesis of ERSFQ bias networks is the topology of the FJTL stage. Two methods exist for designing these structures—with [11], [18] and without [5], [27] a bias limiting JJ within the JTL stage. Different damping conditions for this bias JJ should be considered [11]. These parameters affect the size and efficiency of an FJTL and are, therefore, discussed in this section.

In underbiased circuits, no effect occurs from the presence of bias limiting JJs within an FJTL. As the bias of each individual stage is lower than the critical current of the bias limiting JJ, these JJs never switch, only slightly adding to the bias inductance as well as significantly increasing the area.

In overbiased circuits, the bias limiting JJs in both the FJTL and load continuously switch. This behavior increases the energy dissipation and decreases the ability of the FJTL to absorb any excess bias currents. Without bias limiting JJs, however, the bias current supplied to the FJTL can exceed the upper bias margin of the FJTL, increasing the switching rate of the junctions within the FJTL, which, in turn, dissipates more dynamic energy. A nontrivial tradeoff among the area, energy, and bias regulation capability, therefore, exists.

A comparison of the bias regulation capability for an FJTL without a bias JJ, as well as an FJTL with different sizes of the bias JJ, is shown in Fig. 6. The bias JJs are assumed to either be critically damped or overdamped. Note that no difference in bias current distribution occurs in the underbiased circuits. For the overbiased circuits, the FJTL without bias JJs produces a preferable bias distribution for the overbiased case (a smaller bias current in the load). From Fig. 6, the FJTL with overdamped bias junctions follows the same trend although

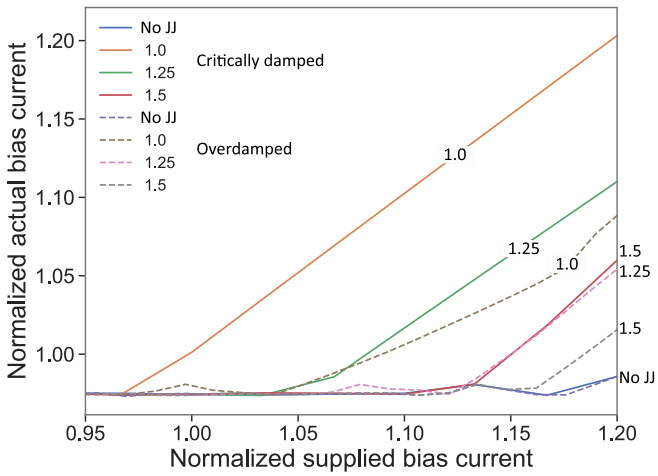


Fig. 6. Dependence of load bias current on supplied bias current for the critically damped and overdamped bias JJs within an FJTL. The example FJTL contains 64 stages, corresponding to 50% of the load bias current. The critical current of the bias JJ is normalized to 350 μA. Three different sizes of bias JJs (standard size, 25% greater size, and 50% greater size) are considered, as well as the absence of a bias JJ.

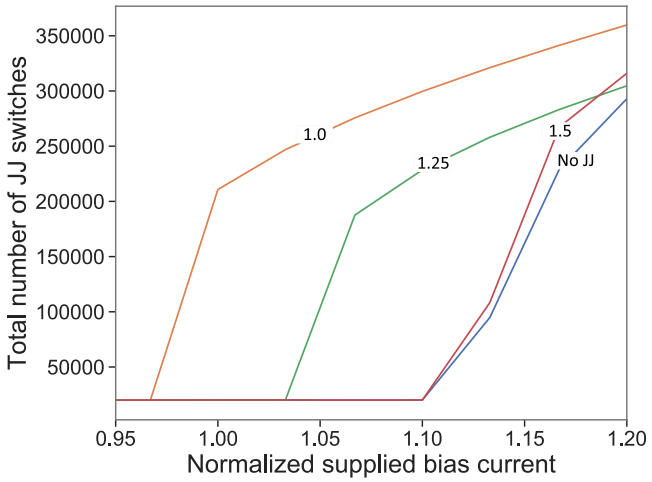


Fig. 7. Dependence of the total number of bias JJ switches and FJTL switches on supplied bias current. The critical current of the bias JJ is normalized to 350 μA. Three different sizes of bias JJs (standard size, 25% greater size, and 50% greater size) are considered, as well as the absence of a bias JJ.

the bias distribution with overdamped bias JJs is improved as compared with an FJTL with critically damped bias JJs. An FJTL without bias JJs in an overbiased circuit diverts more bias current into the FJTL.

A comparison of the dynamic energy dissipation is shown in Fig. 7. The dynamic energy is based on the total number of JJ switching events during a fixed time period for different bias levels. FJTLs without bias JJs dissipate less energy for all reasonable bias current levels (below 20% overbiasing) despite the higher switching activity of the FJTL operating in the overbiased region.

C. Bias Margins of FJTL

The purpose of an FJTL in an ERSFQ circuit, apart from providing a voltage source, is to absorb excess bias current in the overbiased circuits and provide additional bias current

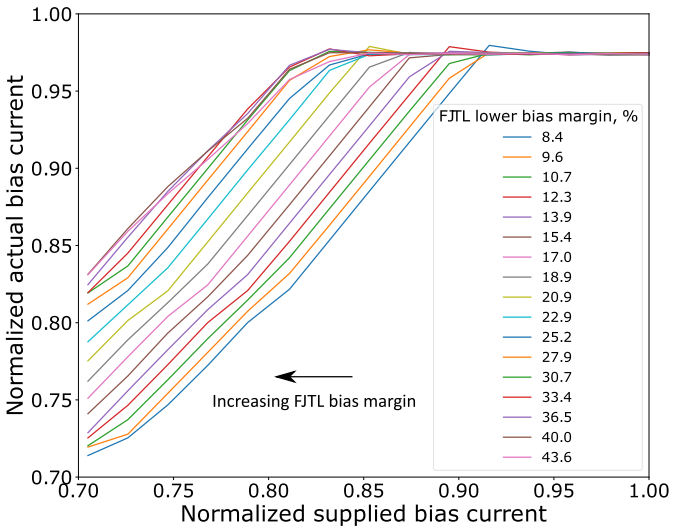


Fig. 8. Dependence of load bias current on supplied bias current for FJTL with the same size and different bias margins (8.4%–43.6%).

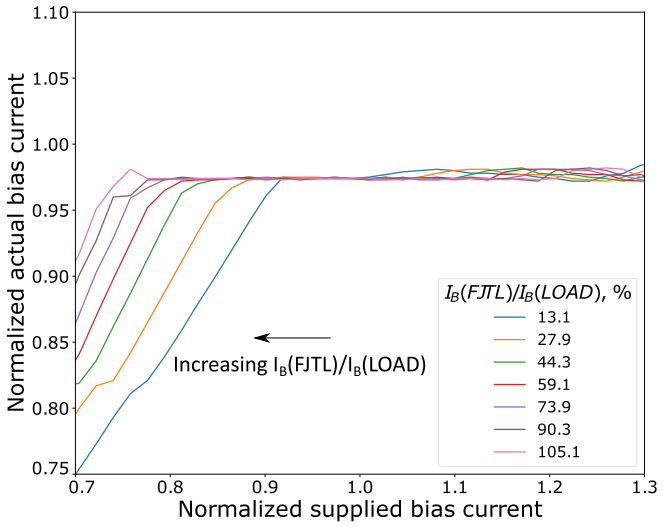
to the underbiased circuits. An FJTL, therefore, experiences large current variations as a part of the intended behavior. Despite an FJTL behaving as an analog voltage reference, the correct operation of an FJTL depends upon the ability to pass SFQ pulses. Bias variations can produce either additional SFQ pulses or insufficient SFQ pulses to establish the correct bias voltage. An FJTL is, therefore, considered, in this section, as a digital transmission line, and the effects of the bias margins of the FJTL are discussed.

In overbiased circuits, an FJTL can switch more frequently, raising the voltage on the bias bus, expending additional energy. In underbiased circuits, an FJTL can either skip multiple SFQ pulses or completely cease operation, resulting in a loss of the voltage source and incorrect bias distribution. Wider FJTL bias margins improve the energy efficiency of overbiased circuits. In underbiased circuits, wider FJTL bias margins can increase the bias current in the load, ensuring the circuit operates properly at lower bias levels.

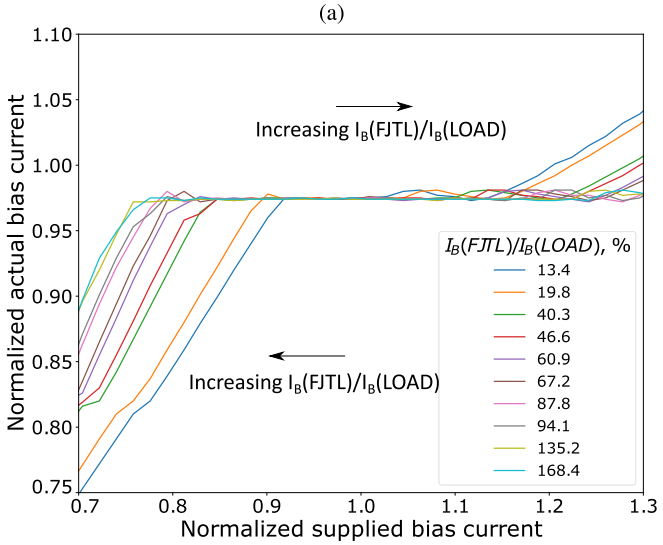
As confirmed in Fig. 8, wider bias margins of an FJTL improve the distribution of the bias current in underbiased circuits and enable correct operation with a lower supplied bias current. The benefits of higher FJTL bias margins diminish beyond a bias margin of about 40%.

D. Size of FJTL

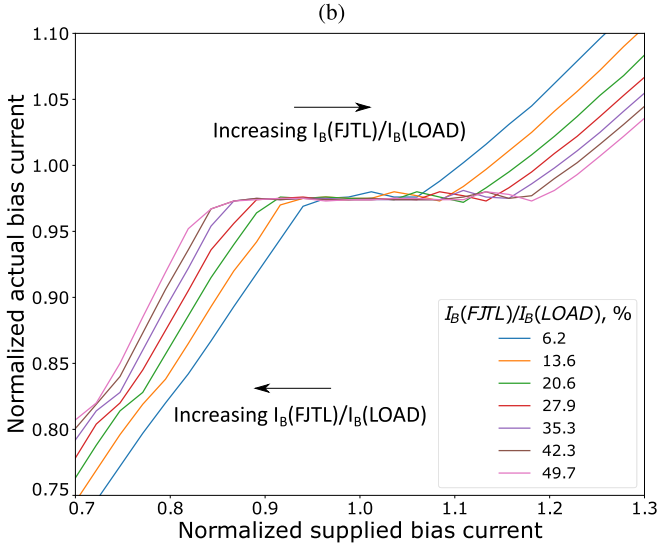
The size of an FJTL—the total bias current of all of the JTL stages comprising an FJTL—is another important parameter in ERSFQ bias networks. This current is typically compared with or normalized to the bias current of the load connected to the FJTL. With the JTL cells as a part of a standard cell library, the total FJTL bias current is set by the number of stages. A larger FJTL can provide or absorb more current from the load and, therefore, better distribute the bias current. Additional stages, however, increase area and energy dissipation. In this section, those factors affecting the reasonable size of an FJTL for large-scale circuits are discussed.



(a)



(b)



(c)

Fig. 9. Dependence of load bias current on the supplied bias current. (a) 8-bit load (21.31 mA). (b) 16-bit load (44.27 mA). (c) 32-bit load (90.19 mA).

Different FJTLs and loads are evaluated for different supplied bias currents, as presented in Fig. 9. Note that a larger FJTL produces a preferable bias distribution in all cases, with the bias current closer to the target objective (smaller for overbiased cases and larger for underbiased cases). The benefits of increasing FJTL size, however, diminish with additional stages.

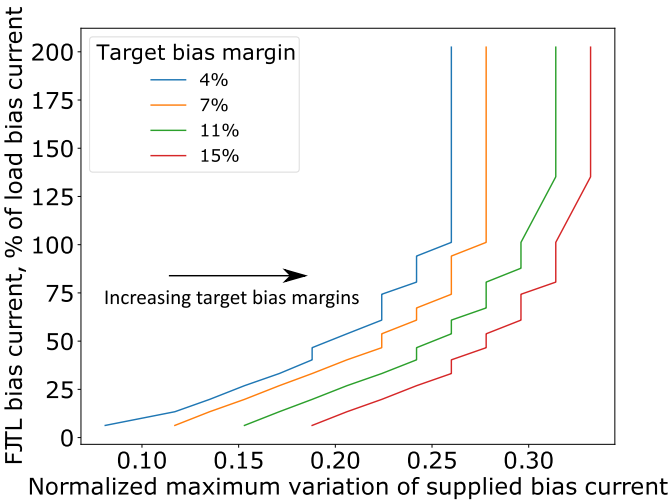


Fig. 10. Dependence of FJTL size on desired bias variations and expected supply variations.

To constrain the size of an FJTL and provide effective design guidelines, two additional design parameters are necessary. One parameter is the target bias variations—the maximum bias current variations of an ERSFQ system, including the FJTL. This target is constrained by those circuits with minimum bias margins within the load (least robust). An ERSFQ system is designed to guarantee to not exceed this bias margin.

The second design parameter is the maximum variation of the supplied bias current. This current is determined by the characteristics of the external bias source and the physical layout. In ERSFQ circuits with current recycling [28], [29], the maximum variation is the difference in bias current between serially biased circuit partitions.

The dependence of the size of an FJTL on the maximum variation of the supplied bias current and target bias current variations is shown in Fig. 10. The benefits of adding more stages to an FJTL diminish after the FJTL bias current exceeds approximately 50% of the load bias. In those cases where large bias variations are not expected, the bias current of an FJTL can be as small as 0%–10% of the load bias current. For overbiased circuits, larger FJTLs further increase the range of energy-efficient operation, enhancing the robustness of the system against larger variations.

E. Inductance of Bias Bus

In ERSFQ bias networks, the bias bus is the line connecting an FJTL and load to a current source (the off-chip bias source connected to the on-chip I/O port). The inductance of this bias bus, typically parasitic, consists of two parts—the inductance L_{LOAD} between the current source (the I/O port) and the load, and the inductance L_{FJTL} between the current source and the FJTL. This topology is schematically depicted in Fig. 3. These inductances are extracted from the physical dimensions of the bias lines. In this section, the effects of the inductance of this bias bus are discussed.

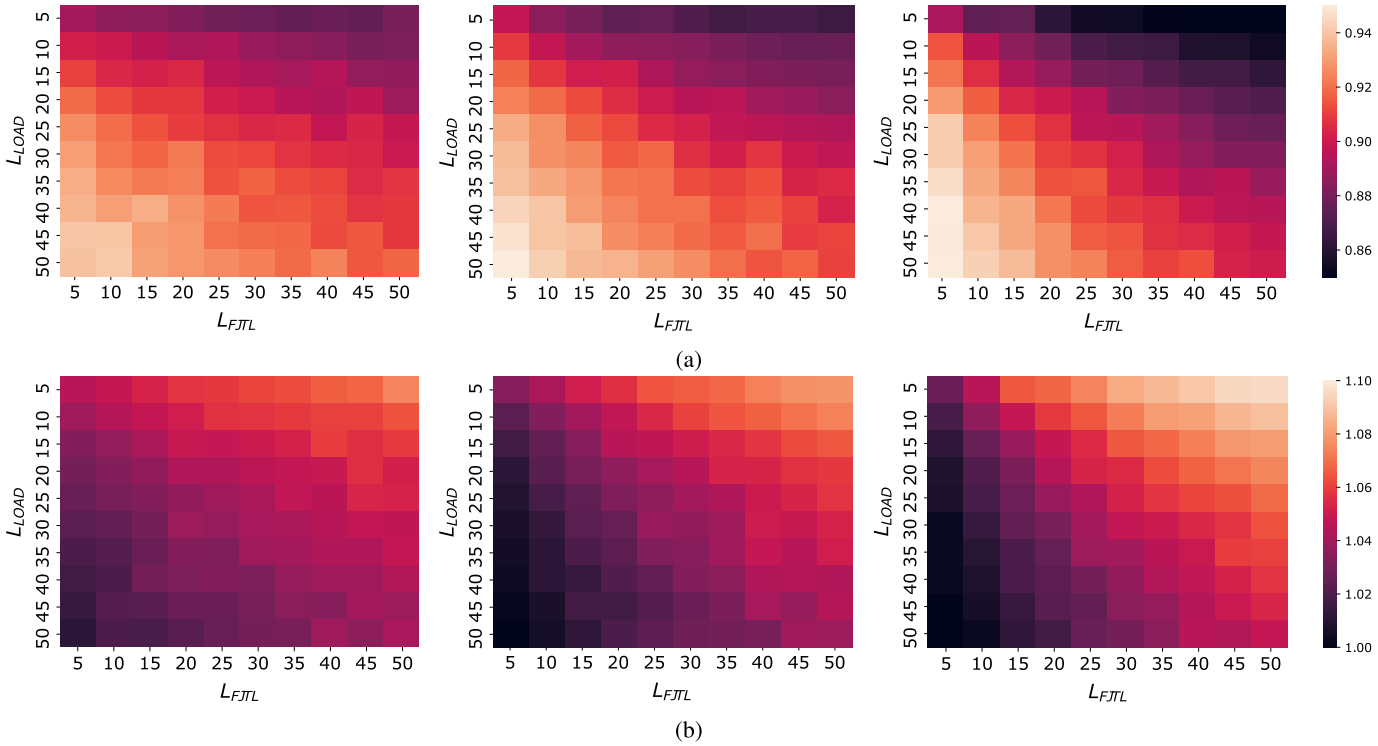


Fig. 11. Bias current in the load normalized to the target bias current in the load. The bias current supplied to the system is momentarily changed to (a) 90% and (b) 110% of the nominal current. The three different FJTL sizes (bias currents) correspond to, respectively, left to right, 12.5%, 25%, and 50% of the load bias current. The brighter areas represent higher current. (a) 90% of target bias current. (b) 110% of target bias current.

L_{LOAD} and L_{FJTL} form an inductive current divider, splitting the bias current between the FJTL and the load. While the steady-state current distribution depends upon the average voltage on the bias bus and the bias node within the cell, L_{LOAD} and L_{FJTL} affect the transient current distribution. By modifying the ratio of this current divider, additional bias current can be steered into the load in the case of a sudden decrease in bias current. An FJTL is among the most robust RSFQ circuits and exhibits wide parameter margins. Moreover, the output of an FJTL is typically not used, and therefore, the errors do not directly affect the circuit function. By redistributing additional bias current from the FJTL into the load, the function is preserved despite the system being temporarily underbiased.

Although the bias current eventually converges to the same current for all values of inductance, this approach improves the transient operation of the underbiased circuits in the presence of bias current variations and preserves the correct circuit operation when the bias current is temporarily reduced. This approach, however, further reduces the bias current supplied to an FJTL, partially sacrificing the high bias margins of the FJTL.

To isolate the load from changes in the supplied current, the inductance of the source-to-load path L_{LOAD} is increased. To enable an FJTL to accommodate changes in the bias current, the inductance of the source-to-FJTL path L_{FJTL} is decreased. These conditions can be converted into physical guidelines for bias network placement algorithms. The load should be placed farther from the I/O port, while the FJTL should be placed closer to the source. Alternatively, the wire shape can be modified to increase the inductance of the source-to-load path, or an additional inductor can be added.

While the effect described here could be achieved by increasing the bias inductance of the load as compared with the bias inductance of the FJTL, an additional external inductance produces a less complex circuit layout. The bias inductors are connected in parallel. A large L_{LOAD} translates into a much higher L_B within the load, requiring more physical area.

Redistribution of bias current from an FJTL does not initially affect the operation of the FJTL until the bias current is below the bias margin, where the FJTL ceases to function properly (missed SFQ pulses or the absence of any switching in the FJTL). While several skipped pulses may not significantly change the bias voltage, a sufficiently underbiased FJTL terminates the operation, removing the voltage reference from the system. The proposed approach is, therefore, constrained by the bias margins of the FJTL. An analysis of the proposed methodology is illustrated in Fig. 11. In Fig. 11(a), the supplied bias current of the system momentarily changes to 90% of the target bias current. In Fig. 11(b), the supplied bias current of the system momentarily changes to 110% of the target bias current. In Fig. 11(a) and (b), respectively, the minimum and maximum bias currents in the load are shown, normalized to the target load bias current.

The inductances, L_{FJTL} and L_{LOAD}, are varied from 5 to 50 pH. These inductances are chosen, somewhat arbitrarily, to demonstrate the proposed approach. The small inductance case is chosen as 5 pH, where the inductance is assumed to be mostly parasitic, and the number of bias inductors connected in parallel is large. The large inductance is limited to 50 pH to reduce simulation time. The size (bias current) of the FJTL

is also varied from 13% to 50% of the load bias current. Currents closer to the target bias current are indicative of a more beneficial parameter set. The less shaded areas in Fig. 11 correspond to a higher bias current in the load—a desirable condition for underbiased circuits and an undesirable condition for overbiased circuits.

From Fig. 11, the difference between the highest and lowest bias currents for different values of inductance in both underbiased and overbiased circuits can be over 11% of the load bias current for the case with a large FJTL (50% of the load bias current). For smaller FJTLs, this difference in the load bias current, dependent on the inductance, is smaller but over 6%. The choice of an optimal inductance is, therefore, important to improve the distribution of bias current in the presence of variations in the bias supply. As illustrated in Fig. 11, it is indeed desirable to increase the inductance of the source-to-load path and decrease the inductance of the source-to-FJTL path to improve the behavior of ERSFQ bias networks during transient changes in the supplied current.

V. Distributed FJTL Methodology

In this section, a methodology for distributed FJTL placement in large-scale ERSFQ circuits is proposed based on the guidelines described in Section IV. Current design approaches commonly utilize one large FJTL for the entire IC [9]. This approach is suitable for small and medium-scale ICs, enabling the fast design of operational FJTLs and less complex testing. In addition, this approach is commonly used in test circuits, where additional control and signal inputs are available for the bias network.

A single FJTL, however, is not optimal for VLSI ERSFQ circuits. In these circuits, the desirable size of an FJTL can be on the order of hundreds of thousands of stages, requiring large on-chip area. In large-scale circuits, different components operate at different clock frequencies. A single common FJTL for an entire IC would necessarily operate at the highest of these frequencies, dissipating unnecessary dynamic power. As discussed in Section IV-D, the size of an FJTL depends upon the target bias margins. Different blocks and components within a complex circuit exhibit different target bias margins, resulting in different sizes for the corresponding FJTL. Requiring the strictest target bias margins from all FJTLs unnecessarily overdesigns the bias network, increasing both the physical area and dynamic power dissipation.

Furthermore, as suggested in Section IV-E, the inductance of the source-to-load path should be higher than the inductance of the source-to-FJTL path. In modern ERSFQ ICs, each input supplies only a small fraction of the total required on-chip bias current (a few hundred milliamperes). In prospective VLSI circuits, this fraction of the on-chip bias current will further decrease as the bias requirements increase. In circuits with a single FJTL, current from multiple bias pins is combined to provide the overall current. This shared bias bus spans the entire IC. Parasitic inductances within this bus are difficult to control and balance, making this topology inappropriate for large-scale circuits.

In the proposed methodology, a VLSI ERSFQ circuit is subdivided into smaller blocks, consisting of circuits of similar complexity (and, therefore, similar target bias margins) and clock frequency. A similar approach is described in [12]. Each partition is connected to a separate FJTL and one or more independent bias pins. This approach enhances the control of both the FJTL characteristics and the parasitic inductances within each block, preventing overdesign of the bias network. Each distributed FJTL is connected to the clock source within the corresponding block, thereby operating at the correct local clock frequency.

Consider a large-scale ERSFQ circuit with 20 000 gates divided into two different clock domains of equal size with a clock frequency of 20 and 50 GHz. Assuming that each gate requires an average bias current of 500 μA, the total bias current is approximately 10 A. If the necessary bias current of the FJTL for this circuit is 15% of the total bias current (1.5 A) and the bias current of each FJTL stage is 350 μA, 4285 FJTL stages (8570 JJs) would be required. In the case of a single lumped FJTL, this topology would dissipate a dynamic power $P_D \approx (175\ \mu\text{A}) * \Phi_0 * (50\ \text{GHz}) * 8570 \approx 155\ \mu\text{W}$. In the case of two separate FJTLs, each operating at the corresponding clock frequency (20 and 50 GHz), $P_D \approx 77.5\ \mu\text{W} + 31\ \mu\text{W} \approx 109\ \mu\text{W}$, an approximate 30% improvement. This example illustrates the savings in dynamic power from the proposed methodology.

The disadvantage of the proposed methodology is a significant increase in circuit complexity. Multiple FJTLs operating at different frequencies require separate connections to corresponding bias networks. Separation of a large-scale circuit into multiple clock domains requires separate clock and bias networks, as well as synchronization elements for crossing clock domains.

Furthermore, this approach can be combined with current recycling techniques [30], where each partition is placed on a separate ground plane to reduce the total bias current. Partitions with equal bias currents are necessary for current recycling. FJTLs connected to a clock line can balance the bias requirements of different partitions while maintaining zero static power dissipation [29].

VI. Conclusions

In this article, the bias distribution network for a cryogenic electronics technology—ERSFQ logic—is discussed. Robust bias networks are essential for the integration of ERSFQ circuits into LSI and VLSI complexity systems.

For different components within an ERSFQ bias network, trends are considered and advantageous tradeoffs are discussed. These design guidelines enable more robust ERSFQ circuits resistant to severe variations in bias current. Trends and tradeoffs described in this article provide a means to decrease the bias current of FJTLs within large-scale ERSFQ circuits, thereby reducing physical area and power dissipation.

A methodology for the distributed placement of ERSFQ FJTLs in large-scale circuits is described. This methodology enables precise control of the parasitic inductances within a bias network, reducing the area and power as compared to a single large FJTL. The proposed methodology and guidelines can be integrated into commercial EDA bias network design

tools for prospective ERSFQ VLSI circuits, incentivizing SFQ as a promising beyond CMOS technology.

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