# Distributed Pass Gates in Power Delivery Systems With Digital Low-Dropout Regulators

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***Abstract*— On-chip digital low-dropout (LDO) regulators enable fast dynamic voltage scaling, reducing power consumption. Integrating these regulators into a highly resistive environment has complicated the design of power delivery systems. With the increasing sensitivity of complex integrated systems to power noise, effective approaches to distribute on-chip LDOs are needed due to the limited metal resources. In this article, a methodology is proposed to distribute the pass gates of a system of on-chip digital LDOs. The distribution of the pass gates considers the location of the load currents to reduce voltage variations across the power grid. The proposed pass gate distribution topology reduces the maximum voltage variations across the grid, on average, by two to three times under nonuniform load distributions.**

***Index Terms*— Digital low-dropout (LDO), on-chip voltage regulator, parasitic resistance, power delivery noise.**

## I. Introduction

IN HIGH-PERFORMANCE, high-complexity integrated systems, power noise is a primary challenge due to the increasing load currents and parasitic interconnect resistances [1]. Furthermore, lower supply voltages have made digital circuits highly sensitive to power noise. In a deeply scaled integrated system (for example, below 28 nm), a noise voltage of a few tens of millivolts can be sufficient to produce a timing failure. The on-chip power delivery network has therefore become a primary concern [2], [3].

To reduce power consumption in high-performance, high-complexity systems, the supply voltage is dynamically changed with respect to workload conditions. Low-dropout (LDO) regulators are typically integrated on-chip to enable fast dynamic voltage scaling [4], [5]. Specifically, digital LDOs are utilized in high-performance systems due to ease of integration under low supply voltages [6].

A digital LDO consists of a digital controller driving multiple pass gates [6]–[9]. A digital LDO controller (typically a bidirectional shift register) receives a control signal from a comparator that compares a reference voltage with the output voltage of the regulator, sampled from the power grid, as shown in Fig. 1 [6]. Depending upon the difference between the reference and grid voltages, the controller either turns on or off a set of pass transistors. The digital LDO includes a digital controller with a dedicated clock signal. A set of pass gates is switched by the active edge of the clock signal.

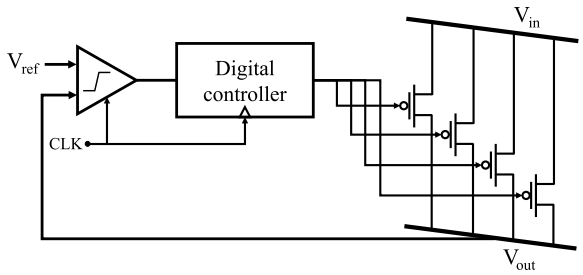


Fig. 1. LDO digital regulator.

To reduce power noise, a low parasitic resistance between the pass gates and the load is desirable. The parasitic resistance can be reduced by either decreasing the distance between the pass gates and the load or by utilizing the low resistance, upper metal interconnects. In practice, the upper metal layers are limited and shared among the clock distribution network, input power grid, and global signals [4]. Due to these limited metal resources, the higher resistance, lower metal layers are often used to route the pass gates to the loads. As a result, the pass gates need to be placed close to the loads [4]. In this article, a methodology to distribute the pass gates of a digital LDO to reduce IR drops across a power grid is proposed. Based on the load distribution, a centroid that represents the region of a grid with the largest current demand is introduced. These grid centroids are used to determine the location of the pass gates.

In Section II, the proposed pass gate distribution methodology is described. In Section III, an analysis of power noise is provided. The proposed methodology is also compared with other conventional distribution techniques. In Section IV, some conclusions are offered.

## II. Distributed Pass Gates

A digital LDO compares a reference voltage with a voltage sampled from a single node within a power grid, as shown in Fig. 2. The digital LDO produces a local output voltage at the sampled node when the sampled voltage is similar to the reference voltage. A small portion of the power grid is,

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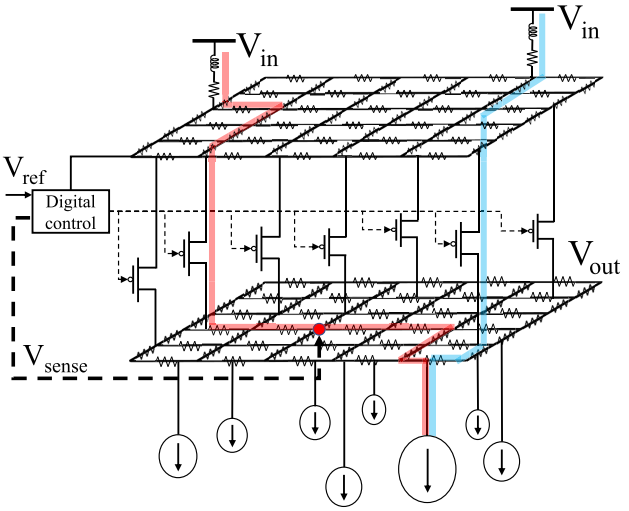


Fig. 2. Distributed set of pass gates integrated with an input and output power delivery grid.

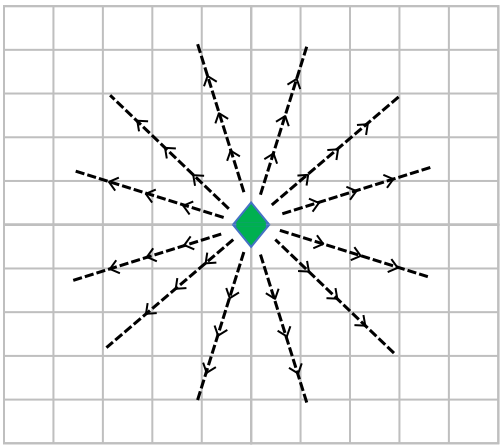

Fig. 3. Pass gates located at the centroid of a grid to source the distributed load currents.

therefore, actively regulated, yielding voltage variations across the power delivery network due to the parasitic resistances. One approach to enlarge the regulated portion of a power grid is distributing multiple LDOs and sampling multiple voltages across the grid [10]. This approach, however, requires additional area and reduces energy efficiency due to larger quiescent currents. Furthermore, multiple LDOs can decrease the stability of a power grid [11], [12]. To maintain a regulated voltage across the power grid using a single digital LDO, the IR drops need to be low. To reduce the IR drops, the proposed digital LDO methodology switches on the pass gates at the centroid of the power delivery network, as shown in Fig. 3. In the case of a single centroid, the current is injected into the grid from the node where the centroid is located. In Section II-A, the centroid of a grid is described. A heuristic-based algorithm to estimate the centroid is provided in Section II-B.

### A. Grid Centroid

The centroid of a grid is the location within a power grid that minimizes the maximum IR drop when connected to either

**Algorithm 1** Calculate $(x_{\text{cent}}, y_{\text{cent}})$

**INPUT:** Set of $n$ current loads and coordinates
**OUTPUT:** Centroid coordinates
$I_{cent} \leftarrow I_1$ ▷ Initialize centroid
$(x_{cent}, y_{cent}) \leftarrow (x_1, y_1)$
**for all** i = 2 to n **do**
  $I_1 \leftarrow I_{cent}$
  $I_2 \leftarrow I_i$
  $(x_1, y_1) \leftarrow (x_{cent}, y_{cent})$
  $(x_2, y_2) \leftarrow (x_i, y_i)$
  $I_{cent} \leftarrow I_1 + I_2$ ▷ Update centroid
  $(x_{cent}, y_{cent}) \leftarrow \Big(x_1 + ((x_2 - x_1)I_2/I_1 + I_2), y_1 + ((y_2 - y_1)I_2/I_1 + I_2)\Big)$
**return** $(x_{cent}, y_{cent})$

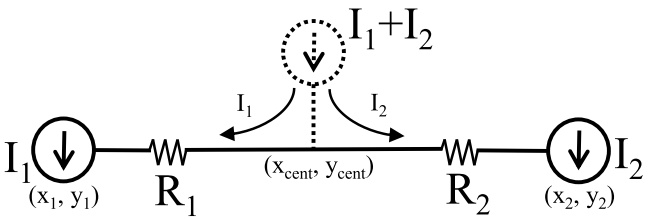


Fig. 4. Centroid of two load currents.

a voltage or current source. Consider a network consisting of two current loads, as shown in Fig. 4. The centroid between these two current sources, $I_1$ and $I_2$, is located to ensure that if connected to a current source, the maximum voltage drop is minimized. To minimize the maximum IR drop, the centroid is placed between two loads to ensure that $I_1\ R_1 = I_2\ R_2$, where $R_1$ is the resistance between $I_1$ and the centroid, and $R_2$ is the resistance between $I_2$ and the centroid.

Suppose $I_1$ and $I_2$ are located within a grid structured power network. The location of the centroid between two current sources is

$$\left(x_1 + \frac{(x_2 - x_1)I_2}{I_1 + I_2}, y_1 + \frac{(y_2 - y_1)I_2}{I_1 + I_2}\right) \tag{1}$$

where $(x_1, y_1)$ and $(x_2, y_2)$ are, respectively, the location of current sources $I_1$ and $I_2$ on the grid. The resistance between two nodes, $(x_1, y_1)$ and $(x_2, y_2)$, is assumed to be proportional to the Manhattan distance between these nodes.[1] Note that the grid centroid gravitates toward the load requiring higher current.

### B. Proposed Algorithm

To estimate the centroid of a grid consisting of multiple current sources, an iterative approach is considered here. Pseudocode for estimating the centroid is shown in Algorithm 1. The runtime for determining the centroid of $n$ current loads is $O(n-1)$. During each step of the iteration, a new centroid between the old centroid and a load

[1]The Manhattan distance between $(x_1, y_1)$ and $(x_2, y_2)$ is $|x_1 - x_2| + |y_1 - y_2|$.

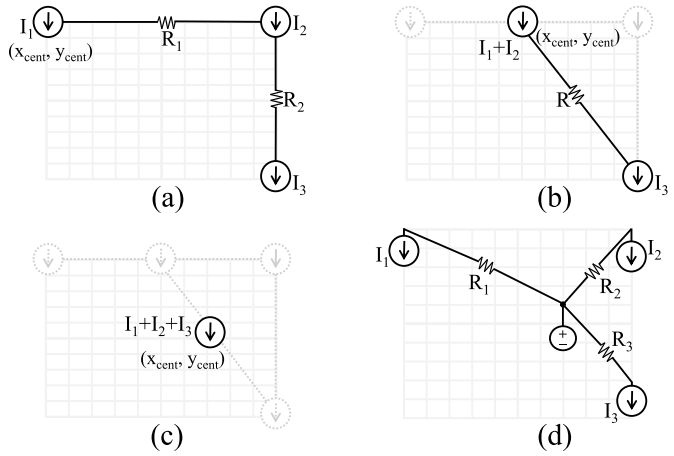


Fig. 5. Iterative process for determining the centroid of three load currents. (a) Centroid is initially assigned to load current $I_1$. (b) New centroid between $I_1$ and $I_2$ is determined and replaces the old centroid. (c) New centroid is determined between the current centroid and $I_3$, replacing the old centroid. (d) Final centroid is replaced by a source connected to the load currents.

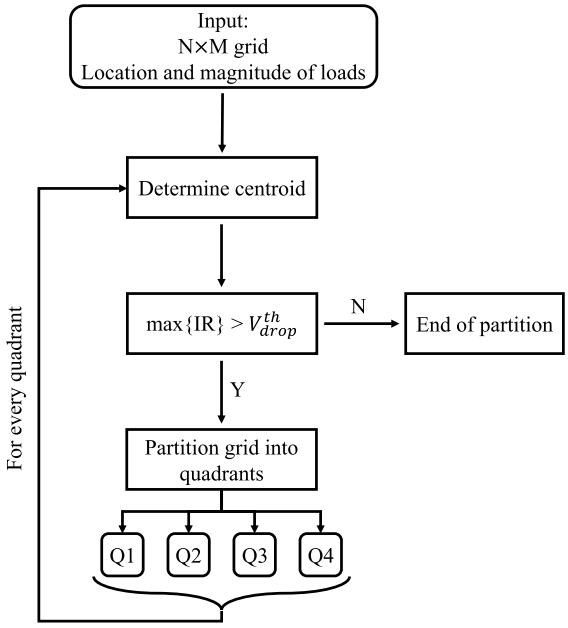


Fig. 6. Recursive process to determine multiple centroids.

current is determined based on (1). This iterative process is illustrated in Fig. 5. The algorithm places the centroid closer to those regions loaded with a higher current to minimize the maximum IR drop. Alternatively, the centroid of $n$ load currents can be determined using

$$(x_{\text{cent}}, y_{\text{cent}}) = \left( \frac{\sum_{i=1}^{n} x_i I_i}{\sum_{j=1}^{n} I_j}, \frac{\sum_{i=1}^{n} y_i I_i}{\sum_{j=1}^{n} I_j} \right). \tag{2}$$

Note that (2), produced by Algorithm 1 considering the centroid as described by (1), is identical to the center of mass for discrete mass points in two dimensions [13], where the mass is replaced by the magnitude of the load currents.

To reduce the IR drops across the grid, the pass gates are placed at the centroid of the grid (see Fig. 3). If the maximum

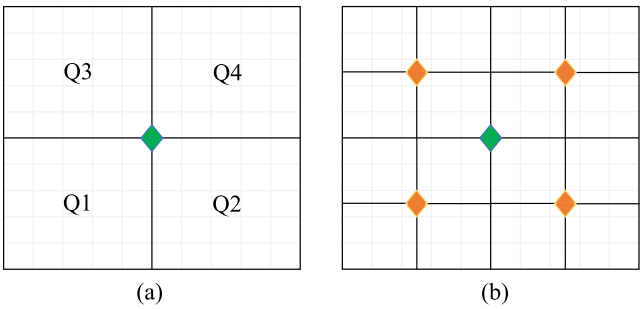


Fig. 7. Iterative process for determining the location of the quadrant centroids. (a) Power grid divided into four quadrants. (b) Centroid placed within each quadrant. A diamond represents an individual centroid.

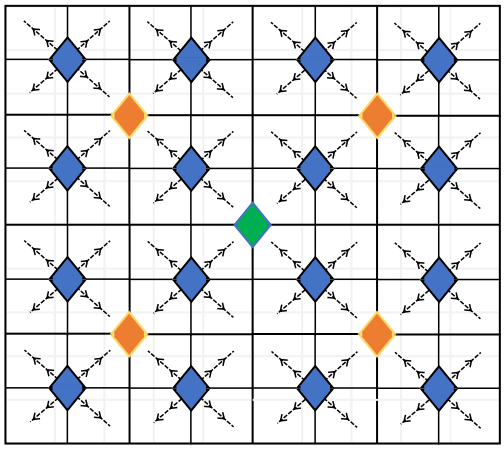

Fig. 8. Power grid composed of 16 regions with separate centroids under a uniform load distribution.

IR drop is greater than a critical threshold $V_{\text{drop}}^{\text{th}}$ (which depends upon the technology node), the grid is partitioned into quadrants to support distributed centroids. The steps describing the partitioning process are shown in Fig. 6. For example, a power grid divided into four different quadrants, each with a unique centroid, is illustrated in Fig. 7(a). A centroid is determined within each quadrant using the procedure outlined in Algorithm 1, as shown in Fig. 7(b). The grid can be further divided into finer granularity by breaking each quadrant into an additional four quadrants, leading to 16 regions. The pass gates are placed at these quadrant centroids to distribute the current across the grid, as shown in Fig. 8. A power grid consisting of $Q$ centroids and a digital LDO with an $N$-bit bidirectional shift register embodies $Q \times N$ pass gates. A set of $Q$ pass gates is turned on at the active edge of the clock signal of the digital LDO, each located at a different centroid within the $Q$ quadrants. The pass gates are sized in proportion to the current demand within the specific centroid to reduce the amplitude of any limit cycle oscillations [14].[2] In Section III, the proposed digital LDO placement methodology is compared with conventional placement methodologies.

[2]The width of the pass gates are sized in proportion to $(I_{\text{quad}}/I_{\max}/\text{QuadNo})$, where $I_{\text{quad}}$ is the total current within a specific quadrant, $I_{\max}$ is the maximum load current of the digital LDO, and QuadNo is the total number of quadrants

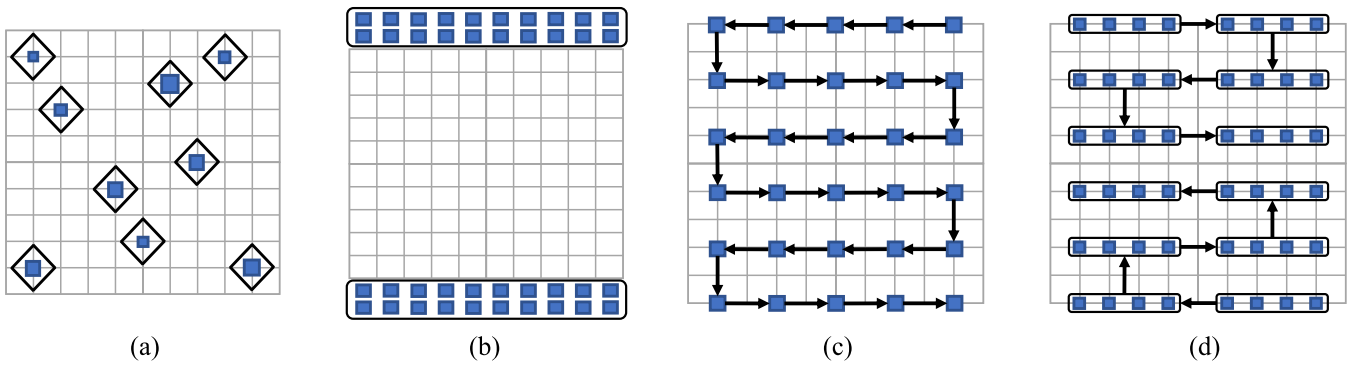


Fig. 9. Different pass gate distribution topologies. (a) Proposed centroid-based distribution topology where the pass gates are sized according to the maximum load current. (b) Top–bottom topology [15], [16]. (c) Daisy chain topology [17]. (d) Distribution topology from [4].

## III. Power Grid Analysis

The proposed pass gate distribution topology is compared with three different distribution topologies. These distribution topologies are introduced in Section III-A. An analysis of the power grid and a comparison of different distribution topologies are explored in Section III-B.

### A. Distribution Topologies

Three different pass gate distribution topologies have been considered: top–bottom, daisy chain, and the distribution topology described in [4], as shown in Fig. 9. In the top–bottom topology [see Fig. 9(b)], the pass gates are clustered in the upper and lower sections of the power grid. The low resistance, upper metal layers distribute the current from the top and bottom portions of the grid to the loads, ensuring low IR drops. This technique is prohibitive in those cases where the upper metal layers are largely used by the clock distribution network, global signals, and input portion of the power distribution network [4]. Alternatively, the daisy chain topology is typically considered in power gating schemes. Since the pass gates used for power gating are also used for the digital LDOs [18], the daisy chain distribution is considered here. In this configuration, the pass gates are serially turned on to reduce the transient current: $C(dV/dt)$ current, where $C$ is the power grid capacitance [see Fig. 9(c)]. The propagation delay between the two ends of the chain prevents the pass gates from simultaneously turning on, limiting the $C(dV/dt)$ current. The topology illustrated in Fig. 9(d) has recently been proposed to distribute the pass gates of a digital LDO [4]. Similar to the daisy chain topology, a clustered group of pass gates is switched in a serial fashion at the active edge of the clock signal. Two clusters switch from the top and bottom sections of the grid toward the center of the grid.

### B. Comparison of Pass Gate Distribution Topologies

In this section, the proposed distribution topology is compared with the topologies described in Section III-A. A power analysis is conducted considering a $32 \times 32$ output grid with a 1-$\Omega$ resistance between the adjacent grid nodes. The resistance of the input and ground grids is assumed to be negligible (due to the low resistance, upper metal layers, and large number of

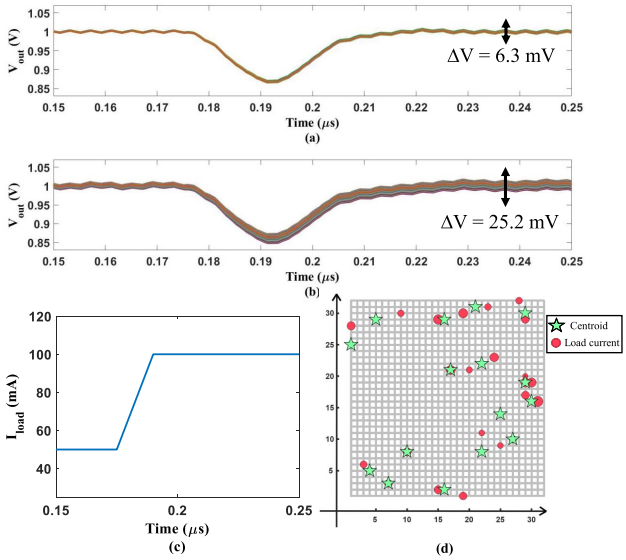


Fig. 10. Transient response to a variation in load at the output of a digital LDO. (a) Proposed centroid-based distribution topology. (b) Top–bottom distribution topology. (c) Total transient load current. (d) Location of the centroids as well as the distribution of load currents. The size of the circles is proportional to the magnitude of the local load current.

distributed C4 power connections). The input voltage is 1.2 V, and the output voltage is 1 V. A total current load of 150 mA is assumed. The total size of the pass gates is set according to the total current load and is maintained equal across all topologies. A digital LDO with two controllers composed of 32-bit bidirectional shift registers is considered to enable both coarse and fine modes of operation for mitigating limit cycle oscillations [14]. In the proposed topology, 16 centroids are considered [see Fig. 8]. The grid voltage is sampled from the primary centroid of the grid (the initial centroid before partitioning) for all of the distribution topologies.

An exemplary transient response of the digital LDO on the output power grid is shown in Fig. 10. The superimposed transient voltage at each node on the power grid illustrates the voltage variations across the grid. If the current traveling across the grid is minimal, the voltages on the power grid remain approximately equal [the voltage curves align, as shown in Fig. 10(a)]. Contrarily, if significant current flows

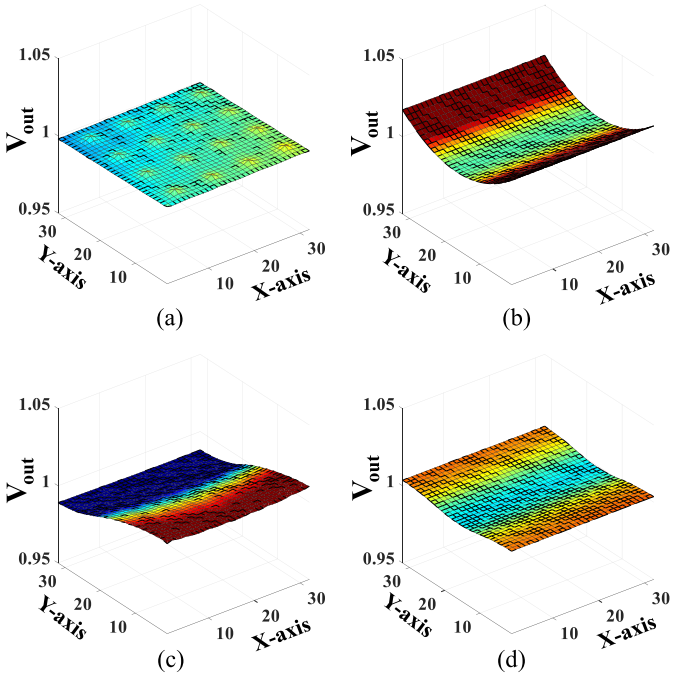


Fig. 11. Power grid assuming a uniform load distribution. (a) Proposed centroid-based distribution topology. (b) Top–bottom topology [15], [16]. (c) Daisy chain topology [17]. (d) Distribution topology from [4].

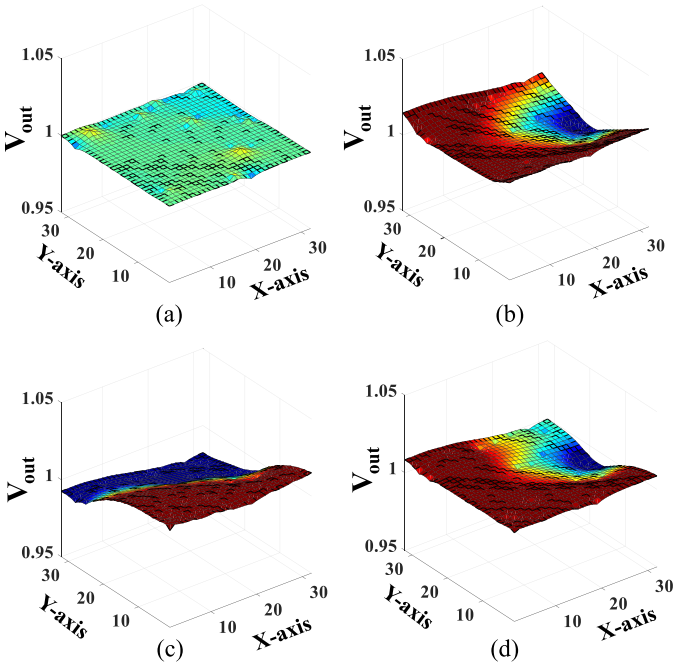


Fig. 12. Power grid considering a nonuniform load distribution. (a) Proposed centroid-based distribution topology. (b) Top–bottom topology [15], [16]. (c) Daisy chain topology [17]. (d) Distribution topology from [4].

through the output power grid (e.g., due to a large distance between the pass gates and load), the voltage across the output power grid varies [see the misaligned voltage curves, as shown in Fig. 10(b)].

A voltage map of the power grid assuming a uniform load distribution is shown in Fig. 11. The output grid voltage is averaged across time to determine the dc voltage (filtering out the limit cycle oscillations). The difference between the maximum and minimum voltages are 5 mV for the proposed distribution topology and the topology described in [4], whereas this difference is 18 and 22 mV for, respectively, the top–bottom and daisy chain topologies.

The daisy chain topology suffers from significant IR drops, on the order of tens of millivolts. Since the grid centroid is at the geometric center of the grid under a uniform load condition, the digital LDO stops turning on additional pass gates once the voltage at the center node is equal to the reference voltage. The pass gates toward the end of the chain, therefore, remain closed, resulting in an unbalanced distribution of pass gates. The current, therefore, flows from the upper portion of the chain toward the lower portion, leading to the voltage degradation shown in Fig. 11(c).

Furthermore, the top–bottom topology also suffers from significant IR drops since the pass gates are not distributed across the power grid. A set of pass gates is simultaneously switched from both clusters within the top and bottom regions of the grid, producing a symmetric voltage map [see Fig. 11(b)]. The current flowing from the upper and lower sections toward the grid center produces a higher voltage at the edge of the grid, forming a valley pattern.

The high IR drop of the top–bottom topology is mitigated using the topology described in [4]. Since the clustered pass gates are distributed and simultaneously controlled from both the upper and lower parts of the grid, the distance the currents travel within the grid is reduced. Under a uniform load condition, both the proposed centroid-based topology and the topology described in [4] significantly eliminate any IR drops.

Under nonuniform load conditions where a portion of the grid is loaded with large currents, the daisy chain, top–bottom, and the topology described in [4] exhibit significantly higher IR drops, as shown in Fig. 12. The difference between the maximum and minimum voltages after reevaluating the centroids is 6.3 mV for the proposed distribution topology, 18.3 mV for the topology described in [4], and 25.2 and 35.2 mV for, respectively, the top–bottom and daisy chain topologies. The distribution topology described in [4], daisy chain, and top–bottom are sensitive to nonuniform load distributions since the location of the pass gates does not consider the location of the load currents. The proposed centroid-based distribution topology, however, determines the regions loaded with the highest currents and places and sizes the pass gates according to the location and current demand of the centroids. A low IR drop across the power grid is, therefore, maintained despite nonuniform load distributions, as shown in Fig. 12(a).

To explore the effects of a nonuniform load distribution on the steady-state voltage variations while considering dynamic loads, a set of Monte Carlo simulations is described, as shown in Fig. 13. The magnitude of the load between each node within the output and ground network is treated as an independent random variable. These random variables are assigned a number sampled from a uniform distribution. Each sample

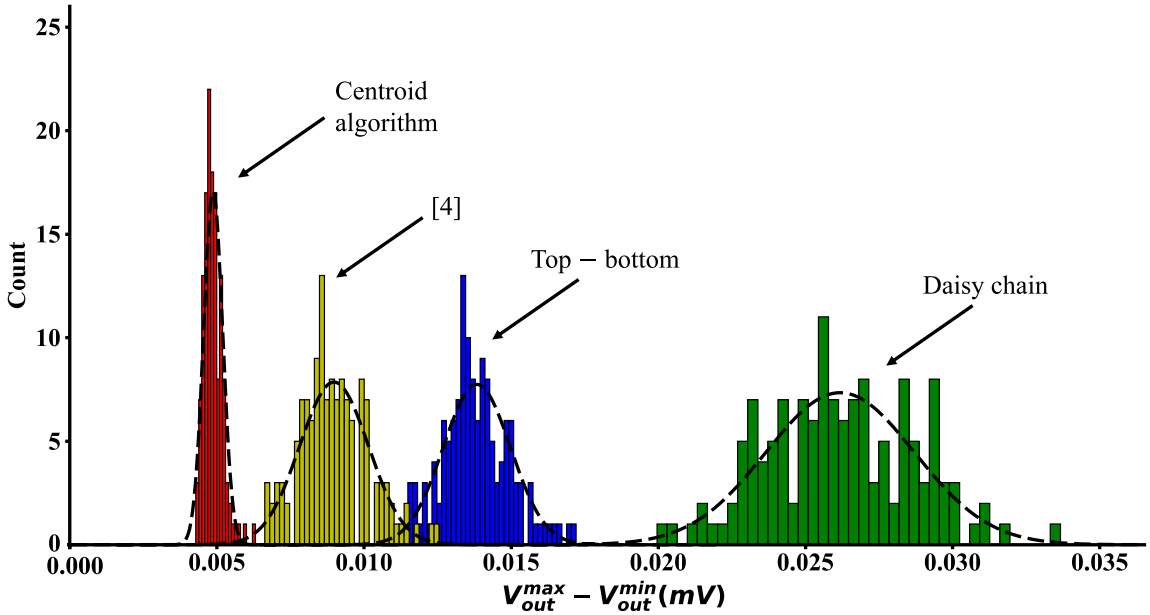


Fig. 13. Monte Carlo simulations depicting the difference between the maximum and minimum voltages across a power grid considering four different pass gate distribution topologies.

TABLE I
MEAN AND VARIANCE OF DISTRIBUTIONS (mV)

| Topologies | Mean | Variance |
|---|---|---|
| Proposed heuristic | 4.87 | 0.32 |
| [4] | 8.97 | 1.17 |
| Top–bottom | 13.8 | 1.14 |
| Daisy chain | 26.1 | 2.52 |

shown in Fig. 13 is the arithmetic mean of 50 samples obtained from a Monte Carlo simulation under a fixed centroid configuration. For each one of the 50 samples, the load currents are varied while satisfying a maximum load condition (i.e., an upper bound defined for each load). The centroids (the location of the pass gates) remain constant for those samples based on this maximum load condition. The total load current is maintained below 150 mA. For each mean of 50 samples, the maximum load condition is reevaluated based on a uniform probability distribution where the centroids are recalculated using the procedure outlined in Algorithm 1. Approximately 7500 simulations are considered, producing in total 150 (7500/50) samples per each distribution, as shown in Fig. 13. Due to the large number of different load distributions, high coverage of possible cases requires significant computational power. Rather, the Gaussian curves are fitted to account for the extrapolation.

The mean and variance of the histograms shown in Fig. 13 are listed in Table I. The voltage variations across the power grid are higher for the topology described in [4], top–bottom, and daisy chain as compared to the proposed distribution topology since these other distribution topologies do not consider the location of the loads. The mean of the differences between the maximum and minimum voltages within the grid increases by 1.8×, 2.8×, and 5.4× for, respectively, the topology described in [4], top–bottom, and daisy chain with respect to the proposed distribution topology. Furthermore, the variance significantly increases for the topology described in [4], top–bottom, and daisy chain. As a result, a large number of cases exist in which these topologies lead to greater voltage variations across the grid under steady-state conditions. In contrast, the proposed centroid-based approach maintains a relatively low variance of less than a millivolt. The proposed pass gate distribution topology is therefore more suitable to ensure lower voltage variations across a power grid.

## IV. CONCLUSIONS

In this article, the effect of different pass gate distribution topologies on a power distribution grid utilizing a digital LDO is evaluated. The concept of a power grid centroid is introduced to determine those regions within a power grid loaded with the highest currents. Based on this centroid approach, a pass gate distribution topology is presented. The proposed topology is compared with three different pass gate distribution topologies. Since the existing topologies do not consider the location of the loads, the voltage variations across the power grid are greater than the proposed topology based on the centroids. Statistical simulations indicate that the voltage variations across a grid significantly increase when using existing distribution topologies under nonuniform load conditions. In contrast, the proposed centroid topology demonstrates significantly lower voltage variations across a grid despite a nonuniform load distribution.

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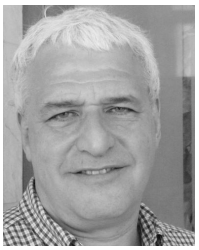

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