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On-Chip Interconnect Noise in High Performance CMOS Integrated Circuits

by

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Submitted in Partial Fulfillment

of the
Requirements for the Degree
Doctor of Philosophy

Supervised by

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Man is still the most extraordinary computer in the world.

– John F. Kennedy

Dedication

This work is dedicated to my parents, my sister, and her family.

Curriculum Vitae

The author was born in China on June 11, 1968. He attended Tsinghua University, Beijing, China from 1986 to 1991 and graduated with a Bachelor of Engineering degree in Electrical Engineering. From 1991 to 1994, he worked as a design/process engineer in the Institute of Microelectronics, Tsinghua University, Beijing, China. He received his Master of Engineering degree in the School of Electrical and Electronic Engineering from the Nanyang Technological University, Singapore in 1996. He came to the University of Rochester in the fall of 1996. In 1998, he received his Master of Science degree in Electrical and Computer Engineering. He has pursued research in high performance CMOS integrated circuits under the direction of Professor Eby G. Friedman from 1998 to 2000 in the areas of on-chip interconnect noise, signal integrity, and related performance issues in very deep submicrometer CMOS integrated circuits.

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The unforgettable memory and experience that I have had at the University of Rochester will greatly enrich the rest of my life. I am extremely grateful to all those who have given me invaluable help and support over the past four years.

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Abstract

As modern CMOS integrated circuit (IC) technology moves into the very deep submicrometer (VDSM) regime, millions of transistors operating at frequencies greater than a gigahertz will be integrated onto a single IC. Serious on-chip electrical problems, including signal distortion along coupled interconnect lines and voltage fluctuations in the power distribution network, are being encountered in these high speed, VDSM high complexity integrated circuits. This on-chip interconnect noise increases the design cost as well as the design time. Moreover, the noise also causes circuit malfunctions and long term reliability issues. On-chip interconnect noise has therefore become one of the primary threats to continued growth in integration density and circuit performance. In order to ameliorate these design challenges in VDSM integrated circuits, design for signal integrity (DSI) strategies need to be incorporated into existing design methodologies and related design automation tools

The first comprehensive research on on-chip interconnect noise in CMOS integrated circuits is presented in this dissertation. The primary objective of the research is to develop a capability for enhancing signal integrity in high performance CMOS integrated circuits. This objective has been satisfied by considering design issues in terms of the interconnect impedance models, coupled on-chip in-

terconnect, and voltage fluctuations in power distribution networks, permitting the effects of the interconnect impedances, coupling noise, and delay uncertainty to be predicted at the system level in order to improve overall circuit performance. The accuracy of the developed propagation delay model is within 7% for a resistive load and 11% for an inductive load as compared to SPICE. The error of the estimated peak coupling noise voltage is within 7% and 13% of SPICE for a two-line and three-line coupled system, respectively. The predicted peak transient *IR* voltage drops and on-chip simultaneous switching noise voltage are within 6% and 10%, respectively, as compared to SPICE. The research presented in this dissertation has provided a capability for estimating on-chip interconnect noise at the system (or IC) level, permitting interconnect-based design strategies and related design methodologies to be developed.

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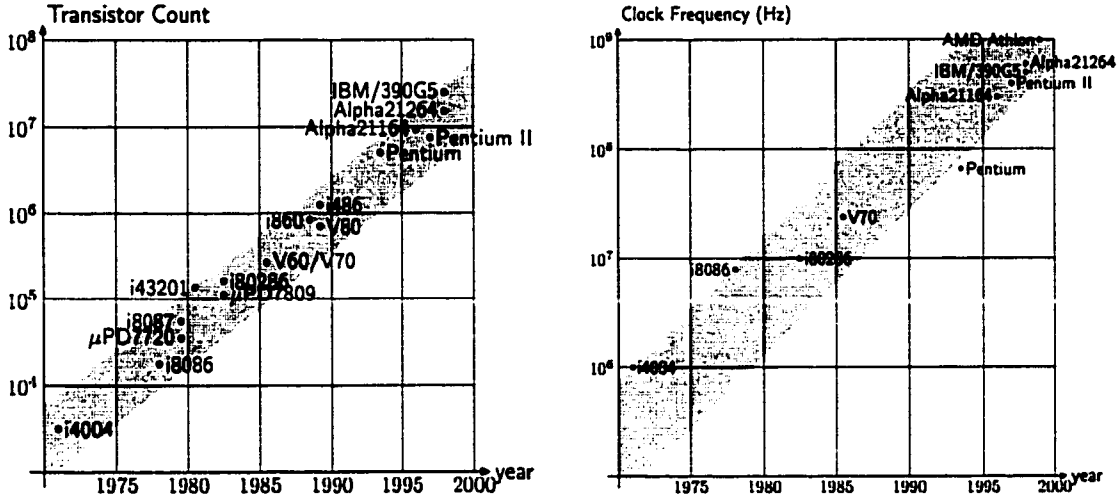
Chapter 1

Introduction

The performance of CMOS integrated circuits (ICs) has been increasing exponentially due to the scaling of on-chip devices and interconnections along with new IC architectures and design methodologies [1, 2], as graphically illustrated in Figure 1.1. Today, a single IC can contain an entire system [the concept of a system-on-a-chip (SOC)] and the structure of on-chip interconnections has become more like those of multi-chip modules (MCMs) and printed circuit boards (PCBs) with many interleaved signal layers and multiple planes of interconnections [3–6].

As the feature size of on-chip devices and interconnections scales down to very deep submicrometer (VDSM) dimensions (less than 0.25 μm), the size of an integrated circuit has also increased and the operating frequencies now exceed a gigahertz [1, 7–13]. For high performance CMOS integrated circuits, on-chip clock frequencies are expected to increase from 750 MHz in 1999 to 10 GHz by 2012 and the chip size of microprocessors will increase from 300 mm^2 to 700 mm^2, according to the SIA (Semiconductor Industry Association) International Technology Roadmap for Semiconductors (ITRS) as illustrated in Table 1.1. The speed of these highly scaled integrated circuits is now dominated by interconnect impedances rather than the characteristics of the transistors with a CMOS logic



(a) Evolution of the number of transistors per integrated circuit

(b) Evolution of clock frequency of high performance microprocessors

Figure 1.1: *Moore's law* - exponential increase in circuit integration density and operating clock frequency

Table 1.1: Roadmap characteristics of CMOS technology

Year of First Product Shipment	1997	1999	2001	2003	2006	2009	2012
Feature Size (nm)							
Dense Lines (DRAM half pitch)	250	180	150	130	100	70	50
Isolated Lines (MPU gates)	200	140	120	100	70	50	35
Density (transistors/cm^2)							
high volume MPU (million)	3.7	6.2	10	18	39	84	180
low volume ASIC (million)	8.0	14	16	24	40	64	100
Clock Frequency (MHz)							
On-chip-local high performance	750	1,250	1,500	2,100	3,500	6,000	10,000
Chip Size (mm^2)							
DRAM	280	400	445	560	790	1120	1580
MPU	300	340	385	430	520	620	750
ASIC	480	800	850	900	1000	1100	1300
Supply Voltage V_{dd} (V)	1.8-2.5	1.5-1.8	1.2-1.5	1.2-1.5	0.9-1.2	0.6-0.9	0.5-0.6
Power (W)							
High performance with heatsink	70	90	110	130	160	170	175
Battery handled	1.2	1.4	1.7	2.0	2.4	2.8	3.2

gate [1, 14–16], as shown in Figure 1.2 [1]. The emergence of copper interconnect and low κ dielectric materials has only delayed this issue rather than solve the interconnect problem. Furthermore, up to 30% of the dynamic power is consumed by the global interconnect network [17], as listed in Table 1.2 for different generations of the Alpha microprocessors [17–20].

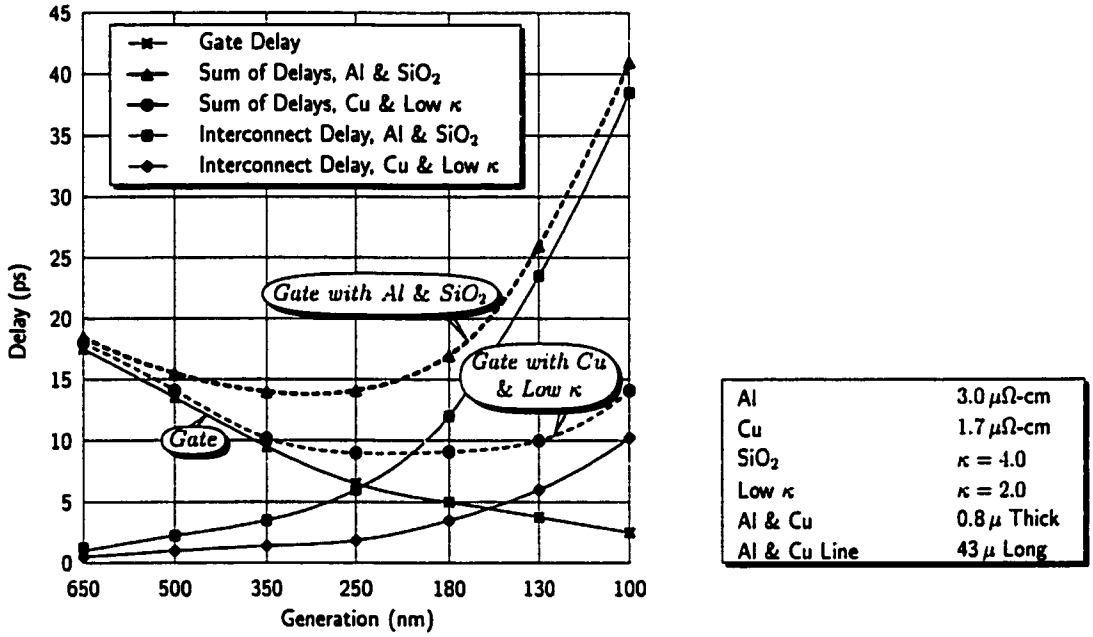


Figure 1.2: Gate and interconnect delay versus technology generation [1]. The interconnect delay dominates the logic gate delay for both aluminum and copper metalization as the feature size decreases.

In addition to interconnect delay and power dissipation, serious on-chip electrical problems are being encountered in these high speed, VDSM high complexity integrated circuits [15, 21–25]. These problems include signal distortion along coupled interconnect lines, the degradation of signal quality due to the parasitic interconnect resistance, capacitance, and inductance, and voltage fluctuations in the power distribution network, each of which are major sources of on-chip interconnect noise in high performance VDSM CMOS integrated circuits [26–30].

One major advantage of CMOS digital circuits in a noisy environment is that CMOS logic gates have a relatively high immunity to noise disturbances [31–33]. However, as power supply levels decrease (as listed in Table 1.1), this advantage has diminished [34]. Therefore, the problem of noise has increased in importance such that on-chip interconnect noise has become one of the primary threats to the continued growth in integration density and circuit performance [35, 36].

Table 1.2: Technology and performance characteristics of DEC/Compaq Alpha microprocessors

Generation	21064 (I)	21164 (II)	21264 (III)
Year	1993-1994	1995-1996	1997-1998
Feature size (μm)	0.75	0.5	0.35
Transistors (million)	1.68	9.3	15.2
Die size (mm^2)	16.8x13.9	18.1x16.5	16.7x18.8
Frequency (MHz)	200	300	600
Capacitive load of the clock distribution network (nF)	3.25	3.75	—
Power supply (V)	3.3	3.3	2.2
Supply current (A)	< 10	~ 15	> 30
Total Power (W)	~ 30	~ 50	~ 72
Percentage of total power dissipated on the clock distribution network	40%	40%	44%

In the design of high performance CMOS integrated circuits, it is of fundamental importance to be able to predict the effects of on-chip interconnect noise at the system (or IC) level [37–40]. This capability permits the development of design techniques that avoid circuit malfunctions or additional power dissipation caused by on-chip interconnect noise. The design cycle and cost can therefore be reduced, as well as signal integrity and circuit reliability improved.

A physically oriented approach is presented in this dissertation to minimize or solve the problems of on-chip interconnect noise. The VDSM MOS transistors are characterized by an empirical short-channel device model - the nth power

model [41] or the effective output resistance depending upon the specific tradeoff between circuit complexity and computational efficiency. On-chip interconnect lines are characterized by capacitive, resistive, and/or inductive models depending upon the specific input, drive, and load conditions. The interconnect capacitance, resistance, and inductance can be characterized by classical geometric layout parameters. Analytical expressions describing the timing properties, voltages, and currents are developed based on the device and interconnect parameters, providing concise and physically intuitive expressions for the voltage waveform, propagation delay, power dissipation, and noise characteristics of on-chip interconnect networks. The expressions are used to develop useful design techniques and methodologies applicable to VDSM high performance integrated circuits.

The primary objective of this dissertation is to investigate and develop strategies to improve signal integrity in high speed VDSM CMOS integrated circuits, incorporating noise information into the design flow of integrated circuits. This objective is satisfied by considering signal integrity design issues in terms of the interconnect impedance models, on-chip crosstalk, delay uncertainty of a CMOS logic gate due to coupled interconnect, and voltage fluctuations in the power distribution network, thereby providing the capability for predicting the effects of on-chip interconnect noise at the system level. The specific objectives are to

- develop enhanced circuit models to characterize the electrical and physical attributes of on-chip interconnect parasitic impedances

- develop analytical expressions to characterize the waveform shape of the output voltage, the propagation delay, and the transient power dissipation of a CMOS logic gate driving resistive, capacitive, and inductive interconnect

- develop an analytical model to characterize the effective load capacitance, delay uncertainty, and coupling noise caused by capacitively coupled on-chip interconnections due to changing signal activity
- develop analytical expressions to estimate transient *IR* voltage drops and on-chip simultaneous switching noise within the power distribution network
- estimate the effects of noise at the system level based on the aforementioned analytical equations and determine circuit- and layout-level design constraints to avoid circuit failure and power dissipation caused by on-chip interconnect noise
- provide guidelines for repeater insertion, interconnect routing, and the proper design of the power distribution network
- develop design techniques to improve signal integrity and minimizing delay uncertainty in the design of high speed CMOS integrated circuits

Conventional scaling theory of CMOS technology is presented in Chapter 2. The nth power law device model, which is accurate in both the linear and saturation regions, is also introduced to characterize the short-channel MOS transistors. Other topics such as on-chip parasitic inductance, a variety of interconnect models, and noise margins in CMOS logic gates are also discussed. Signal integrity and design for noise (DFN) issues in VDSM integrated circuits are emphasized throughout Chapter 2.

A Fourier analysis of typical on-chip signals is presented in Chapter 3. An on-chip signal can be approximated by a Fourier series. The effect of distributed interconnect on the waveform shape of an on-chip signal can be characterized by

an effective load impedance, which includes the frequency dependence of the interconnect impedances. The effective load impedance model presented in Chapter 3 is based on the input transition time and the distributed characteristics of the on-chip interconnections.

Analytical expressions characterizing the output voltage, propagation delay, and transient power dissipation of a CMOS logic gate driving a resistive-capacitive interconnect line are presented in Chapter 4. The interconnect is modeled as a lumped *RC* load in order to emphasize the nonlinear behavior of a CMOS logic gate. Analytical expressions describing the output voltage are based on a fast ramp input signal. The propagation delay of a CMOS logic gate is characterized for both a fast ramp and slow ramp input signal. Analytical expressions characterizing both the short-circuit power and resistive power consumption are also presented based on the input transition time and load conditions. The signal quality is degraded by the interconnect resistance, causing additional short-circuit power to be dissipated within the following logic stage.

The effects of on-chip inductance on the waveform shape of the output voltage, propagation delay, and short-circuit power of a CMOS logic gate are presented in Chapter 5. The interconnect is modeled as a lumped *RLC* impedance to emphasize the effect of the on-chip interconnect inductance on the behavior of a CMOS logic gate. Analytical equations characterizing the output voltage are derived based on an assumption of a fast ramp input signal. The propagation delay of a CMOS logic gate is derived for both fast ramp and slow ramp input signals. Large inductive loads and fast input transition times can result in significant short-circuit current within the driver stage. Closed form expressions of the short-circuit power are also presented based on the input transition time and load impedance.

An analysis of two capacitively coupled CMOS logic gates based on the signal activity is presented in Chapter 6. The uncertainty of the effective load capacitance on the propagation delay due to the signal activity is addressed. Analytical expressions characterizing the coupling noise voltage on a quiet interconnect line are also considered in Chapter 6. The transistors within a coupled system must be carefully sized to balance the load capacitances in order to reduce any delay uncertainty caused by the coupling capacitance.

A transient analysis of CMOS logic gates driving coupled resistive-capacitive interconnect is presented in Chapter 7. Analytical expressions characterizing the output voltage of each CMOS logic gate are developed for a two-line and a three-line coupled system. Specific circuit techniques to minimize the effects of coupling capacitances are also described in Chapter 7.

Interconnect between a CMOS driver and receiver can be modeled as a lossy transmission line in high speed CMOS integrated circuits as signal transition times become comparable to or less than the time of flight delay of the signal propagating through a low resistivity interconnect line. In Chapter 8, closed form expressions for the coupling noise between adjacent interconnect lines are presented to estimate the coupling noise voltage on a quiet line. Design guidelines to determined the driver impedance are also discussed in terms of the propagation delay of the driver stage, the relaxation time of the coupling noise voltage, and the peak noise at both ends of the quiet line.

Due to the lossy characteristics of the metal interconnections in CMOS integrated circuits, transient IR voltage drops within the power distribution network, which are caused by large on-chip current and occur during logic transitions in a synchronous CMOS integrated circuit, are no longer negligible. An analysis of

transient *IR* voltage drops is presented in Chapter 9. Circuit- and layout-level design constraints are also addressed to manage the maximum *IR* voltage drops. The delay uncertainty of a CMOS logic gate due to transient *IR* voltage drops within the power distribution network is also addressed in Chapter 9.

Simultaneous switching noise (SSN) has become an important issue in the design of on-chip power distribution networks in high speed CMOS integrated circuits. An inductive model is used in Chapter 10 to characterize the power distribution network when a transient current is generated by the simultaneous switching of on-chip registers and logic gates in a synchronous CMOS integrated circuit. An analytical expression of the simultaneous switching noise voltage is presented based on a lumped *RLC* model to characterize the transient behavior of the power supply current. Design constraints at both the circuit and layout levels are also discussed based on minimizing the effects of the peak on-chip simultaneous switching noise. The delay uncertainty of a CMOS logic gate due to on-chip simultaneous switching noise voltages is also presented in Chapter 10.

Specific conclusions derived from the research described in this dissertation are provided in Chapter 11. Extended future research topics to improve on-chip signal integrity, incorporate interconnect noise into a high performance IC design flow, and reduce design costs are discussed in Chapter 12.

Chapter 2

Challenges in the Design of Deep Submicrometer CMOS Integrated Circuits

IC design productivity now lags far behind the complexity growth rate provided by existing technology manufacturing capabilities. Technology scaling has provided the level of transistor packing density per unit area outpacing design utilization at an exponential rate. The complexity growth rate (density) is about 58% per year, while the design productivity growth rate (utilization) is about 21% per year, as shown in Figure 2.1 [25]. To deal effectively with the "design gap," new design disciplines and methodologies will be required over the next decade, in which physical design will become a pivotal issue in the hierarchical design process.

The National Technology Roadmap for Semiconductors (NTRS) predicts that one of five design challenges before 2006 is the modeling of interconnect and power structures for synthesis/system level design. Furthermore, signal integrity will be a major design challenge after 2006 as listed in Table 2.1 [1]. Identifying and addressing these design issues, such as the effects of technology scaling, the interconnect impedance and models, on-chip interconnect noise, and the de-

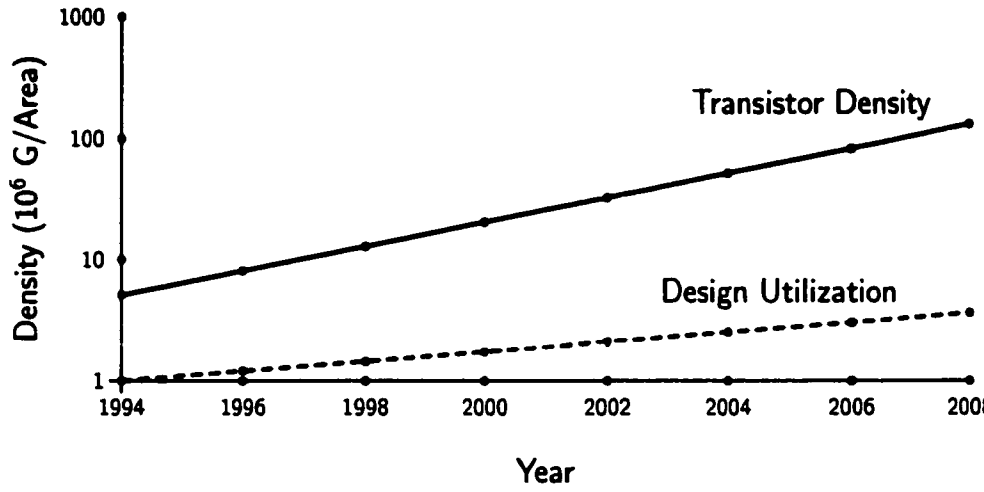


Figure 2.1: Gap between design productivity and semiconductor manufacturing capability

sign of global distribution networks in deep submicrometer integrated circuits at the system level will significantly enhance the goal of achieving parity between technological manufacturing and design productivity.

In this chapter, technology scaling of CMOS integrated circuits is reviewed in Section 2.1. On-chip interconnect inductance is described in Section 2.2. A variety of interconnect models are summarized in Section 2.3. A compact, empirical device model of short-channel MOS transistors is introduced in Section 2.4. Noise margins of CMOS logic gates and the issue of signal integrity in VDSM integrated circuits are discussed in Sections 2.5 and 2.6, respectively.

2.1 Scaling of CMOS Technology

In the development of next generation CMOS integrated circuit technologies, there has been a common established rule for scaling - if the device dimensions are reduced by about 2/3, the chip size increases by 1.5 times, and the number of transistors in an integrated circuit increases by a factor of four. This process

Table 2.1: Interconnect related issues in the next decade

CHALLENGES $\geq$ 100 nm / BEFORE 2006	*SUMMARY OF ISSUES*
More accurate interconnect model and power models for synthesis/system level design	Modeling methodology defining guidelines for model development for different system components
Constraint-dominated interconnect synthesis	Gigascale designs will be dominated by interconnect Automatic synthesis and optimization of N-layer interconnects for performance
CHALLENGES $\leq$ 100 nm / BEYOND 2006	*SUMMARY OF ISSUES*
Architectural and other design methods to overcome fatal interconnect performance methods	Limitations of material (copper/low κ) to overcome interconnect problem associated with high performance ICS
Signal integrity and IC reliability	Noise, interconnect, and reliability related issues

occurs almost every three years in accordance with *Moore's law* [2], which has held true for more than 20 years.

2.1.1 Scaling of MOS Transistors

Minimizing MOS transistor dimensions has been and continues to be a popular method to improve circuit speed and integration density. Ideal scaling theory, which is one of the fundamental approaches to shrinking MOS transistors, is used in this chapter to demonstrate the effects of technology scaling. The MOS transistors are scaled in five dimensions - the three physical dimensions, the voltage supply level, and the doping concentration to maintain a constant electric field within the conducting channel. The basic MOSFET structure is shown in Figure 2.2.

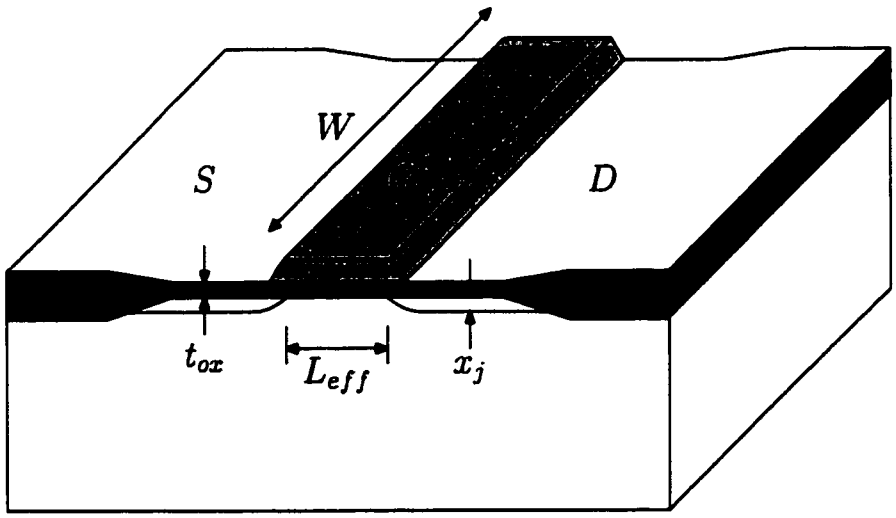


Figure 2.2: Physical dimensions of a MOS transistor

The ideal scaling of MOS transistors is listed in Table 2.2, where S ($S > 1$) is the scaling factor. All geometric dimensions of a MOS transistor (W, L_{eff}, t_{ox}, x_j) are decreased by $1/S$. The substrate doping concentration (N_{sub}) is increased by

S, and all voltages (V_{dd}, V_{TN}, V_{TP}) are reduced by $1/S$. Therefore, the internal electric field remains unchanged.

Table 2.2: Ideal scaling of MOS transistors

Parameters	Scaling Factor
Dimensions (W,L, t_{ox}, x_j)	$1/S$
Substrate doping (N_{sub})	S
Voltage (V_{dd}, V_{TN}, V_{TP})	$1/S$
Current per device (I_{DS})	$1/S$
Gate Capacitance ($C_g = \epsilon_{ox}\frac{WL}{t_{ox}}$)	$1/S$
Transistor on-resistance ($R_{tr} \propto \frac{V_{DS}}{I_{DS}}$)	1
Intrinsic gate delay ($\tau_g = \frac{C_g \Delta V}{I_{av}}$)	$1/S$
Power-dissipation per gate ($P = IV$)	$1/S^2$
Power-delay product per gate ($P\tau_g$)	$1/S^3$
Area per device ($A = WL$)	$1/S^2$
Power-dissipation density (P/A)	1

As a result, with ideal scaling, devices become faster, the power-delay product and the power dissipation of the devices are decreased, the integration density is increased, while the power-dissipation density remains constant. High speed, high density integrated circuits are therefore possible; both the speed and functionality of integrated circuits are improved without increasing the power dissipation density.

However, the silicon bandgap and built-in junction potentials impose a limit to ideal scaling. Furthermore, several second-order effects are caused by shrinking the MOS transistor structure, such as mobility degradation and velocity saturation, which degrade the performance of the MOS transistors. Moreover, a long channel device model can no long be used to approximate the I-V characteristics of a MOS transistor due to a variety of short-channel effects [42].

2.1.2 Scaling of On-Chip Interconnect

The parasitic interconnect capacitance and resistance can be determined by the physical geometric parameters of an interconnect line, *i.e.*, W_{int}, H_{int}, S_{int}, t_{in}, and l_{int}. These interconnect dimensions are illustrated in Figure 2.3. W_{int} is the width, H_{int} is the thickness, and l_{int} is the length of the interconnect line. S_{int} is the spacing between adjacent interconnect lines. t_{in} is the thickness of the insulation layer. The parasitic capacitance per unit length of a single interconnect line is [15]

$$C_{int} = \epsilon_{ox}\left[\frac{W_{int}}{t_{in}} - \frac{H_{int}}{2t_{in}} + \frac{2\pi}{ln[1+\frac{2t_{in}}{H_{int}}(1+\sqrt{(1+\frac{H_{int}}{t_{in}})})]}\right]. \tag{2.1}$$

The interconnect resistance per unit length is

$$R_{int} = \frac{\rho}{W_{int}H_{int}}, \tag{2.2}$$

where ρ is the resistivity of the metal line.

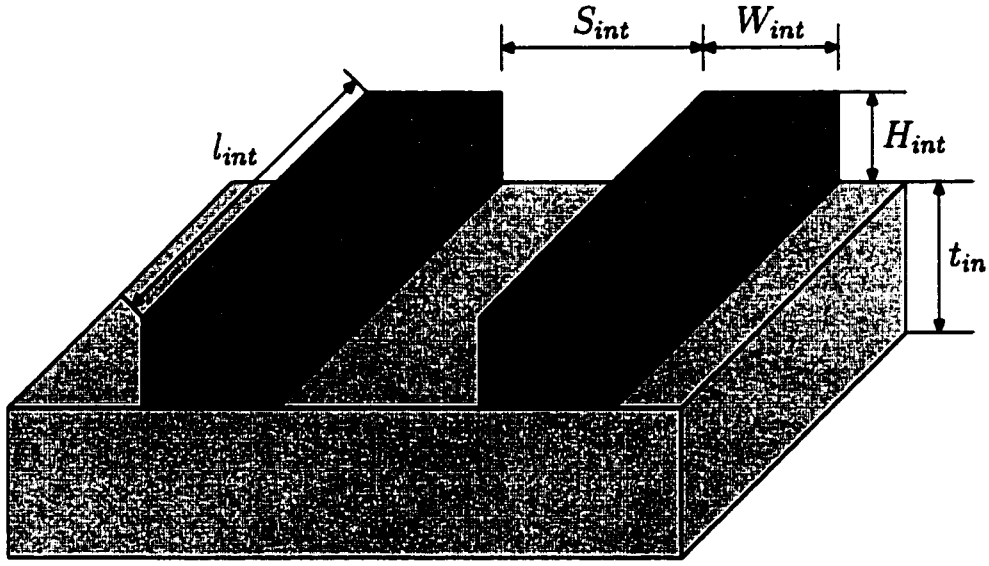


Figure 2.3: Geometric parameters of interconnect lines

The ideal scaling of local and global interconnect lines are listed in Tables 2.3 and 2.4. A typical length of a global interconnect line is $\sqrt{A_c}/2$, where A_c is the chip area. For global interconnections, S_c is the scaling factor for the chip size ($S_c > 1$).

Table 2.3: Ideal scaling of local interconnect

Parameters	Ideal scaling
Thickness (H_{int})	$1/S$
Width (W_{int}	$1/S$
Separation (S_{int})	$1/S$
Insulator thickness(t_{in})	$1/S$
Length (l_{loc})	$1/S$
Resistance (R_{int})	S
Capacitance to substrate	$1/S$
Capacitance between lines	$1/S$
RC delay (τ_{RC})	1
Voltage drop (IR)	1
Current density ($J = \frac{I}{H_{int}W_{int}}$)	S

Table 2.4: Ideal scaling of global interconnect

Parameters	Ideal scaling
Thickness (H_{int})	$1/S$
Width (W_{int}	$1/S$
Separation (S_{int})	$1/S$
Insulator thickness(t_{in})	$1/S$
Length (l_{loc})	S_c
Resistance (R_{int})	S^2S_c
Capacitance (C_{int})	S_c
RC delay (τ_{RC})	$S^2S_c^2$

The delay of local interconnect lines remains the same although the delay of the MOS transistors decreases by $1/S$. Moreover, the delay of global interconnect lines increases by $S^2S_c^2$. Therefore, interconnect delay has become more critical than gate delay in deep submicrometer integrated circuits.

2.2 On-Chip Inductance

Because of the lossy nature of the on-chip interconnect lines, the parasitic inductance is not important in low and medium frequency applications, where the transition times of on-chip signals are greater than the transmission delay of the on-chip interconnections. On-chip inductance becomes important as the transition time becomes comparable to the transmission delay for low loss interconnections or the inductive time constant of an interconnection exceeds the resistive time constant [43].

The on-chip inductance is a complex circuit structure. The self-inductance of a metal line is related to a current loop [23]. For simplicity, the signal propagation along an interconnect line is approximated as a TEM or quasi-TEM wave, as shown in Figure 2.4, where the silicon substrate is assumed to be an ideal ground plane. The parasitic inductance of the interconnect line per unit length can be determined from (2.3),

$$L = \frac{\mu \int_s \vec{H} d\hat{s}}{\oint_c \vec{H} d\hat{l}}, \tag{2.3}$$

where μ is the permeability of the dielectric.

The penetration of an electromagnetic field, however, is determined by the "skin depth" δ in (2.4),

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0}}, \tag{2.4}$$

where ρ is the resistivity of the dielectric and f is the operating frequency. Due to the high resistivity of the silicon substrate (25 mΩ-cm as compared to 4 $\mu\Omega$-cm of metal lines), the penetration depth is about 250 μm in the silicon substrate at 1 GHz, which is almost half the thickness of a typical wafer. The parasitic induc-

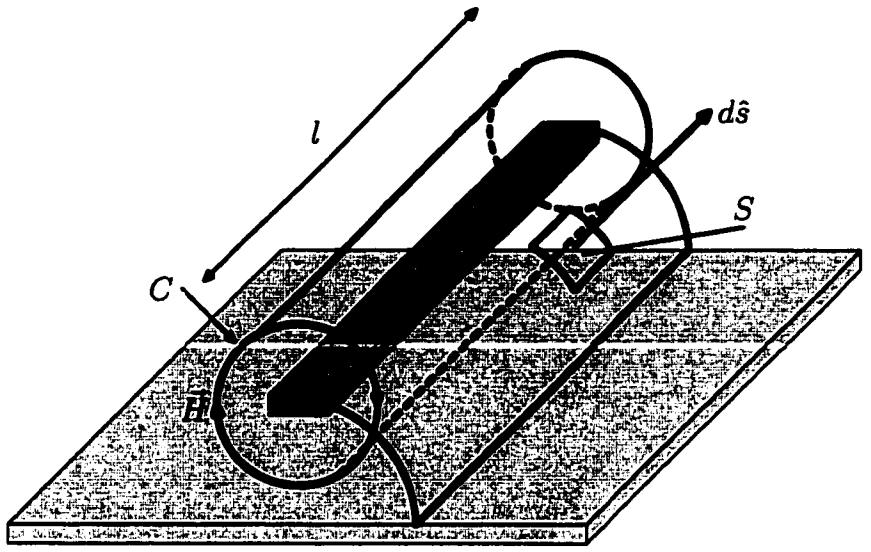


Figure 2.4: Parasitic inductance of an on-chip interconnect line

tance of a metal line above the silicon substrate is greater than the corresponding value estimated based on an ideal ground plane [44].

The current return path also greatly complicates the issue of on-chip inductance. Due to the high resistivity of the silicon substrate, the current returns through the nearby ground lines and the silicon substrate. The process in which the on-chip inductance is accurately determined is an on-going and active research problem and is not a topic discussed within this dissertation.

The on-chip inductance becomes important when the active lossless characteristics exceed the resistive lossy characteristics of the interconnect which depends upon the operating frequency and the parasitic impedances of the interconnect line. The line impedance versus frequency for two metal lines with different widths is shown in Figure 2.5 [44]. In this example, the thickness of the metal line is $1\,\mu$m and the oxide thickness is $2\,\mu$m. The width of the wide line is $200\,\mu$m and the width of the narrow line is $2\,\mu$m. For a wide, low resistance line, the impedance

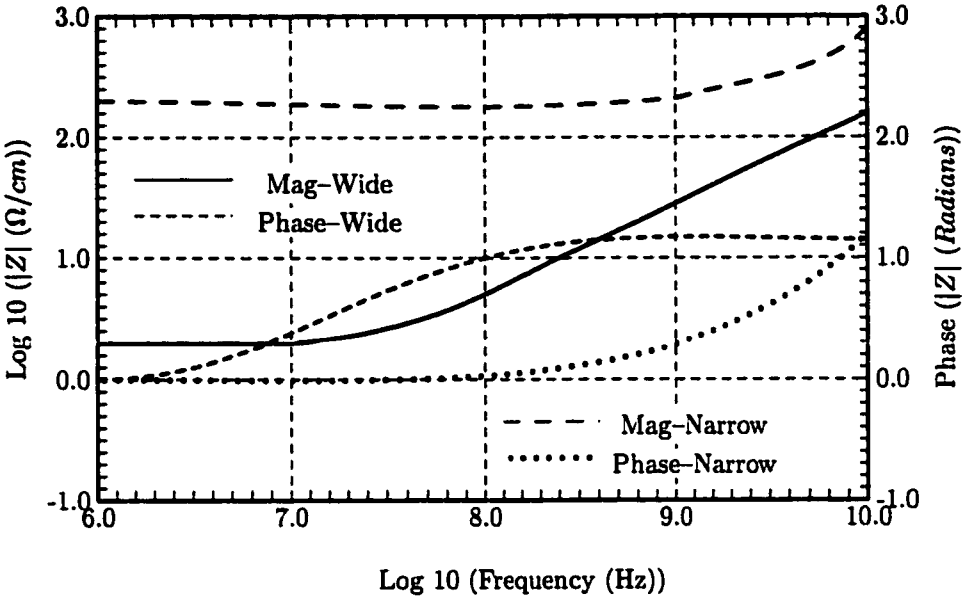


Figure 2.5: Series impedance of metal lines over the silicon substrate

is roughly doubled and is more active than resistive (the phase angle $> \pi/4$) at 100 MHz. For the narrow line, the crossover from a line exhibiting resistive characteristics to inductive characteristics occurs at a much higher frequency.

On-chip inductance is one of the basic characteristics of on-chip interconnections in addition to the capacitance and resistance in CMOS integrated circuits. The on-chip inductance has not been particularly important in low and medium frequency applications or high lossy environments. It is necessary to include on-chip inductance in the interconnect model for low loss interconnections operating in high speed applications.

2.3 Interconnect Modeling

Interconnections have become important in determining the speed, power, area, reliability, and yield of CMOS integrated circuits. It is necessary to pre-

dict the timing, voltage, and power characteristics of a CMOS logic gate driving an interconnect line at the system level, providing design guidelines for optimal repeater insertion to improve the performance of deep submicrometer integrated circuits.

The choice of an appropriate interconnect model depends upon the characteristics of the target application. A capacitive model of the interconnect is introduced in Section 2.3.1. A resistive and an inductive interconnect model are addressed in Sections 2.3.2 and 2.3.3, respectively.

2.3.1 Capacitive Interconnect

For long channel devices, the gate capacitance dominates the total load capacitance, permitting the interconnect capacitance to be neglected. As the feature size of devices is scaled down and chip dimensions are increased, the interconnect capacitance has become more important. The interconnect can be modeled as a capacitor when the interconnect capacitance is comparable to the gate capacitance of the following logic stage, as shown in Figure 2.6. With increasing chip size and integration density, the performance of a CMOS integrated circuit is limited by the interconnect capacitance. A capacitive model of the interconnect is appropriate for low frequency applications and for those conditions under which the interconnect capacitance dominates the gate capacitance.

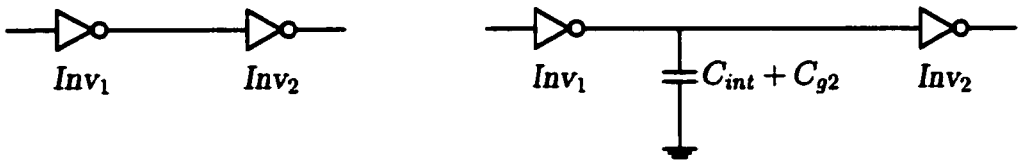


Figure 2.6: Capacitive model of the interconnect

2.3.2 Resistive-Capacitive Interconnect

The parasitic resistance of both local and global interconnections increases as CMOS technologies are scaled, as listed in Tables 2.3 and 2.4. The interconnect resistance should be included within an interconnect model when the parasitic resistance is comparable to the output resistance of the CMOS logic gate driving the interconnect line. Therefore, the interconnect should be modeled as a lumped *RC* or distributed *RC* line, as shown in Figure 2.7. The resistive-capacitive interconnect model is appropriate for medium and long interconnect lines at medium frequency applications. The critical length for an interconnect line to be modeled as a resistance-capacitive interconnect is

$$l_{\text{int, cric}} \approx \frac{R_{tr} W_{int} H_{int}}{\rho}, \tag{2.5}$$

where R_{tr} is the output resistance of the CMOS logic gate driving the interconnect line.

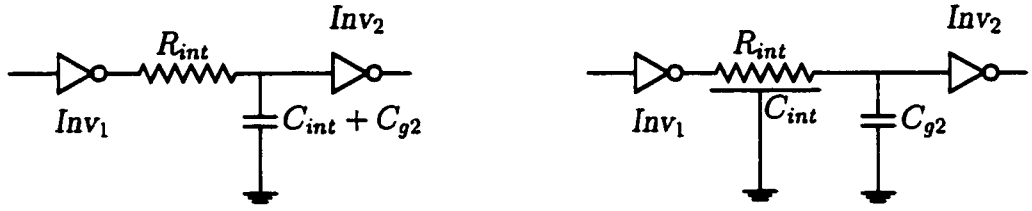


Figure 2.7: Resistive-capacitive model of the interconnect

2.3.3 Inductive Interconnect

If the transition times of the on-chip signals in high speed VLSI circuits are comparable to the time of flight of the signals propagating along the low resistivity interconnect line, the effects of inductance should also be considered in the

interconnect model [44, 45]. The condition when on-chip inductance cannot be neglected [45] is

$$\tau \approx \tau_p = \frac{l_{int}}{\sqrt{L_{int}C_{int}}}, \tag{2.6}$$

$$C_L \ll C_{int}l_{int}, \tag{2.7}$$

$$Z_{drv} \approx Z_0, \tag{2.8}$$

$$R_{int}l_{int} \leq 2Z_0 = 2\sqrt{\frac{L_{int}}{C_{int}}}, \tag{2.9}$$

where τ is the transition time of the on-chip signals, τ_p is the wave propagation delay time along the interconnect line, Z_0 is the characteristic impedance of the interconnect line, C_L is the gate capacitance of the following logic stage, and Z_{drv} is the driver output impedance (Inv_1). R_{int}, C_{int}, and L_{int} are the interconnect resistance, capacitance, and inductance per unit length, respectively. l_{int} is the length of the interconnect line. The first constraint means that the transition time of the signals is comparable to the transmission delay along the interconnect line. The second and third constraints are the conditions under which ringing occurs, an important characteristic of on-chip inductance. The final constraint requires the interconnect line to be low loss, making the signal attenuation small. Low loss interconnect in high speed integrated circuits should therefore be modeled as a lumped *RLC* or as a distributed *RLC* line, as shown in Figure 2.8.

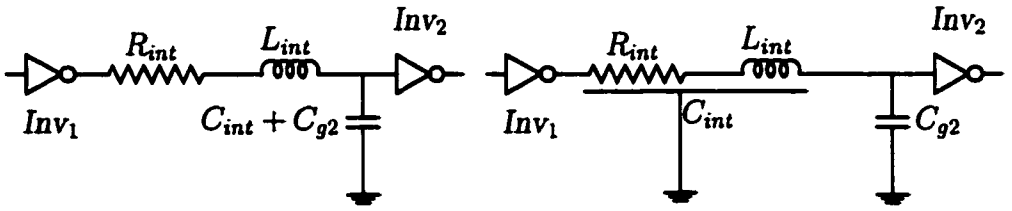


Figure 2.8: Inductive model of the interconnect

2.4 The nth Power Law Model

The Shichman-Hodges model [46] for MOSFETs has been widely used in analyzing the characteristics of MOSFET circuits [47, 48]. However, the model is no longer accurate for short-channel MOS transistors because it neglects the effects of velocity saturation on the carriers, which is significant in the submicrometer regime. Alternatively, there are more precise MOS models like SPICE Level 3 [49], BSIM [50], and high level empirical models implemented in HSPICE [51]. Most of these models do not permit a tractable expression of the characteristics of a MOSFET circuit.

The alpha power law I-V model [52] was first proposed in 1990 to fill the gap between the simple Shichman-Hodges model and these more precise (and complicated) I-V models. However, this model is not accurate in the linear region and in determining the drain-to-source saturation voltage of an MOS transistor. An improved model, the nth power law model [41], has also been proposed by the same authors. The nth power law model is used in this dissertation to derive tractable analytical equations to characterize the circuit operation, thereby improving the understanding of the device and circuit behavior in the submicrometer regime.

The nth power law model [41] is used to characterize a short-channel MOS transistor and are represented by the following expressions:

$$V_{DSAT} = K(V_{GS} - V_{TH})^m, \tag{2.10}$$

$$\begin{aligned} I_{DS} = I_{DSAT} &= B'\frac{W_{\text{eff}}}{L_{\text{eff}}}(V_{GS} - V_{TH})^n \\ &= B(V_{GS} - V_{TH})^n \quad (V_{DS} \geq V_{DSAT} : \text{saturation region}), \end{aligned} \tag{2.11}$$

$$I_{DS} = I_{DSAT}(2 - \frac{V_{DS}}{V_{DSAT}})\frac{V_{DS}}{V_{DSAT}} \quad (V_{DS} < V_{DSAT} : \text{linear region}), \tag{2.12}$$

$$I_{DS} = 0 \qquad (V_{GS} < V_{TH} : \text{cutoff region}), \tag{2.13}$$

where V_{GS} and V_{DS} are the gate-to-source voltage and drain-to-source voltage, respectively. W_{eff} and L_{eff} are the effective channel width and effective channel length, respectively. V_{TH} is the threshold voltage and I_{DS} is the drain-to-source current. V_{DSAT} is the drain-to-source saturation voltage. n, m, K, and B are constants used to empirically characterize the short-channel effects and can be extracted based on experimental I-V data. n characterizes the effects of velocity saturation and is typically between one and two. For extremely short devices, n is close to one. The parameters K and m control the linear region characteristics while B' and n determine the saturation region characteristics.

This model reduces to the Shichman-Hodges model [46] if $K = 1$, $m = 1$, $B' = 0.5\beta$, and $n = 2$. A comparison of the nth power law model and the Shichman-Hodges model with simulations based on SPICE Level 3 is shown in Figure 2.9 for a $0.5\,\mu$m MOS transistor. Note that the nth power law can accurately model the I-V characteristics of a short-channel MOS transistor.

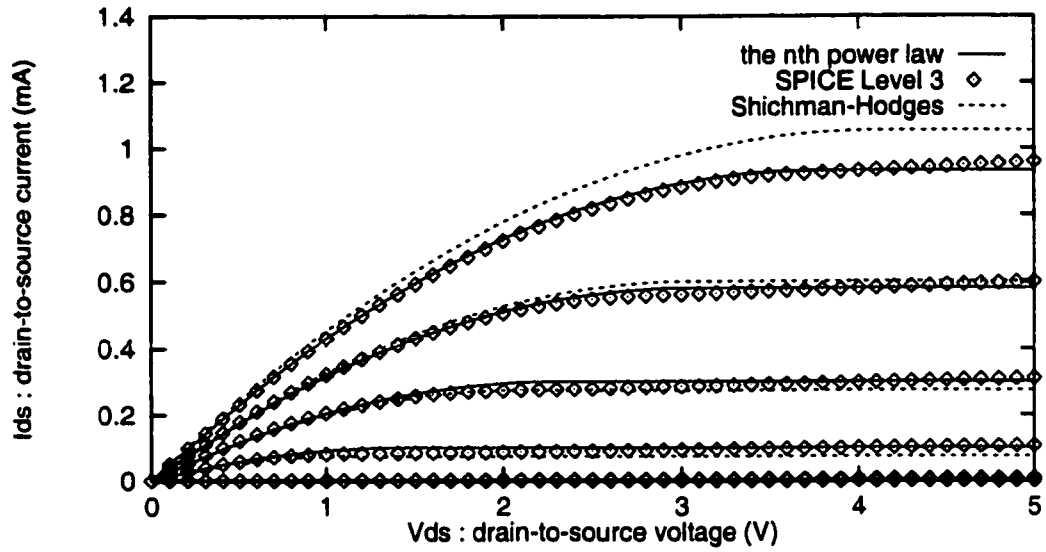


Figure 2.9: I_{ds}-V_{ds} characteristics based on SPICE Level 3 are compared to the nth power law and Shichman-Hodges models.

2.5 Noise Margin

The voltage transfer characteristics (VTC) of a CMOS inverter is shown in Figure 2.10. The regions of acceptable logic high and low voltages are defined as V_{IH} and V_{IL}, respectively. The region between V_{IH} and V_{IL} is called the *undefined region* or *transition region*.

$$\begin{aligned} V_{out} &\geq V_{OH} \qquad \text{when } V_{in} \leq V_{IL}, \\ V_{out} &\leq V_{OL} \qquad \text{when } V_{in} \geq V_{IH}, \end{aligned} \tag{2.14}$$

where $V_{IH} > V_{IL}$. Steady-state signals in a digital circuit should avoid this region to ensure proper circuit operation.

For a CMOS logic gate to be robust and insensitive to noise disturbances, it is essential that the logic low and logic high interval should be as wide as possible. A measure of the sensitivity of a logic gate to noise is the noise margins, denoted by NM. The noise immunity of a digital circuit increases with NM. Two noise

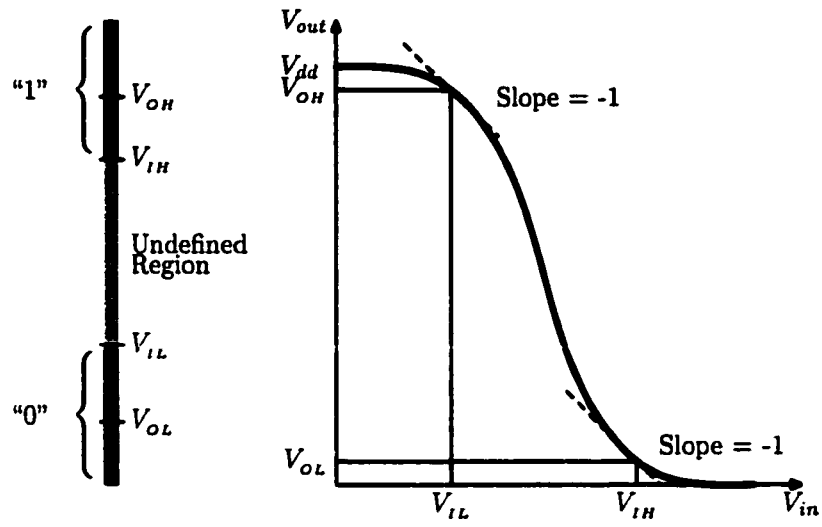


Figure 2.10: Voltage transfer characteristics and mapping of the digital logic levels of a CMOS inverter

margins are defined as NM_L (*the noise margin low*) and NM_H (*the noise margin high*).

$$NM_L = V_{IL} - V_{OL}, \tag{2.15}$$

$$NM_H = V_{OH} - V_{IH}. \tag{2.16}$$

The noise margins characterize the levels of noise that can be satisfied when logic gates are cascaded. As indicated in Figure 2.11, the valid region of the input and output voltages, the noise margins represent the amount of variation in the signal levels allowed as the signal is transmitted from the output of one logic gate to the input of the following logic gate. With technology scaling, the voltage supply V_{dd} has decreased, decreasing the noise margins, as shown in Figure 2.11. The signal-to-noise ratio has also decreased due to the scaling of the CMOS technology [53].

The noise margin in VDSM static CMOS integrated circuits has decreased since the power supply voltage has also been scaled down by two to three times

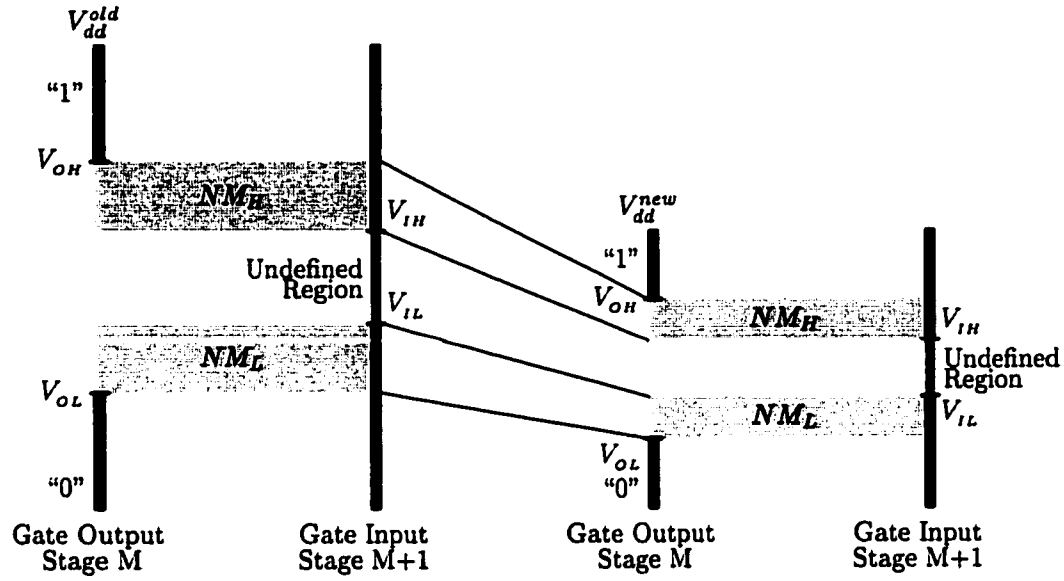


Figure 2.11: Effect of scaling supply voltage on the noise margins

in order to maintain a constant electric field [32]. The threshold voltages of the MOS devices, however, have been decreased only slightly so as to control the magnitude of the subthreshold current [54]. Moreover, the noise immunity of a dynamic CMOS integrated circuit is even poorer than its static counterpart since the switching threshold of a dynamic circuit is the threshold of a single transistor [55, 56]. Therefore, the noise margin of both static and dynamic circuits has been significantly reduced in VDSM CMOS integrated circuits, making the impact of noise on circuit performance, which until recently was considered to be a second order effect, a fundamental integrated circuit design issue.

2.6 Signal Integrity

The term *noise* in the context of digital integrated systems has come to mean *unwanted variations of the voltages and currents at various logic nodes* [33]. This

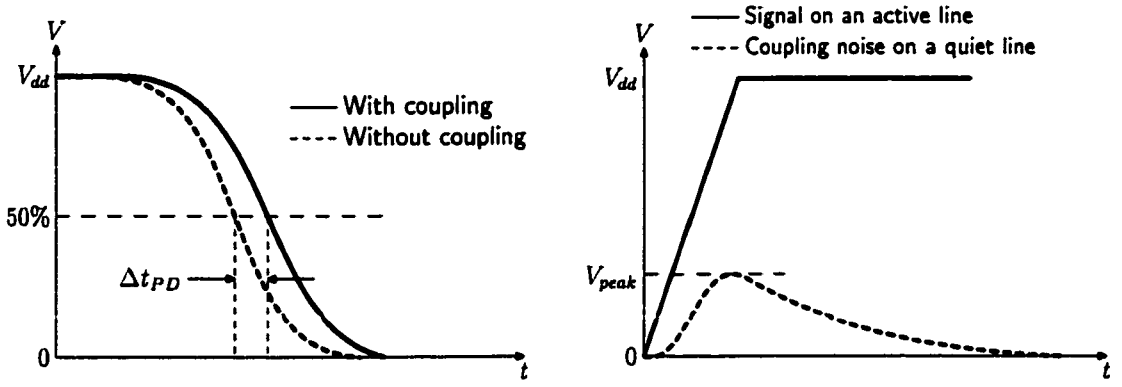
noise becomes significant when the signal begins to incorrectly switch within logic states, dissipating additional power, delaying switching times, and potentially creating catastrophic faults. One source of noise in a CMOS integrated circuit is the interference signal induced by signals on neighboring interconnect lines. This noise is different from the *intrinsic* noise generated by FETs or by other active devices. This FET noise is essentially an *unpredictable* and *random* phenomenon [23].

Noise has become a problem in sub 0.25 μm CMOS technologies, in which the interconnect has become an increasingly dominant factor in circuit design. Technology scaling has caused fringing coupling capacitance between on-chip signals to become a large fraction of the total capacitance. At the same time, as transistor dimensions are shrunk and the number of long interconnects has increased, the amount of interconnect-related capacitance is becoming larger and more significant than the gate capacitance [17–20].

A common strategy is to evaluate the coupling between individual signals where one line acts as an "aggressor," inducing a voltage and/or current change on an adjacent "victim" line, thereby causing a functional failure or the storage of an incorrect logic state. Coupling noise can also affect switching circuits by altering the propagation delay by increasing the load on a line, thereby causing timing uncertainty, as shown in Figure 2.12.

2.6.1 Coupled Interconnect

Interconnections in CMOS integrated circuits are multi-conductor lines existing on different physical planes [14]. The parasitic resistance, capacitance, and resistance of the conductor lines can be extracted from the geometric layout [57–59]. The coupling capacitance is physically a fringing capacitance between neighboring interconnect lines, which strongly depends on the physical structure of the



(a) Delay uncertainty due to coupling

(b) Coupling noise voltage on a quiet line

Figure 2.12: Effects of coupled on-chip interconnect

adjacent interconnections [60–62]. For parallel metal lines on the same layers, the fringing capacitance will increase as the spacing between the interconnections decreases and the thickness-to-width aspect ratio of the interconnection increases. Due to the screen effect of low level interconnect, the metal-to-metal coupling capacitance among different layers can also contribute to the total coupling capacitance [23].

Because the nearby ground lines are part of the current return path when the on-chip inductance cannot be neglected, inductive coupling can extend across great distances (in the context of VDSM semiconductors) by coupling among each other through the substrate and the common ground lines. The interconnect should therefore be modeled as a lumped *RLC* or lossy *RLC* transmission line in the design of high frequency circuits [63, 64]. Therefore, there are two coupling mechanisms in high speed VDSM integrated circuits, *i.e.*, capacitive coupling and inductive coupling [65]. The capacitive and inductive coupling will change

the effective load capacitance and inductance of a CMOS driver depending upon the signal activity. This effect will significantly alter the transient response of a CMOS driver as compared to not considering the coupling capacitance and inductance. Moreover, if the interconnect behaves like a distributed *RC* or *RLC* line, reflections due to discontinuities along the transmission lines can occur. In this dissertation, the signal distortion due to the nonuniformity of the on-chip interconnections is considered as a component of the total on-chip interconnect noise.

Coupling noise between adjacent interconnects can cause disastrous effects on the logical functionality and long-term reliability of a digital CMOS integrated circuit. Coupling effects become more significant as the feature size is decreased to VDSM dimensions (less than 0.25 μm) because the spacing between conductor lines is decreased and the thickness of the conductors is increased in order to reduce the parasitic resistance of the conductors. Not only may the coupling noise increase the delay of the logic gates, if the peak noise voltage at the receiver is greater than the threshold voltage of the CMOS receiver, the noise may cause a circuit to malfunction. Furthermore, the induced noise voltage may cause extra power to be dissipated on the quiet line due to momentary glitches at the output of the logic gates. Carrier injection or collection into the substrate may occur as the coupling noise voltage rises above the power supply voltage V_{dd} or falls below ground [18]. These deleterious effects caused by the coupling noise voltage become aggravated as the relaxation time, the time for the coupling noise to reach a steady state voltage, increases.

2.6.2 Simultaneous Switching Noise

A necessary requirement of power distribution systems in high complexity CMOS circuits is to provide sufficient current to support both the average and the peak power demands within all parts of an integrated circuit. An inductive model is required to characterize the power supply rails when a transient current is generated by simultaneously switching the on-chip registers and logic gates in a synchronous CMOS circuit. Therefore, simultaneous switching noise (SSN - also known as Delta-I noise or ground bounce) originating from the internal circuitry is expected to become an important issue in the design of VDSM high performance integrated circuits by adding uncertainty to the delay analysis of the on-chip circuitry.

Simultaneous switching noise affects the signal delay, creating delay uncertainty since the power supply level temporally changes the local drive current. If the parasitic inductance of the on-chip power rails is sufficiently large and a large number of the internal on-chip drivers that are connected to the same power rail switch at close to the same time, a significant $L\,di/dt$ drop in the power supply voltage can momentarily occur. Furthermore, logic malfunctions may be created and excess power may be dissipated due to faulty switching if the power supply fluctuations are sufficiently large [66]. Some types of problems that are encountered due to simultaneous switching noise are false triggering, double clocking, and/or missing clocked pulses [67].

Besides simultaneous switching noise within the power supply rails, transient DC IR voltage drops can occur with high on-chip currents. Decreased power supply levels reduce the tolerance to voltage changes within power distribution networks in CMOS integrated circuits. These IR voltage drops can also create

delay uncertainty within the data path due to momentary changes in the supply voltage, making the maximum and minimum propagation delays difficult to estimate.

The interconnect coupling noise voltage and simultaneous switching noise voltage will increase as the spacing between the conductor lines decreases, the transition time of a signal decreases, the chip dimensions increase, and the total on-chip current increases. Therefore, it is necessary to propose a new design paradigm - Design for Noise (DFN).

2.6.3 Design For Noise

As the signal propagates along the interconnect, the signal integrity can be easily compromised. Therefore, the timing of critical signals can be significantly affected. Ringing, overshoots, and undershoots caused by transmission line effects, glitching, and transmission line delay can threaten noise immunity and signal monotonicity. Moreover, fast clock rates make it difficult to satisfy clock skew requirements, making on-chip crosstalk a significant issue. These signal integrity challenges can wreak havoc on the integrated circuit design process. Furthermore, at present many of these effects are detected only after the physical layout has been completed, wasting significant time and money. Special design effort is required to satisfy the performance requirements of the global signals on an integrated circuit, such as the clock and power supply distribution networks, which can lead to major circuit redesign efforts and multiple design iterations [38].

Although different noise sources have been addressed in the previous sections, these noise sources are actually related. The power distribution network is interconnect related since power buss lines are conductors on physical planes. Moreover, the power distribution network can affect the coupling noise. The inductive

return paths frequently pass through the power distribution network, making the layout and location of the power line relative to the high speed data paths of significant importance. The primary goal of this research described in this dissertation is to integrate all of these noise mechanisms into a unified design capability for estimating system level noise. Because the device and interconnect parameters are dependent upon low level physical structures, a bottom-up research strategy will be applied in the analysis of system level signal integrity.

2.7 Summary

Ideal scaling of CMOS technologies is addressed in this chapter. Because of scaling, the interconnect impedances have come to dominate the performance of deep submicrometer CMOS integrated circuits. On-chip inductance also cannot be neglected in high speed applications. A variety of interconnect models has therefore been presented, noting which model is appropriate depending upon the specific input, drive, and load conditions. Short-channel effects have also become important as the feature size of MOS transistors has shrunk. The nth power law I-V model is therefore used to characterize these short-channel MOS transistors. The noise margins in CMOS logic gates have also decreased with technology scaling, making on-chip interconnect noise including on-chip simultaneous switching noise of increasing importance. Therefore, on-chip interconnect noise and signal integrity must be considered in new developmental disciplines, creating a new design paradigm, Design For Noise.

Chapter 3

Lumped Versus Distributed On-Chip Interconnect Impedances

3.1 Introduction

The driving force behind the rapid growth of the CMOS integrated circuit technology has been the continuous reduction of the feature size of MOS transistors [1, 15]. Since the chip size and the integration density have both increased dramatically, the average interconnect length has not scaled down with decreasing feature size [10, 11]. Therefore, on-chip interconnect has become increasingly important in determining system (or circuit) performance [28, 35]. The delay of these highly scaled integrated circuits has now become dominated by the interconnect impedance rather than the active transistor components [1, 14].

On-chip interconnect in modern CMOS integrated circuits not only has become important but also is very difficult to model in predicting the circuit performance, since the *distributed nature* of the on-chip interconnections has to be considered. On-chip interconnect in CMOS integrated circuits has historically been modeled as a capacitive load, including the interconnect parasitic capaci-

tance and the gate capacitance of the following logic stage [68, 69]. Analytical expressions characterizing the output voltage and propagation delay of a CMOS logic gate driving a purely capacitive load have been previously addressed in the literature [47, 48, 52, 70]. The effect of short-circuit current on the propagation delay has also been described in [71]. A comprehensive delay model of a CMOS logic gate driving a capacitive load has been summarized in [72, 73].

Due to the scaling of CMOS integrated circuit technologies [1, 15], the interconnect parasitic resistance has increased significantly. If the interconnect resistance becomes comparable to the effective output resistance of a CMOS logic gate, the interconnect impedance must be modeled as a resistive-capacitive load [15, 74, 75]. The transient analysis of a CMOS logic gate driving a resistive-capacitive load [76, 77] has recently been addressed in the literature in terms of the output voltage and propagation delay [47, 71, 73, 78–80].

If the signal transition times in high speed CMOS integrated circuits are comparable to the time of flight of the signals propagating along a low resistivity interconnect line (the inductive time constant of an interconnection exceeds the resistive time constant), the interconnect inductance should also be considered in the interconnect model [44, 45, 63, 64]. The interconnect in these high speed integrated circuits should therefore be modeled as a lumped or distributed *RLC* line [43, 81]. A guideline for choosing an appropriate interconnect model has been described in Chapter 2.

On-chip interconnections in CMOS integrated circuits can be modeled as distributed lines [82]. However, a distributed model causes significant computational complexity in characterizing the propagation delay and voltage waveform of a CMOS logic gate driving on-chip interconnect since the MOS transistors are non-

linear devices. Nonlinear circuit theory is therefore required to solve the circuit equations characterizing this system. In order to develop analytical expressions characterizing the behavior of a CMOS logic gate driving an *RC* or *RLC* interconnect, some simplifications should be applied [82, 83]. Sakurai presents in 1983 a simplified model in [74] to characterize a resistive-capacitive interconnect line. However, a unified equation cannot be developed based on the model presented in [74]. Interconnect is modeled as an *RC* and *RLC* transmission line in [78] and [81], respectively, while an MOS transistor is approximated by an effective output resistance. An MOS transistor behaves like a current source when operating in the saturation and can be approximated by a resistor when operating in the linear region. Therefore, the analytical expressions described in [78] and [81] may not accurately predict the voltage waveform of a CMOS logic gate. A simple π model is used in [79] and [80] to characterized the effective load capacitance of a CMOS logic gate. A curve fitting technique is applied in [79] and [80] to characterize the output voltage waveform instead of using device parameters, losing the physical intuition of the circuit behavior of a CMOS logic gate.

A Fourier analysis of typical on-chip signals in CMOS integrated circuits is presented in this chapter. On-chip signals are approximated by a Fourier series up to the 15th harmonic component. The effective load impedance of a distributed *RC* and *RLC* line driven by a CMOS logic gate is based on this Fourier analysis of the on-chip signals, which includes the frequency dependence of the interconnect impedance. The effective load impedance model presented here is based on the input transition time and the distributed characteristics of the on-chip interconnections. The voltage waveform based on the effective load impedance model is

similar to a distributed *RC* and *RLC* line approximated by sections of lumped *RC* and *RLC* elements.

A Fourier analysis of typical on-chip signals in CMOS integrated circuits is presented in Section 3.2. Analytical expressions characterizing the effective load impedance of a distributed *RC* and *RLC* line are developed in Section 3.3 based on the Fourier analysis of the on-chip signals. Signal waveforms of the output voltage of a CMOS logic gate based on the effective load impedance model are also compared in this section to those based on distributed interconnect followed by some concluding remarking in Section 3.4.

3.2 Fourier Analysis of On-Chip Signals

The solid line shown in Figure 3.1 depicts a typical voltage waveform of an on-chip signal in a CMOS integrated circuit. The signal is assumed to behave periodically with a period of T. The dashed line shown in Figure 3.1 approximates an on-chip signal, with rising and falling transition times τ_r and τ_f, respectively. The signal represented by the dashed line shown in Figure 3.1 can be expressed as

$$V(t) = \begin{cases} \frac{t}{\tau_r} V_{dd} & 0 \le t \le \tau_r, \\ V_{dd} & \tau_r \le t \le \frac{T}{2}, \\ V_{dd}(1 - \frac{t}{\tau_f} + \frac{T}{2\tau_f}) & \frac{T}{2} \le t \le (\frac{T}{2} + \tau_f), \\ 0 & (\frac{T}{2} + \tau_f) \le t \le T. \end{cases} \tag{3.1}$$

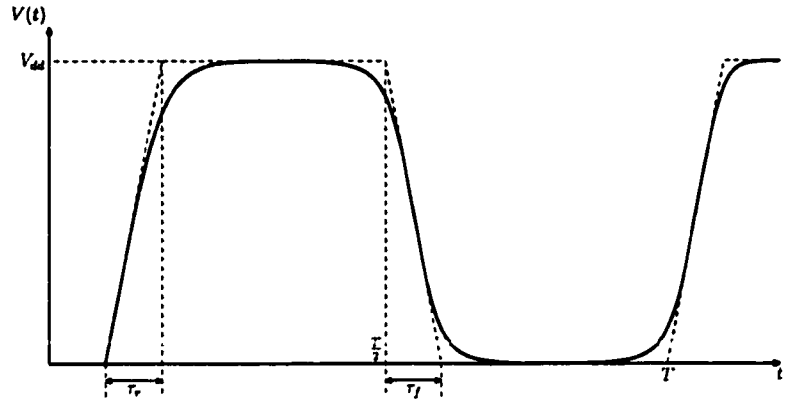


Figure 3.1: Typical voltage waveform of an on-chip signal in a CMOS integrated circuit.

For on-chip signals in a practical CMOS integrated circuit, τ_r is typically equal to τ_f [33, 52, 55]. Therefore, the Fourier series of $V(t)$ is

$$V(t) = \frac{V_{dd}}{2} + \sum_{\substack{m=2k+1 \\ k=0}}^{k=\infty} \frac{T}{\tau_r} \frac{V_{dd}}{m^2\pi^2} \left[(\cos m\omega_o\tau_r - 1)\cos m\omega_o t + (\sin m\omega_o\tau_r)\sin m\omega_o t\right], \tag{3.2}$$

where $\omega_o = 2\pi/T$. The amplitude of the mth order harmonic component is

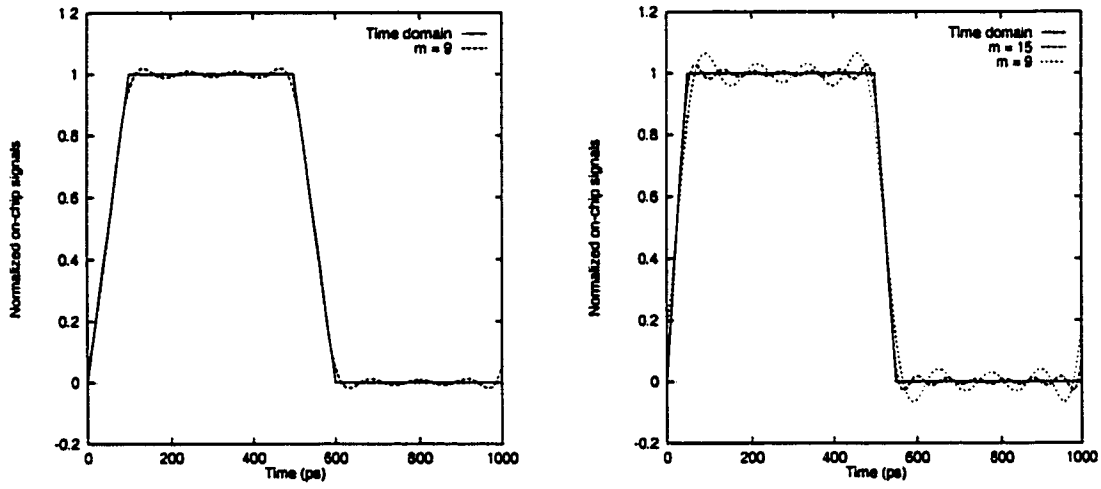
$$A_m = \frac{T}{\tau_r} \frac{V_{dd}}{m^2\pi^2} \left[(1 - \cos m\omega_o\tau_r) + |\sin m\omega_o\tau_r|\right] \frac{\sqrt{2}}{2}, \tag{3.3}$$

where m is an odd number. Note that the amplitude of the DC component is $V_{dd}/2$ and A_m depends upon the ratio of T over τ_r, which means significantly higher order harmonic components existing for short transition times. Since A_m deceases quadratically with m, $V(t)$ can therefore be approximated by the first several higher order harmonic components.

For the condition of $\tau_r/T = 0.1$ ($\tau_r = 100$ ps at a one gigahertz operating frequency), the Fourier series with $m = 9$ is compared to a time domain waveform in Figure 3.2(a). Note that the waveform derived from the Fourier series is quite

close to the voltage waveform in the time domain with $m=9$. If τ_r/T is greater than 0.1, note that a Fourier series with $m=9$ can be used to reproduce the on-chip signals in a CMOS integrated circuit.

If the transition time of the on-chip signals is quite short, for example, if $\tau_r/T=0.05$ ($\tau_r=50\,\text{ps}$ at a one gigahertz operating frequency), the waveforms derived from the Fourier series with $m=9$ and $m=15$ are similar to the time domain waveform as shown in Figure 3.2(b). Note that the waveform determined by the Fourier series with $m=15$ is quite accurate as compared to the time domain waveform. Therefore, if τ_r/T is less than 0.1, the Fourier series with $m=15$ can be used to approximate on-chip signals in a CMOS integrated circuit.



(a) $\tau_r/T=0.1$ and $m=9$

(b) $\tau_r/T=0.05$, $m=9$, and $m=15$

Figure 3.2: Comparison of signal waveform based on a Fourier series with the waveform based on the time domain.

3.3 Effective Lumped Load Versus Distributed Lines

On-chip interconnections can be approximated by sections of lumped circuit elements [15, 74, 82]. Based on a Fourier analysis of the on-chip signals presented in Section 3.2, analytical expressions characterizing the effective load impedance for a resistive and inductive distributed line are developed in Sections 3.3.1 and 3.3.2, respectively. Signal waveforms of the output voltage of a CMOS logic gate based on the effective impedance model are also compared to those based on a distributed *RC* and *RLC* line.

3.3.1 Distributed *RC* lines

A distributed *RC* line can be approximated by n sections of lumped *RC* elements as shown in Figure 3.3(a) [74]. In order to derive tractable analytical expressions characterizing the signal waveform of the output voltage of a CMOS logic gate driving a resistive-capacitive interconnect, an effective load resistance and capacitance are used to approximate a distributed *RC* line as shown in Figure 3.3(b).

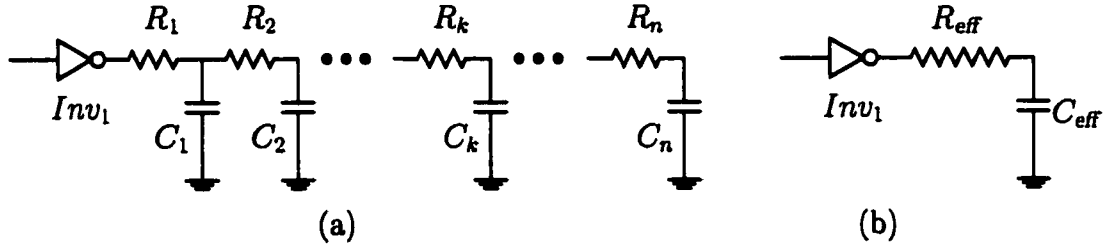


Figure 3.3: A resistive-capacitive interconnect line, (a) a distributed *RC* line approximated by n sections of lumped elements, (b) the effective load impedance, R_{eff} and C_{eff}.

If the number of sections n is more than two, the effective load resistance and capacitance can be determined from (3.6) and (3.7) (see Table 3.1) based on an

$L2$ circuit model of a nonuniform RC line as shown in Figure 3.4(a). In order to simplify the problem, a distributed RC line is assumed to be uniform in this discussion.

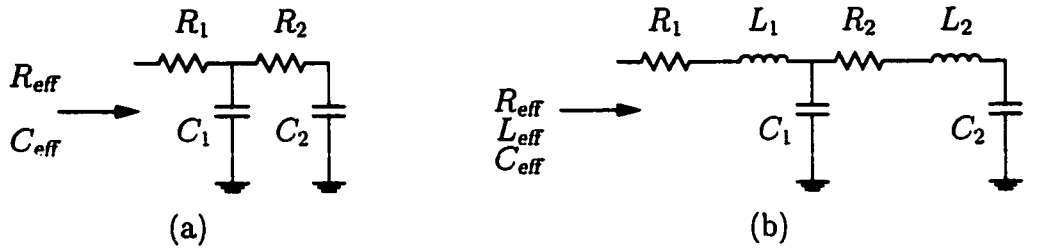


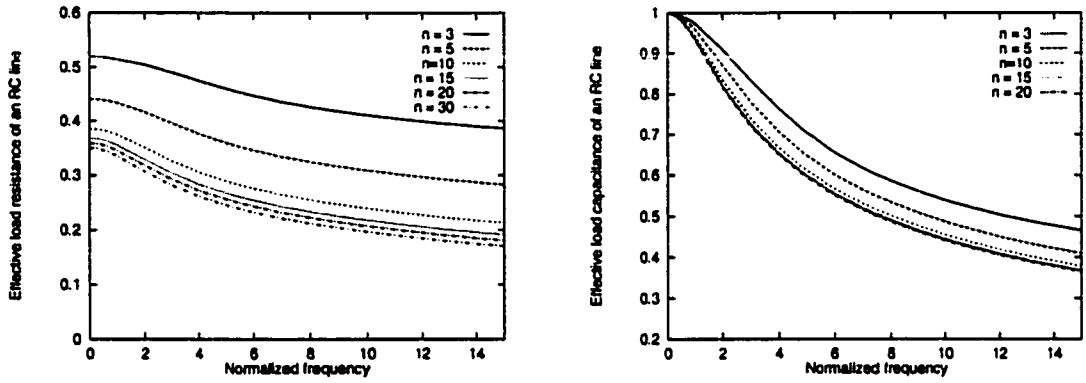
Figure 3.4: L2 model of nonuniform RC and RLC lines, (a) a resistive-capacitive load, (b) an inductive load.

Table 3.1: Analytical expressions characterizing the effective load impedance of a distributed RC line

No. of sections	Analytical Expressions
$n=1$	$R_{\text{eff}}(\omega) = R$ (3.4) $C_{\text{eff}}(\omega) = C$ (3.5)
$n \geq 2$	$R_{\text{eff}}(\omega) = R_1 + \frac{R_2}{(R_2\omega C_1)^2 + (\frac{C_1+C_2}{C_2})^2}$ (3.6) $C_{\text{eff}}(\omega) = \frac{(\omega R_2 C_2)^2(\frac{C_1}{C_1+C_2})^2 + 1}{(\omega R_2 C_2)^2 \frac{C_1}{C_1+C_2} + 1}(C_1 + C_2)$ (3.7)

The effective resistive and capacitive load impedance depends upon the operating frequency and the number of sections used to approximate the distributed RC line, as shown in Figure 3.5. The relative error of the effective load impedance is compared to an $n = 30$ distributed impedance in Figure 3.6. Note that if n is greater than ten, the relative error of $C_{\text{eff}}(\omega)$ is within 5%; however, the relative error of $R_{\text{eff}}(\omega)$ exceeds 10% for n less than fifteen. Therefore, the number of sec-

tion should be greater than 15 in order to accurately approximate a distributed RC line. Moreover, on-chip signals contain both DC and higher harmonic components rather than a single frequency component which cause additional complexity when determining the effective load resistance and capacitance.



(a) Effective load resistance $R_{\text{eff}}(\omega)$ of a distributed RC line

(b) Effective load capacitance $C_{\text{eff}}(\omega)$ of a distributed RC line

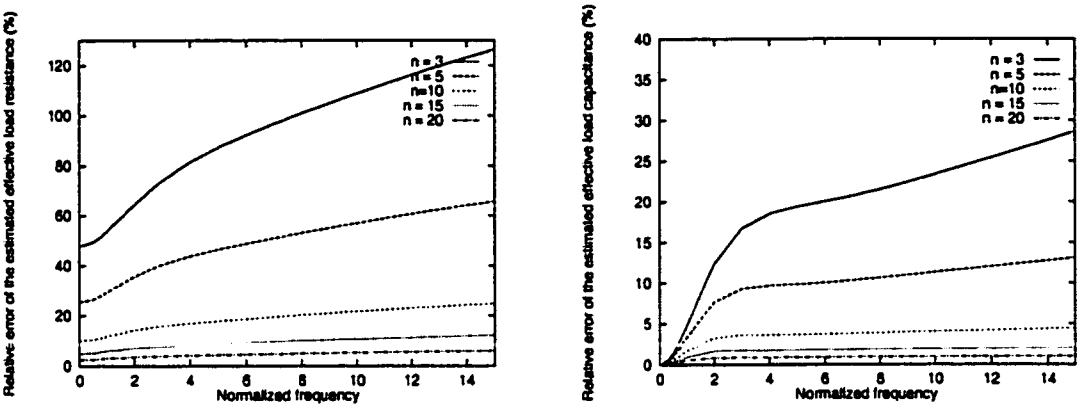
Figure 3.5: The effective load impedance of a uniform distributed RC line approximated by lumped elements with $n = 3, 5, 10, 14, 20$, and 30. The frequency is normalized to $\omega_{RC} = \frac{1}{RC}$.

In practical CMOS integrated circuits, the output transition time of a CMOS logic gate is similar to the input transition time [52]. Therefore, if the number of sections n is fixed, the effective load resistance and capacitance can be approximated by

$$R_{\text{eff}} = \left[A_0 R_{\text{eff}}(0) + \sum_{\substack{m=2k+1 \\ k=0}}^{k=4 \text{ or } 7} A_m R_{\text{eff}}(m\omega_o) \right] \left(A_0 + \sum_{\substack{m=2k+1 \\ k=0}}^{k=4 \text{ or } 7} A_m \right)^{-1}, \qquad (3.8)$$

and

$$C_{\text{eff}} = \left[A_0 C_{\text{eff}}(0) + \sum_{\substack{m=2k+1 \\ k=0}}^{k=4 \text{ or } 7} A_m C_{\text{eff}}(m\omega_o) \right] \left(A_0 + \sum_{\substack{m=2k+1 \\ k=0}}^{k=4 \text{ or } 7} A_m \right)^{-1}, \qquad (3.9)$$



(a) Relative error of the effective load resistance $R_{\text{eff}}(\omega)$

(b) Relative error of the effective load capacitance $C_{\text{eff}}(\omega)$

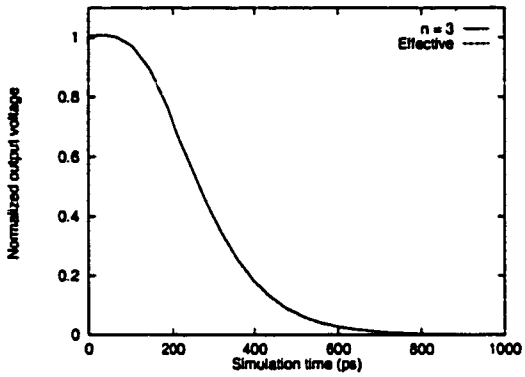
Figure 3.6: The relative error of the effective load resistance versus the number of sections. The frequency is normalized to $\omega_{RC} = \frac{1}{RC}$

where $A_0 = V_{dd}/2$ is the amplitude of the DC component of the on-chip signals in a CMOS integrated circuit.

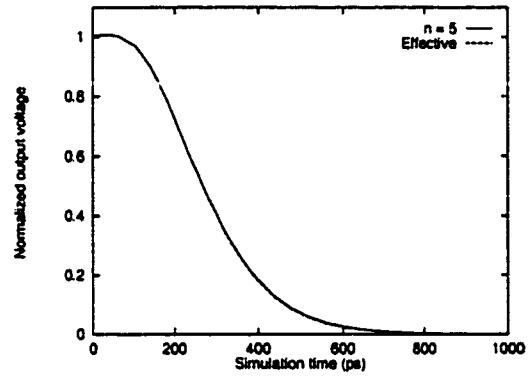
SPICE simulations based on an effective load resistance and capacitance, determined from (3.8) and (3.9), are compared to a distributed RC line as shown in Figures 3.7 and 3.8. Note that the voltage waveform based on the effective load resistance and capacitance is almost the same as the waveform based on a distributed RC line model.

3.3.2 Distributed *RLC* lines

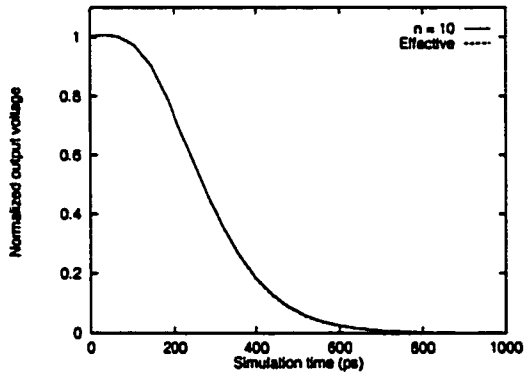
There are two time constants associated with a distributed RLC line, an inductive time constant $\sqrt{LC}$ and a resistive time constant RC [43]. A typical condition for the on-chip inductance to become important is if the inductive time constant is comparable to or exceeds the resistive time constant of an on-chip interconnection [44, 45]. A distributed RLC line can be approximated by n sections



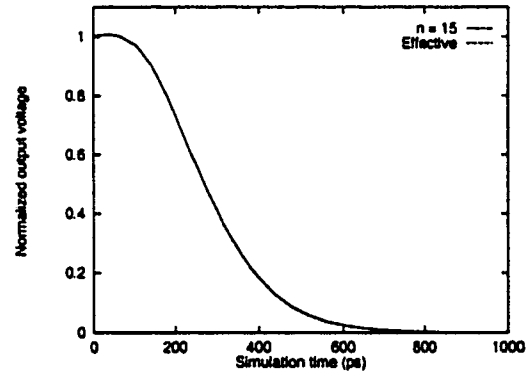
(a) SPICE simulation with $n = 3$ versus the effective load model



(b) SPICE simulation with $n = 5$ versus the effective load model

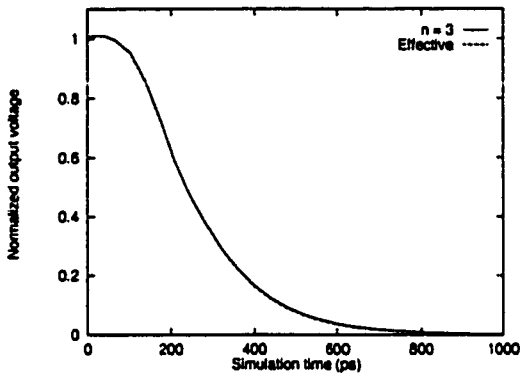


(c) SPICE simulation with $n = 10$ versus the effective load model

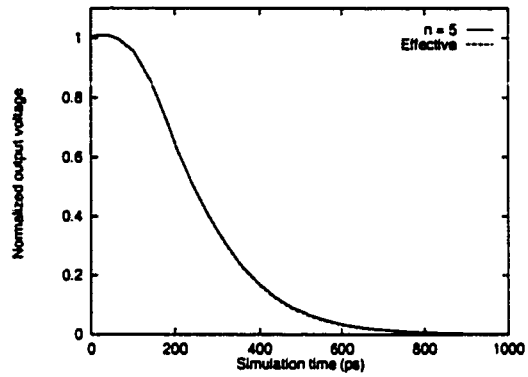


(d) SPICE simulation with $n = 15$ versus the effective load model

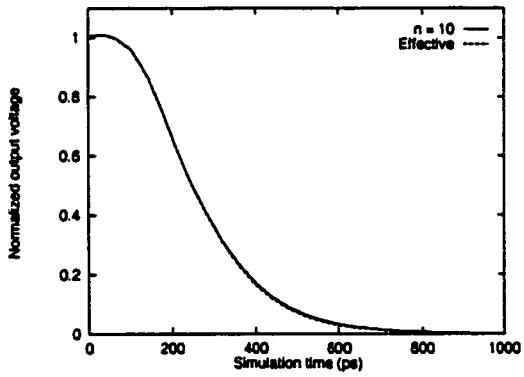
Figure 3.7: Comparison of the effective load model with SPICE for a distributed RC line, $R = 200\,\Omega$ and $C = 0.2\,\text{pF}$ with $n = 3$, 5, 10, and 15, respectively.



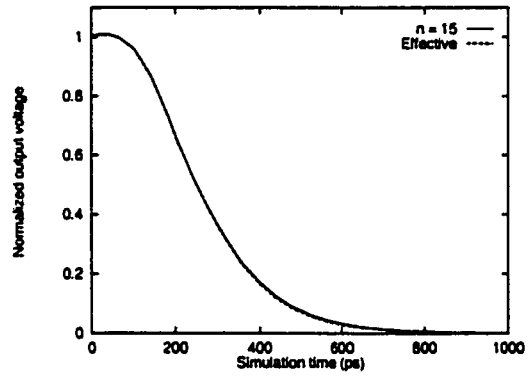
(a) SPICE simulation with $n = 3$ versus the effective load model



(b) SPICE simulation with $n = 5$ versus the effective load model



(c) SPICE simulation with $n = 10$ versus the effective load model



(d) SPICE simulation with $n = 15$ versus the effective load model

Figure 3.8: Comparison of the effective load model with SPICE for a distributed RC line, $R = 500\,\Omega$ and $C = 0.2\,\text{pF}$ with $n = 3$, 5, 10, and 15, respectively.

of lumped RLC elements as shown in Figure 3.9(a). In order to analyze the timing and voltage characteristics of a CMOS logic gate driving an inductive interconnect line, a distributed RLC line can be approximated by an effective load resistance, inductance, and capacitance as shown in Figure 3.9(b).

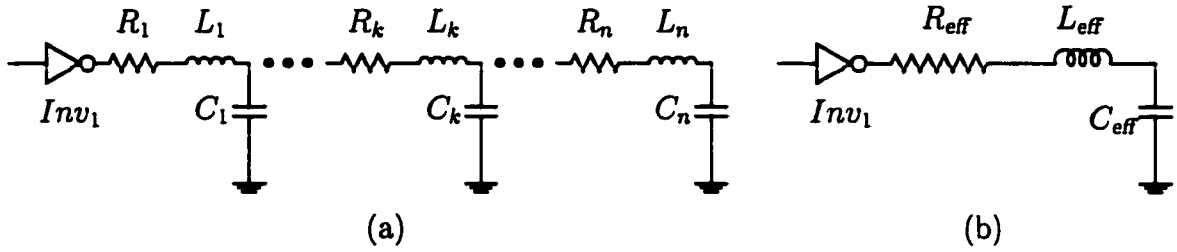


Figure 3.9: An inductive interconnect line, (a) a distributed RLC line approximated by n sections of lumped elements, (b) the effective load impedance R_{eff}, L_{eff} and C_{eff}.

A uniformly distributed RLC line is also assumed in the development of an effective load impedance. If the number of sections n is greater than two, the effective load resistance, inductance, and capacitance can be determined from (3.13), (3.14), and (3.15), respectively, which are based on an $L2$ circuit model as shown in Figure 3.4(b).

The effective load impedance shown in Figures 3.10 and 3.11 is determined from the conditions of $\sqrt{LC} = RC$, $\sqrt{LC} = 2.0\,RC$, $\sqrt{LC} = 3.0\,RC$, and $\sqrt{LC} = 4.0\,RC$, respectively. Note that when the operating frequency is close to $\omega_{LC} = \frac{1}{\sqrt{LC}}$, the effective load inductance increases significantly. However, if the operating frequency is comparable to ω_{LC}, the characteristics of a signal propagating along an inductive on-chip interconnection can be modeled by a TEM or quasi-TEM wave, requiring the interconnection to be modeled as a transmission line [64]. If the operating frequency is close to ω_{LC}, the effective load impedance is

Table 3.2: Analytical expressions characterizing the effective load impedance of a distributed RC line

No. of sections	Analytical Expressions
$n = 1$	$R_{\text{eff}}(\omega) = Req : RLC - 1a$ (3.10) $L_{\text{eff}}(\omega) = L(\omega)eq : RLC - 1b$ (3.11) $C_{\text{eff}}(\omega) = Ceq : RLC - 1c$ (3.12)
$n \geq 2$ $\omega < \frac{1}{\sqrt{LC}}$	$R_{\text{eff}}(\omega) = R_1 + \frac{R_2}{(R_2\omega C_1)^2 + (\omega^2 L_2(\omega)C_1 - \frac{C_1+C_2}{C_2})^2}$ (3.13) $L_{\text{eff}}(\omega) = L_1(\omega) + \frac{L_2(\omega)}{(R_2\omega C_1)^2 + (\omega^2 L_2(\omega)C_1 - \frac{C_1+C_2}{C_2})^2}$ $\frac{C_2 + 2C_1}{C_2}$ (3.14) $C_{\text{eff}}(\omega) = \frac{(\omega R_2 C_1)^2 + (\omega^2 L_2(\omega)C_1 - \frac{C_1+C_2}{c_2})^2}{(\omega R_2 C_1)^2 + \frac{(C_1+C_2)C_1}{C_2^2} + (\omega^2 L_2(\omega)C_1)^2} C_1$ (3.15)
$\omega \gtrapprox \frac{1}{\sqrt{LC}}$	$R_{\text{eff}}(\omega) = \sqrt{\frac{L}{C}}$ (3.16) $L_{\text{eff}}(\omega) = 0.0$ (3.17) $C_{\text{eff}}(\omega) = \frac{2L}{R}\sqrt{\frac{C}{L}}$ (3.18)

approximately equal to the characteristic impedance of the transmission line [84],

$$Z_{\text{eff}} = Z_o = \left[\frac{L}{C}\left(1+\frac{R}{j\omega L}\right)\right]^{\frac{1}{2}} \approx \sqrt{\frac{L}{C}}\left(1-j\frac{R}{2\omega L}\right). \tag{3.19}$$

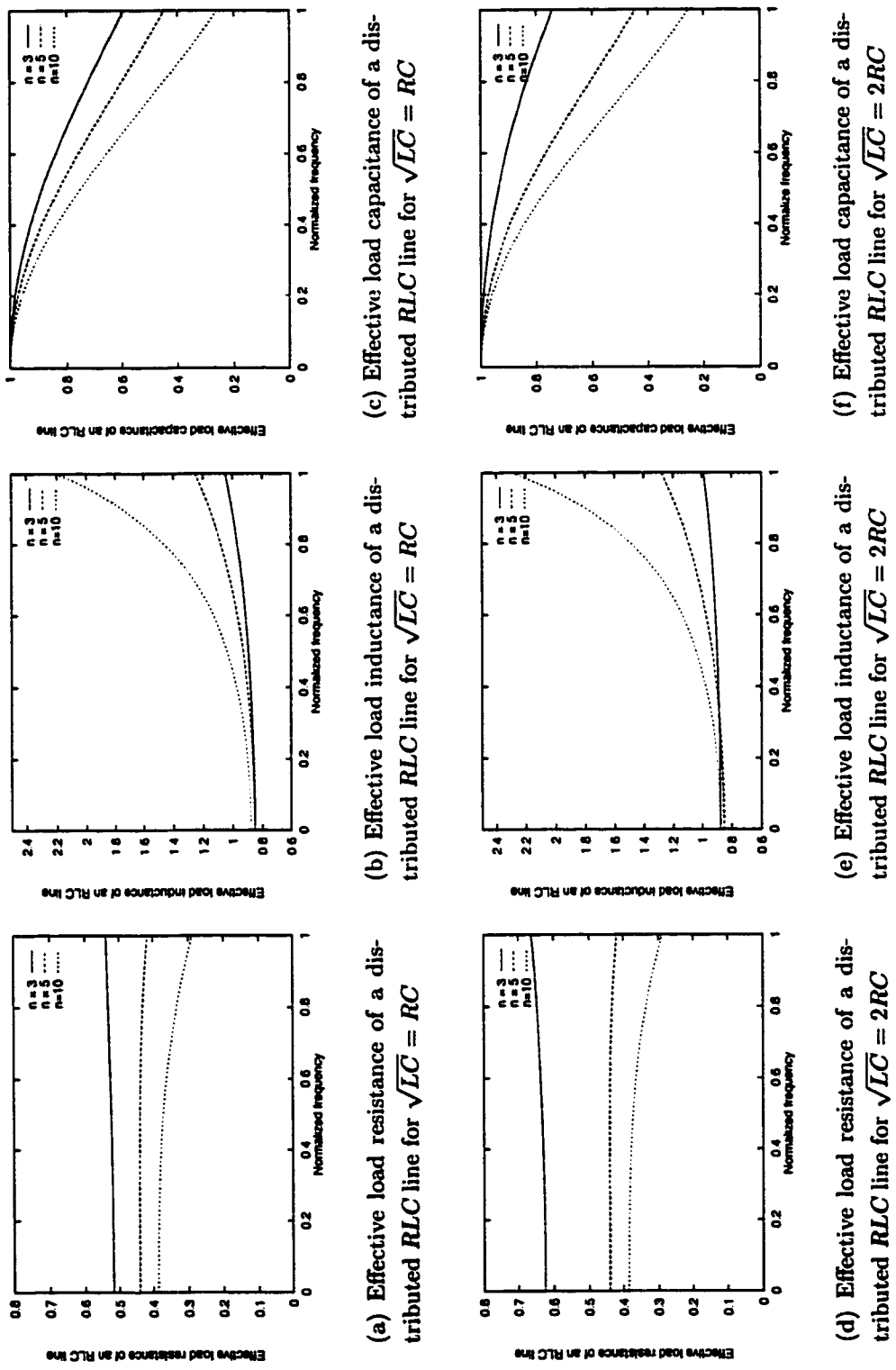
Following the same procedure as in the previous discussion of an RC line, the effective load inductance can be determined as

$$L_{\text{eff}} = \left[A_0 L_{\text{eff}}(0) + \sum_{\substack{m=2k+1 \\ k=0}}^{k=4\text{ or }7} A_m L_{\text{eff}}(m\omega_o)\right]\left(A_0 + \sum_{\substack{m=2k+1 \\ k=0}}^{k=4\text{ or }7} A_m\right)^{-1}. \tag{3.20}$$

The effective load resistance and capacitance are determined by the same formula as (3.8) and (3.9); however, the frequency dependence of the effective load impedance is different from a distributed RC line.

Note that there is a non-convergence problem as the operating frequency becomes close to ω_{LC} as the number of sections increases as shown in Figures 3.10 and 3.11. There is also a discontinuity in the expressions used to determined the effective load impedance (the resistance, inductance, and capacitance). If the input transition is short, the effective inductive load may exceed the total line inductance if (3.20) is used, as shown in Figures 3.10 and 3.11. The effective resistive, capacitive, and inductive load impedance cannot exceed the total line resistance, capacitance, and inductance, respectively. Therefore, the effective resistive, capacitive, and inductive load impedance models are modified, respectively, as

$$R_{\text{eff}} = \min\left(\left[A_0 R_{\text{eff}}(0) + \sum_{\substack{m=2k+1 \\ k=0}}^{k=4\text{ or }7} A_m R_{\text{eff}}(m\omega_o)\right]\left(A_0 + \sum_{\substack{m=2k+1 \\ k=0}}^{k=4\text{ or }7} A_m\right)^{-1}, R\right), \tag{3.21}$$



(a) Effective load resistance of a distributed RLC line for $\sqrt{LC} = RC$

(b) Effective load inductance of a distributed RLC line for $\sqrt{LC} = RC$

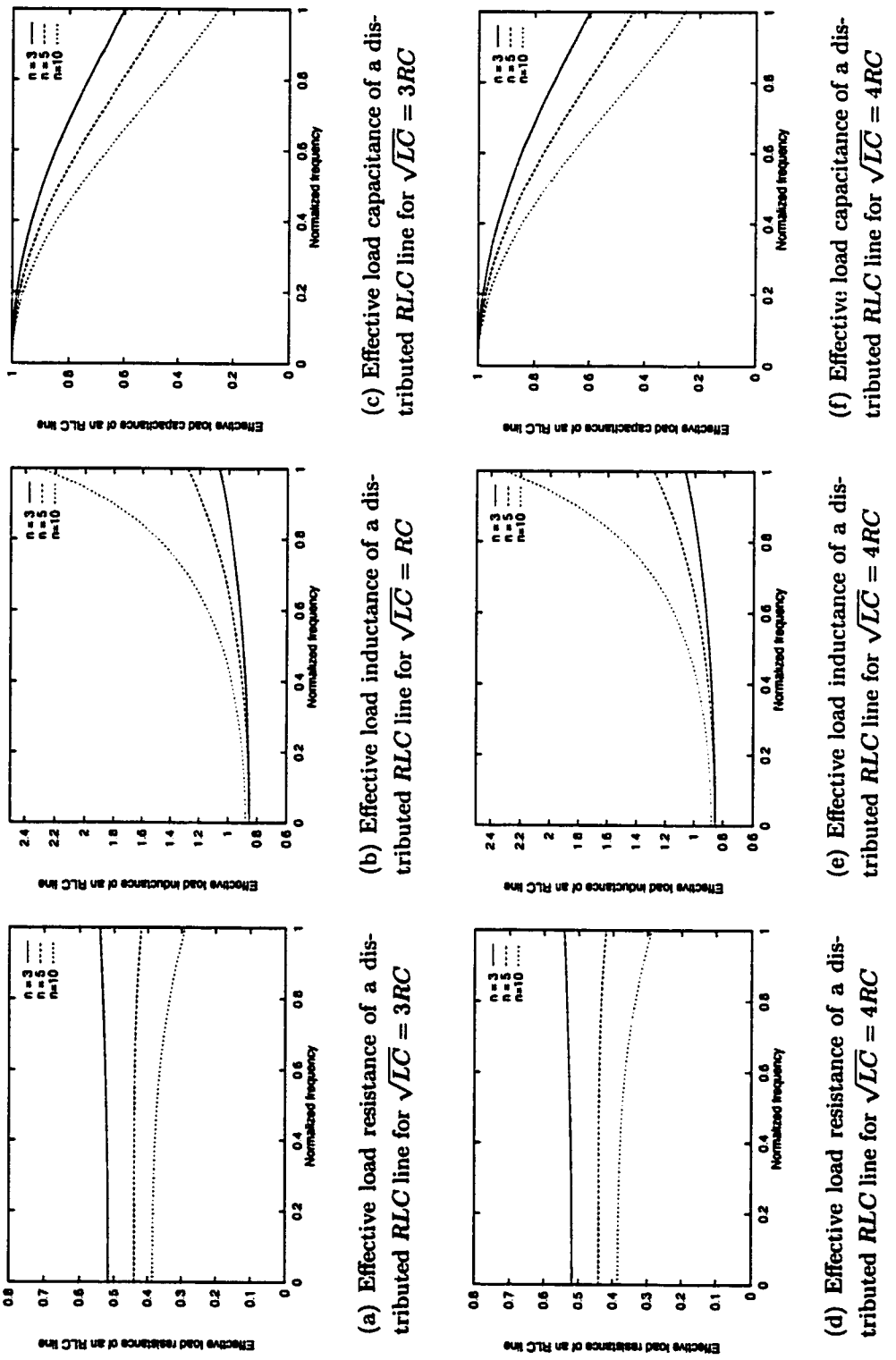
(c) Effective load capacitance of a distributed RLC line for $\sqrt{LC} = RC$

(d) Effective load resistance of a distributed RLC line for $\sqrt{LC} = 2RC$

(e) Effective load inductance of a distributed RLC line for $\sqrt{LC} = 2RC$

(f) Effective load capacitance of a distributed RLC line for $\sqrt{LC} = 2RC$

Figure 3.10: The effective load impedance of a uniform distributed RLC with $\sqrt{LC} = RC$ and $2RC$, respectively. The frequency is normalized to $\omega_{LC} = \frac{1}{\sqrt{LC}}$.



(a) Effective load resistance of a distributed RLC line for $\sqrt{LC} = 3RC$

(b) Effective load inductance of a distributed RLC line for $\sqrt{LC} = RC$

(c) Effective load capacitance of a distributed RLC line for $\sqrt{LC} = 3RC$

(d) Effective load resistance of a distributed RLC line for $\sqrt{LC} = 4RC$

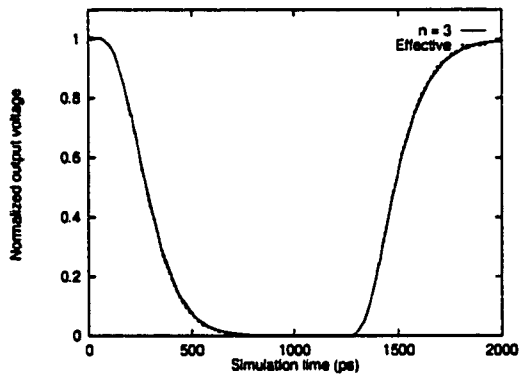
(e) Effective load inductance of a distributed RLC line for $\sqrt{LC} = 4RC$

(f) Effective load capacitance of a distributed RLC line for $\sqrt{LC} = 4RC$

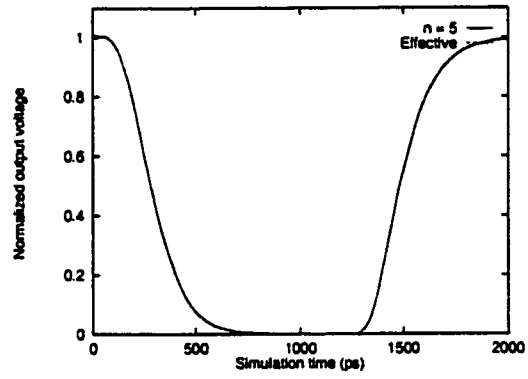
Figure 3.11: The effective load impedance of a uniform distributed RLC with $\sqrt{LC} = 3RC$ and $4RC$, respectively. The frequency is normalized to $\omega_{LC} = \frac{1}{\sqrt{LC}}$.

$$L_{\text{eff}} = \min\left(\left[A_0 L_{\text{eff}}(0) + \sum_{\substack{m=2k+1 \\ k=0}}^{k=4\text{ or }7} A_m L_{\text{eff}}(m\omega_o)\right]\left(A_0 + \sum_{\substack{m=2k+1 \\ k=0}}^{k=4\text{ or }7} A_m\right)^{-1}, L\right), \tag{3.22}$$

$$C_{\text{eff}} = \min\left(\left[A_0 C_{\text{eff}}(0) + \sum_{\substack{m=2k+1 \\ k=0}}^{k=4\text{ or }7} A_m C_{\text{eff}}(m\omega_o)\right]\left(A_0 + \sum_{\substack{m=2k+1 \\ k=0}}^{k=4\text{ or }7} A_m\right)^{-1}, C\right). \tag{3.23}$$



(a) SPICE simulation with $n = 3$ versus the effective load model

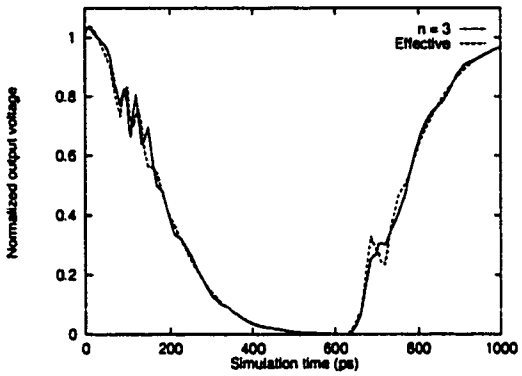


(b) SPICE simulation with $n = 5$ versus the effective load model

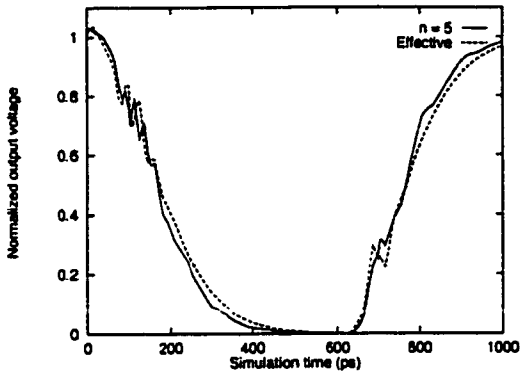
Figure 3.12: Comparison of the effective load model with SPICE for a distributed *RLC* line with $R = 45.0\,\Omega$, $L = 1.0\,\text{nH}$, and $C = 0.5\,\text{pF}$ with $n = 3$ and 5.

The waveforms derived from SPICE simulations based on an effective load resistance, inductance, and capacitance determined from (3.21), (3.22), and (3.23), respectively, are compared to the waveforms derived from a distributed *RLC* line model as shown in Figures 3.12 and 3.13. Note that the voltage waveform based on an effective load resistance, inductance, and capacitance is almost the same as the waveform based on a distributed *RLC* line model.

Although the effective *RC* or *RLC* impedance is based on an assumption of a uniformly distributed *RC* or *RLC* line, this method can also be applied to a



(a) SPICE simulation with $n = 3$ versus the effective load model



(b) SPICE simulation with $n = 5$ versus the effective load model

Figure 3.13: Comparison of the effective load model with SPICE for a distributed RLC line with $R = 45.0\,\Omega$, $L = 2.0\,\text{nH}$, and $C = 1.0\,\text{pF}$ with $n = 3$ and 5.

nonuniformly distributed RC or RLC line. Knowing the relative ratio of the interconnect impedance associated with each section of a nonuniformly distributed RC or RLC line, (3.6) and (3.7) [or (3.13), (3.14), and (3.15)] can also be used to determined the effective load impedance based on an $L2$ circuit model and applying a recursive calculation, as shown in Figure 3.4.

3.4 Summary

A Fourier analysis of typical on-chip signals in CMOS integrated circuits has been presented in this chapter. The on-chip signals can be approximated by a Fourier series up to the 15th harmonic component. The effective load impedance of a distributed RC and RLC line driven by a CMOS logic gate has been developed based on a Fourier analysis of the on-chip signals. The voltage waveform based on the effective load impedance model has been shown to be quite similar to the voltage waveform of a distributed RC and RLC line.

Chapter 4

A CMOS Logic Gate Driving a Resistive Interconnect

4.1 Introduction

In order to reduce design cycles, CMOS digital integrated circuits are often synthesized at the gate and/or cell level. The performance of the logic gates and cells (standard cell library components) are precharacterized to simplify the analysis process, including the propagation delay of a CMOS logic gate/cell for static timing analysis and short-circuit power dissipation for power estimation at the system level. The delay and power characteristics of a CMOS logic gate/cell are often described as a function of the input-signal transition time, the size of MOS transistors, and the load condition.

As integrated circuit technologies continue to improve, the feature size of MOS transistors and interconnect lines has decreased. Since the chip size and the integration density have increased dramatically, the average interconnect length has not scaled down with feature size but remains long relative to other on-chip geometries to carry signals within a chip. Therefore, the parasitic interconnect resistance has increased significantly due to technology scaling. If the interconnect resistance is comparable to the effective output resistance of a CMOS logic gate, the inter-

connect must be modeled as a resistive-capacitive load [74]. Furthermore, the interconnect parasitic capacitance does not decrease with scaling due to fringing fields between neighboring interconnections. If the length of an interconnect line increases linearly, the interconnect impedance increases quadratically [14] due to a linear increase in both the interconnect capacitance and resistance. Therefore, the effect of the *RC* interconnect impedance has become a significant portion of the overall propagation delay.

Repeater insertion techniques [76, 85, 86] are widely used to reduce the effect of the *RC* interconnect impedance and thereby improve circuit performance. Resistive interconnect may degrade the signal quality due to the nondigital behavior of the *RC* load, affecting waveform shapes of on-chip signals and causing additional short-circuit power [47, 80, 87], as well as power dissipated by the interconnect resistance. Therefore, in order to predict circuit performance at the system level, the propagation delay, transient power consumption, and signal quality should be accurately characterized.

The propagation delay model based on [79] and [80] is not physically intuitive, which involves curve fitting techniques. The analytical model presented in [79] and [80] does not explicitly consider the device parameters and is only applicable to small load conditions. The MOS transistors are assumed to solely operate in the linear region and are modeled as a linear resistor in [74], neglecting the nonlinear behavior of the MOS transistors.

In this chapter, an extension of previous work [77, 88] is presented, in which the interconnect is modeled as a lumped *RC* load. The more accurate nth power law model is used to characterize the deep submicrometer MOS transistors. Analytical expressions characterizing the propagation delay of both fast and slow ramp input

signals are presented. The waveform shape of the output voltage of a CMOS inverter is characterized for a fast ramp input signal. The interconnect resistance shields the load capacitance when the MOS transistor operates in the saturation region as compared to a purely capacitive load [79]. The signal quality is also degraded by the interconnect resistance, causing additional short-circuit power to be dissipated by the following logic stage. Analytical equations describing both the short-circuit and resistive power consumption are derived based on the load conditions and the input waveform shape. The accuracy of these analytical equations is compared with SPICE simulation. The waveform of the estimated output voltage based on these analytical equations is quite close to SPICE for fast ramp input signals. The accuracy of the estimated propagation delay for both fast ramp and slow ramp input signals is within 7% as compared to SPICE simulation.

The analytical equations describing the propagation delay of a CMOS inverter driving a resistive-capacitive load for both fast and slow ramp input signals, and the close form expressions characterizing the output voltage of a CMOS inverter for a fast ramp input signal are presented in Section 4.2. The effects of interconnect resistance on the propagation delay and short-circuit power dissipation of a CMOS inverter are discussed in Section 4.3. Short-circuit power and the power dissipated by the resistive interconnect are discussed in Section 4.4. The application of these analytical equations to circuit analysis is presented in Section 4.5, followed by some concluding remarks in Section 4.6.

4.2 Output Voltage and Propagation Delay

The propagation delay of a CMOS inverter depends on the load conditions, device parameters, and input transition times. In this section, the characteristics

of a CMOS inverter driving a resistive-capacitive load is described based on the nth power law model and input slew rate. Close form expressions characterizing the output voltage of a CMOS inverter are derived in Section 4.2.1 under an assumption of a fast ramp input signal. The temporal properties of a CMOS inverter are discussed in Section 4.2.2 for a fast ramp input signal. The propagation delay of a slow ramp input signal is discussed in Section 4.2.3.

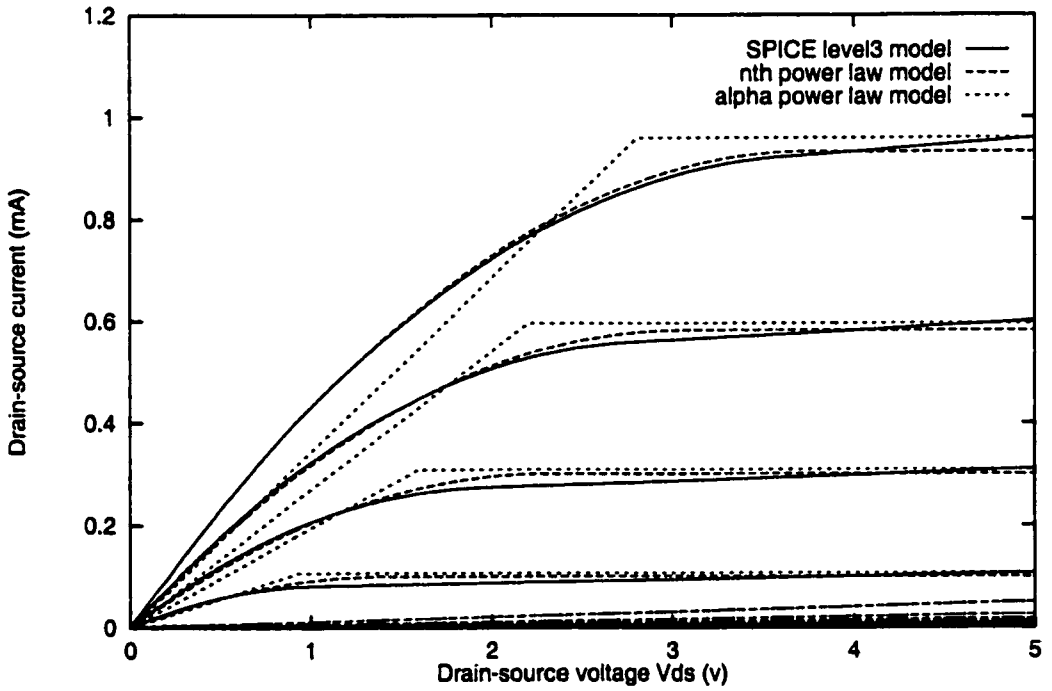


Figure 4.1: Comparison between the alpha power law model, the nth power law model, and SPICE for a 0.5 μm NMOS transistor.

The comparison among the alpha power law model [52], the nth power law model [41], and SPICE [49] is shown in Figure 4.1. The nth power law model is more accurate than the alpha power law model in the linear region and in determining the drain-to-source saturation voltage while avoiding any discontinuity between the linear and saturation regions.

4.2.1 Waveform of the Output Voltage

A circuit diagram of a CMOS inverter driving a lumped *RC* load is shown in Figure 4.2. R and C are the load resistance and capacitance, respectively. The input is assumed to be a rising ramp signal, defined as

$$V_{in}(t) = \frac{t}{\tau_r} V_{dd} \qquad \text{for} \qquad 0 \leq t \leq \tau_r, \tag{4.1}$$

where τ_r is the input transition time. The initial state of both V_o and V_1 are V_{dd}, therefore the PMOS transistor is ON and the NMOS transistor is OFF. No current flows through the PMOS transistor because the drain-to-source voltage is zero.

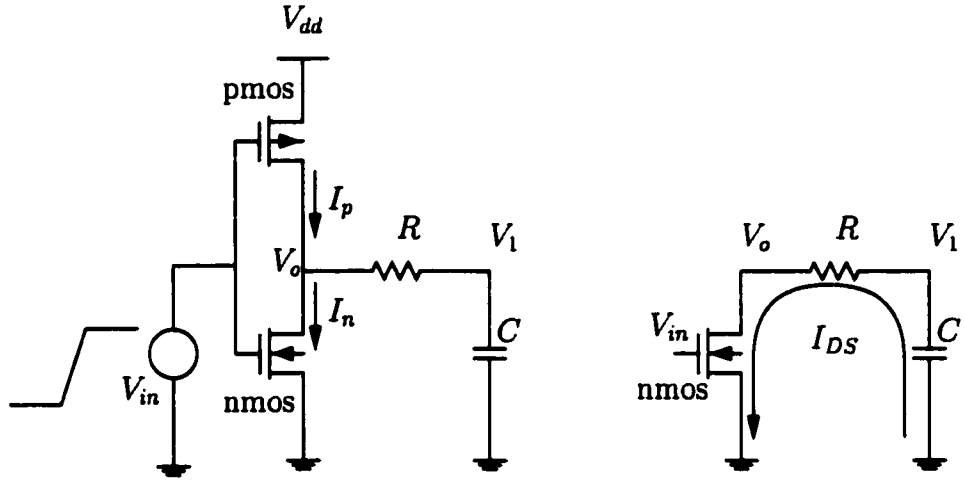


Figure 4.2: A CMOS inverter driving a resistive-capacitive load

The output voltage of a CMOS inverter, *i.e.*, V_o as shown in Figure 4.2, is based on the nth power law model, the load conditions, and a fast ramp input signal. The effect of the PMOS transistor is neglected based on an assumption of a fast ramp input signal, where the input exceeds one-third of the output slope [69]. This assumption is not valid if the input is slow as compared to the output signal.

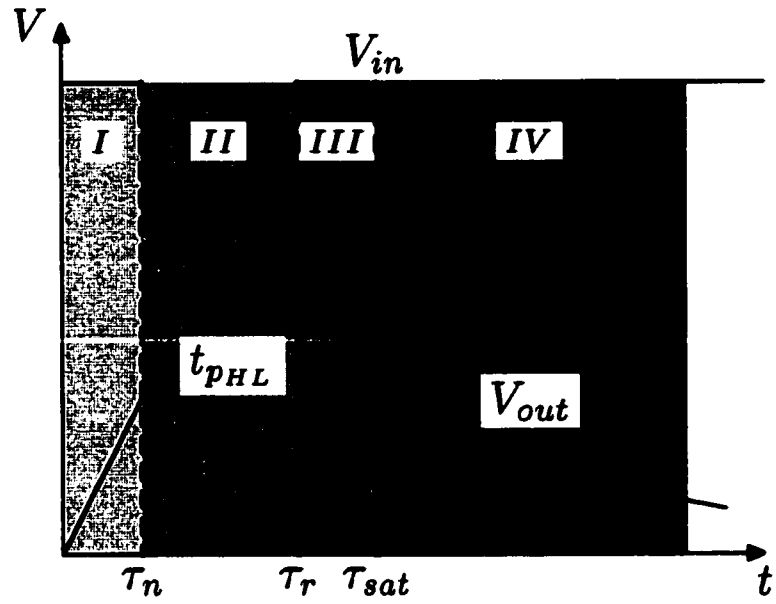


Figure 4.3: Operating regions of an NMOS transistor during the high-to-low output transition.

The regions of inverter operation are illustrated in Figure 4.3. The relations among V_o, V_1, and I_{DS} shown in Figure 4.2 are

$$V_1 = V_o + RI_{DS}, \tag{4.2}$$

$$C\frac{dV_1}{dt} = -I_{DS}. \tag{4.3}$$

Before the input voltage reaches V_{TN}, the NMOS transistor is OFF and no current will flow. Therefore, the output voltage V_o remains at V_{dd}, *i.e.*, the NMOS transistor operates in region I as shown in Figure 4.3.

Once the input voltage reaches V_{TN}, the NMOS transistor turns ON and starts to operate in the saturation region. Once I_n exceeds I_p, V_o drops below the initial voltage V_{dd}. The output voltage satisfies the following differential equation,

$$C\frac{dV_o}{dt} + RC\frac{dI_{DS}}{dt} = -I_{DS}. \tag{4.4}$$

Substituting for I_{DS}, the solution of V_o in region II is

$$V_o(t) = V_{dd} - \frac{B_n V_{dd}^n \tau_r}{C} \frac{1}{n+1} (\frac{t}{\tau_r} - \nu_T)^{n+1} - RB_n V_{dd}^n (\frac{t}{\tau_r} - \nu_T)^n \text{ for } \tau_n \leq t \leq \tau_r, \tag{4.5}$$

where $\nu_T = V_{TN}/V_{dd}$ and τ_n is the time when the input voltage reaches V_{TN}, $\tau_n = \nu_T \tau_r$. At $t = \tau_r$, the output voltage is

$$V_o(\tau_r) = V_{dd} - \frac{B_n V_{dd}^n \tau_r}{C} \frac{1}{n+1} (1 - \nu_T)^{n+1} - RB_n V_{dd}^n (1 - \nu_T)^n. \tag{4.6}$$

In region III, the transition of the fast input signal is completed and the input voltage is fixed at V_{dd}. The NMOS transistor remains in the saturation region. Therefore, the discharge current is the saturated drain-to-source current of the NMOS transistor, *i.e.*, a constant I_{DSAT}. Therefore, V_o is a linear function of time in region III. The output voltage is obtained based on the condition at $t = \tau_r$,

$$V_o(t) = V_{dd} - \frac{B_n V_{dd}^n}{C} (1 - \nu_T)^n (t - \frac{n + \nu_T}{1+n} \tau_r) - RB_n V_{dd}^n (1 - \nu_T)^n \text{ for } \tau_r \leq t \leq \tau_{sat}, \tag{4.7}$$

where τ_{sat} is the time when the NMOS transistor leaves the saturation region and is

$$\tau_{sat} = \frac{C}{B_n V_{dd}^n (1 - \nu_T)^n} (V_{dd} - K(V_{dd} - V_{TN})^m - RB_n V_{dd}^n (1 - \nu_T)^n) + \frac{n + \nu_T}{n+1} \tau_r. \tag{4.8}$$

At time τ_{sat}, the output voltage is equal to $V_{DSAT} = K(V_{dd} - V_{TN})^m$.

In region IV, the input voltage remains at V_{dd} and the output voltage falls below V_{DSAT}. Therefore, the NMOS transistor operates in the linear region and the drain-to-source current I_{DS} is

$$I_{DS} = B_n V_{dd}^n (1 - \nu_T)^n (2 - \frac{V_o}{K(V_{dd} - V_{TN})^m}) \frac{V_o}{K(V_{dd} - V_{TN})^m}. \tag{4.9}$$

Inserting I_{DS} in (4.9) into the differential equation (4.4), the solution for V_o in region IV becomes

$$\begin{aligned} V_o(t) &= \frac{2(V_{DSAT}+2RI_{DSAT})V_{DSAT}}{(V_{DSAT}-2RI_{DSAT})+V_C e^{\frac{t-\tau_{sat}}{\tau}}} \\ \tau &= \frac{(V_{DSAT}+2RI_{DSAT})C}{2I_{DSAT}} \qquad (t \geq \tau_{sat}), \end{aligned} \tag{4.10}$$

where $I_{DSAT} = B_n V_{dd}^n (1-\nu_T)^n$, $V_C = (V_{DSAT}+6RI_{DSAT})$, and τ is the time constant in region IV.

4.2.2 Propagation Delay of a Fast Ramp Signal

The propagation delay of a CMOS inverter is typically defined as the time from the 50% V_{dd} point of the input ($\frac{\tau_r}{2}$) to the 50% V_{dd} point of the output ($t_{0.5}$). The high-to-low propagation delay t_{pHL} of a CMOS inverter is approximated as

$$t_{pHL} = t_{0.5} - \frac{\tau_r}{2} = \frac{C}{I_{DSAT}}(\frac{V_{dd}}{2} - RI_{DSAT}) + (\frac{n+\nu_T}{n+1} - \frac{1}{2})\tau_r, \tag{4.11}$$

where $I_{DSAT} = B_n(V_{dd}-V_{TN})^n$.

Similarly, the low-to-high propagation delay of a CMOS inverter can be derived based on the time required to charge up the load capacitor. Note that there are two terms in the delay expression (4.11). The first term depends on the load condition, which is proportional to the load capacitance and the difference between $V_{dd}/2$ and RI_{DSAT}. The second term is input waveform dependent, which is proportional to the input transition time τ_r.

The output transition time can be approximated by the time $t_{0.9}$ when the output voltage V_o reaches $0.9V_{dd}$ point and the time $t_{0.1}$ when the output voltage V_o reaches $0.1V_{dd}$ point. $t_{0.9}$ can be obtained by using V_o expressed in (4.5) for region II,

$$V_{dd} - 0.9V_{dd} = \frac{B_n V_{dd}^n \tau_r}{C}\frac{1}{n+1}(\frac{t_{0.9}}{\tau_r} - \nu_T)^{n+1} + RB_n V_{dd}^n (\frac{t_{0.9}}{\tau_r} - \nu_T)^n. \tag{4.12}$$

The solution of $t_{0.9}$ can be obtained by using a Newton-Raphson iteration [89]. Two to four iterations are typically required to obtain a solution of $t_{0.9}$. An alternative method is to approximate $t_{0.9}$ by using (4.7),

$$t_{0.9} = \frac{C}{I_{DSAT}}(0.1V_{dd} - RI_{DSAT}) + \frac{n+\nu_T}{n+1}\tau_r. \tag{4.13}$$

Similarly, V_o in region IV is expressed in (4.10), permitting $t_{0.1}$ to be expressed as

$$t_{0.1} = \tau ln\frac{10V_AV_{DSAT} - V_BV_{dd}}{V_{dd}(V_{DSAT} + 6RI_{DSAT})} + \tau_{sat}, \tag{4.14}$$

where $V_A = 2(V_{DSAT} + 2RI_{DSAT})$ and $V_B = V_{DSAT} - 2RI_{DSAT}$.

If the input transition time is assumed to be similar to the output transition time, which is typical in practical VLSI circuits, τ_r can be expressed as

$$\tau_r = \frac{t_{0.1} - t_{0.9}}{0.8} = \frac{1}{0.8}[\tau ln\frac{10V_AV_{DSAT} - V_BV_{dd}}{V_{dd}(V_{DSAT} + 6RI_{DSAT})} + \frac{C}{I_{DSAT}}(0.9V_{dd} - V_{DSAT}]. \tag{4.15}$$

4.2.3 Propagation Delay of a Slow Ramp Signal

The analyses in sections 4.2.1 and 4.2.2 are based on an assumption of a fast ramp input signal, *i.e.*, the NMOS transistor remains in the saturation region before the input transition is completed. Therefore, the fast ramp condition can be quantified based on the previous analysis, *i.e.*, τ_r is compared to the time when the output signal reaches the saturated voltage, τ_{sat} in (4.8). If τ_r is greater than τ_{sat}, *i.e.*, the NMOS transistor enters the linear region before the input transition is completed, the input is treated as a slow ramp signal. A criterion for a fast ramp input signal is

$$\begin{aligned} f(\tau_r) &= \tau_{sat} - \tau_r \geq 0 \\ &= \frac{C}{B_nV_{dd}^n(1-\nu_T)^n}(V_{dd} - RB_nV_{dd}^n(1-\nu_T)^n - K(V_{dd} - V_{TN})^m) \\ &+ (\frac{n+\nu_T}{n+1} - 1)\tau_r \geq 0. \end{aligned} \tag{4.16}$$

Quantitatively, if $f(\tau_r) \geq 0$, the input is a fast ramp signal, otherwise, it is a slow ramp signal.

For a slow ramp input signal, when the input signal is greater than V_{TN}, the NMOS transistor is ON and starts operating in the saturation region. The output voltage can therefore be expressed as

$$V_o(t) = V_{dd} - \frac{B_n V_{dd}^n \tau_r}{C} \frac{1}{n+1} (\frac{t}{\tau_r} - \nu_T)^{n+1} - RB_n V_{dd}^n (\frac{t}{\tau_r} - \nu_T)^n \text{ for } \tau_n \leq t \leq \tau_{sat}. \tag{4.17}$$

τ_{sat} is the time when the NMOS transistor leaves the saturation region. In this case, however, τ_{sat} is calculated based on

$$V_{dd} - \frac{B_n V_{dd}^n \tau_r}{C} \frac{1}{n+1} (\frac{\tau_{sat}}{\tau_r} - \nu_T)^{n+1} - RB_n V_{dd}^n (\frac{\tau_{sat}}{\tau_r} - \nu_T)^n = K(\frac{\tau_{sat}}{\tau_r} V_{dd} - V_{TN})^m. \tag{4.18}$$

The solution of τ_{sat} can be obtained by using a Newton-Raphson iteration [89]. It typically requires two to four iterations to obtain a solution of τ_{sat}.

The time when the output voltage V_o reaches the 50% V_{dd} point can be approximated by using (4.17),

$$\frac{B_n V_{dd}^n \tau_r}{C} \frac{1}{n+1} (\frac{t_{0.5}}{\tau_r} - \nu_T)^{n+1} + RB_n V_{dd}^n (\frac{t_{0.5}}{\tau_r} - \nu_T)^n = \frac{V_{dd}}{2}. \tag{4.19}$$

In the aforementioned analysis of a slow ramp input signal, the effect of the PMOS transistor is neglected. In order to accurately estimate the propagation delay for a slow ramp input signal, some modifications are necessary. The high-to-low propagation delay is approximated as

$$t_{pHL} = \frac{\tau_r}{\tau_{sat}} (t_{0.5} - \frac{\tau_r}{2}), \tag{4.20}$$

where the ratio τ_r/τ_{sat} characterizes the degree to which the input signal deviates from a fast ramp input signal. Both $t_{0.5}$ and τ_{sat} can be obtained from (4.19) and (4.18). Therefore, the propagation delay for both fast ramp and slow ramp input signals are described analytically in (4.11) and (4.20), respectively.

4.3 Effects of Interconnect Resistance

The waveform shape at the output of a CMOS inverter as expressed in (4.11) is degraded with increasing interconnect resistance due to the $\frac{V_{dd}}{2} - RI_{DSAT}$ term in (4.11), where the output voltage decreases due to the RI_{DS} term when the NMOS transistor operates in the saturation region as compared to a capacitive load [41, 52]. Therefore, the interconnect resistance reduces the time during which an MOS transistor remains in the saturation region. This effect is called resistive shielding [79], where a portion of the load capacitance is shielded as the MOS transistor operates in the saturation region when the interconnect resistance is comparable to the effective output resistance of a CMOS logic gate.

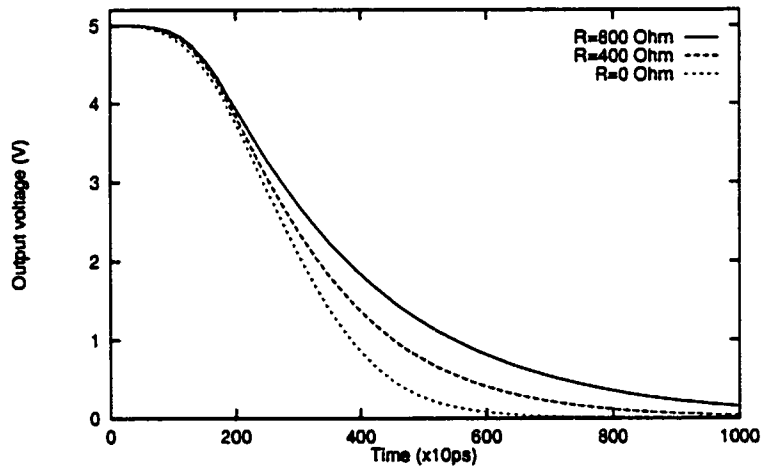


Figure 4.4: Effect of the interconnect resistance with $W_n = 3.6\,\mu$m, $W_p = 7.2\,\mu$m, $C_l = 1.5$ pF, and $\tau_r = 2$ ns.

The second effect of the interconnect resistance is the degraded waveform shape of the output voltage. If the interconnect resistance is comparable to the effective output resistance of a CMOS inverter, *i.e.*, $V_{DSAT} \approx RI_{SADT}$, the time constant τ in region IV when the MOS transistor operates in the linear region, can be

approximated as

$$\tau = \frac{3V_{DSAT}}{2I_{DSAT}}C. \tag{4.21}$$

The time constant τ increases by almost 50% than if the load is primarily capacitive [52]. Therefore, the signal quality has a deleterious effect on the following logic stage because the MOS transistors of the following stage cannot turn off quickly due to the slow transition time of the input signal, as shown in Figure 4.4. Extra short-circuit power and subthreshold current within the following logic stage occur. Therefore, it is important to include short-circuit power in the analysis of the total transient power consumption when the interconnect is modeled as a resistive-capacitive load.

4.4 Transient Power Consumption

Power consumption has become a primary design criterion in VLSI circuits. For a CMOS inverter driving a resistive-capacitive interconnect, there are three contributions, dynamic power dissipation, short-circuit power, and the power dissipated by the interconnect resistance, to the total transient power consumption.

The short-circuit power is often neglected since the dynamic power is assumed to be dominant [68]. The short-circuit power is strongly dependent upon the input waveform as well as the device parameters and the load conditions. The power dissipated by the interconnect resistance has emerged as an additional component in the total transient power consumption since the lossy characteristic of the interconnect resistance cannot be neglected.

Dynamic power is briefly discussed in Section 4.4.1. Analytical expressions describing both the short-circuit and the resistive power components are presented in Sections 4.4.2 and 4.4.3. These three components are included in the total transient power dissipation summarized in Section 4.4.4.

4.4.1 Dynamic Power

Dynamic power describes the energy required to charge and discharge a load capacitance. It is completely independent of the interconnect model and the device parameters. Dynamic power can be characterized by the well known expression,

$$P_{dy} = CV^2 f, \tag{4.22}$$

where C is the load capacitance, V is the swing of the voltage change, and f is the switching frequency of the inverter.

4.4.2 Short-Circuit Power

A DC path between V_{dd} and ground occurs when the input signal transitions from V_{TN} to $V_{dd} - V_{TP}$ (V_{TP} is the absolute value of the PMOS threshold voltage). Short-circuit current will flow through the PMOS transistor, turning off when the input signal transitions, thereby dissipating power.

In characterizing the short-circuit power, the NMOS transistor is assumed to operate in the saturation region during most of the time when the short-circuit

current flows. Based on this assumption, (4.5) is a valid estimate of the output voltage during the time when the short-circuit current flows. The short-circuit power during a high-to-low transition P_{scHL} is

$$P_{sc_{HL}} = fV_{dd}\int I_p(t)dt, \tag{4.23}$$

where f is the switching frequency of the inverter and I_p is the current through the PMOS transistor. The drain-to-source voltage of the PMOS transistor can be expressed as

$$V_{DSP} = \frac{B_n V_{dd}^{n_n}\tau_r}{C}\frac{1}{n_n+1}(\frac{t}{\tau_r} - \nu_{TN})^{n_n+1} + RB_n V_{dd}^{n_n}(\frac{t}{\tau_r} - \nu_{TN})^{n_n}, \tag{4.24}$$

where V_{DSP} is the absolute value of the drain-to-source voltage of the PMOS transistor and $\nu_{TN} = V_{TN}/V_{dd}$.

The PMOS transistor begins operating in the linear region when the input voltage is greater than V_{TN}, at a corresponding time τ_n. At the time τ_{off} when the input signal reaches $V_{dd} - V_{TP}$, the PMOS transistor is OFF. The time when the PMOS transistor enters the saturation region, *i.e.*, τ_{psat}, can be determined from

$$\begin{aligned} K_p(V_{dd} - \frac{\tau_{psat}}{\tau_r}V_{dd} - V_{TP})^{m_p} =& \frac{B_n V_{dd}^{n_n}\tau_r}{C}\frac{1}{n_n+1}(\frac{\tau_{psat}}{\tau_r} - \nu_{TN})^{n_n+1} \\ &+ RB_n V_{dd}^{n_n}(\frac{\tau_{psat}}{\tau_r} - \nu_{TN})^{n_n}. \end{aligned} \tag{4.25}$$

A solution of τ_{psat} can be obtained by applying the Newton-Raphson technique to (4.25) [89].

During the time interval from τ_n to τ_{psat}, the PMOS transistor operates in the linear region and $I_p(t)$ can be described as

$$I_p(t) = I_{DSATP}(2 - \frac{V_{DSP}}{V_{DSATP}})\frac{V_{DSP}}{V_{DSATP}}, \tag{4.26}$$

where

$$\begin{aligned} I_{DSATP} &= B_p(V_{dd} - \frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p}, \\ V_{DSATP} &= K_p(V_{dd} - \frac{t}{\tau_r}V_{dd} - V_{TP})^{m_p}, \end{aligned} \tag{4.27}$$

and $V_{dd}(1 - t/\tau_r)$ is the absolute value of the gate-to-source voltage of the PMOS transistor. The short-circuit power in this region can be calculated from

$$P_{sc_{HLI}} = fV_{dd}\int_{\tau_n}^{\tau_{psat}} I_p(t)dt. \tag{4.28}$$

This integral does not have an analytical solution after substituting (4.26) for $I_p(t)$. An approximation that τ_{psat} is close to τ_{off} is made in order to derive an analytical solution. This approximation is within 10% if the PMOS transistor remains saturated for a short time [90]. The approximate solution of the integral is

$$\begin{aligned} P_{sc_{HLI}} =& \frac{fB_pB_n\tau_r^2}{K_pC(n_n+1)}f(n_n+n_p+2-m_p)\beta(n_n+2,n_p+1-m_p) \\ &+ \frac{fB_pB_nR\tau_r}{K_p}f(n_n+n_p+1-m_p)\beta(n_n+1,n_p+1-m_p) \\ &- [\frac{fB_p{B_n}^2{\tau_r}^3}{{K_p}^2C^2V_{dd}(n_n+1)^2}f(2n_n+n_p+3-2m_p)\beta(2n_n+3,n_p+1-2m_p) \\ &+ 2\frac{fB_p{B_n}^2R{\tau_r}^2}{{K_p}^2C(n_n+1)}f(2n_n+n_p+2-2m_p)\beta(2n_n+2,n_p+1-2m_p) \\ &+ \frac{fB_p{B_n}^2R^2\tau_r}{{K_p}^2}f(2n_n+n_p+1-2m_p)\beta(2n_n+1,n_p+1-2m_p)], \end{aligned} \tag{4.29}$$

where $f(x)$ is

$$f(x) = (\frac{\tau_{psat}}{\tau_r}V_{dd} - V_{TN})^x, \tag{4.30}$$

and $\beta(x,y)$ is the Beta function.

During the time from τ_{psat} to τ_{off}, the PMOS transistor operates in the saturation region and $I_p(t)$ is

$$I_p(t) = B_p(V_{dd} - \frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p}. \tag{4.31}$$

Therefore, the second component of the short-circuit power from τ_{psat} to τ_{off} is

$$P_{sc_{HLII}} = fV_{dd}\int_{\tau_{psat}}^{\tau_{off}} I_p(t)dt = f\frac{B_p\tau_r V_{dd}}{n_p+1}(V_{dd} - \frac{\tau_{psat}}{\tau_r}V_{dd} - V_{TP})^{n_P+1}. \tag{4.32}$$

The total short-circuit power dissipated during the high-to-low transition is the summation of both (4.29) and (4.32),

$$P_{sc_{HL}} = P_{sc_{HLI}} + P_{sc_{HLII}}. \tag{4.33}$$

The short-circuit power dissipated during the low-to-high transition, *i.e.*, $P_{sc_{LH}}$, can be similarly obtained. The average short-circuit power dissipation is

$$P_{sc} = P_{sc_{HL}} + P_{sc_{LH}}. \tag{4.34}$$

The peak short-circuit current occurs during the time interval between τ_n and τ_{psat}. The time during which the peak current occurs is obtained by solving

$$I_p'(t_{peak}) = 0, \tag{4.35}$$

again using a Newton-Raphson iteration. The peak short-circuit current is

$$I_{peak} = I_p(t = t_{peak}). \tag{4.36}$$

However, based on the assumption that the peak current occurs near the middle of the input waveform for a balanced inverter [77, 88], the peak current can be obtained from (4.26) by substituting $t = \tau_r/2$,

$$I_{peak} = B_p(\frac{V_{dd}}{2} - V_{TP})^{n_p}(2 - \frac{V_{DP}}{K_p(\frac{V_{dd}}{2} - V_{TP})^{m_p}})\frac{V_{DP}}{K_p(\frac{V_{dd}}{2} - V_{TP})^{m_p}}, \tag{4.37}$$

where

$$V_{DP} = \frac{B_n V_{dd}^{n_n} \tau_r}{C} \frac{1}{n_n + 1} (\frac{1}{2} - \nu_{TN})^{n_n+1} + R B_n V_{dd}^{n_n} (\frac{1}{2} - \nu_{TN})^{n_n}. \quad (4.38)$$

Note that the peak current depends on both the input waveform shape and the load conditions.

Once I_{peak} is obtained, the short-circuit current $I_{sc}(t)$ can be approximated by a triangle [77, 88], permitting the short-circuit power of the high-to-low transition to be approximated by the product of the area of the triangle and V_{dd}, *i.e.*,

$$P_{sc_{HL}} = \frac{1}{2} I_{peak} (\tau_{off} - \tau_n) V_{dd} f, \quad (4.39)$$

where f is the switching frequency of the inverter. Similarly, the average short-circuit power during the low-to-high transition $P_{sc_{LH}}$ can also be derived from the peak short-circuit current.

4.4.3 Resistive Power Consumption

For resistive interconnect, additional power is dissipated by the interconnect resistance in addition to the power dissipated by the switching of the MOS transistors during the charging and discharging of the load capacitance. The current flowing through the interconnect resistance is identical to the charge/discharge current. An analytical expression characterizing the power dissipated by the interconnect resistance is based on an assumption of a fast ramp input signal. The resistive power consumption of the high-to-low transition is expressed as

$$P_{r_{HL}} = f \int R I_{DS}^2(t) dt, \quad (4.40)$$

where f is the switching frequency of the inverter.

For a high-to-low transition as shown in Figure 4.3, there is no discharge current in region I. In region II, the discharge current is equal to the NMOS

saturation current. The power dissipated by the load resistance during this time period is

$$P_{r_I} = f\int_{\tau_n}^{\tau_r} R(B_n(\frac{t}{\tau_r}V_{dd} - V_{TN})^n)^2 dt = \frac{fRB_n{}^2V_{dd}{}^{2n}\tau_r}{2n+1}(1-\nu_T)^{2n+1}. \quad (4.41)$$

In region III, *i.e.*, from τ_r to τ_{sat}, the NMOS transistor operates in the saturation region with the input signal at V_{dd}. The discharge current is a constant and the resistive power consumption is

$$P_{r_{II}} = fRB_n{}^2V_{dd}{}^2(1-\nu_T)^{2n}(\tau_{sat} - \tau_r). \quad (4.42)$$

In region IV, the NMOS transistor operates in the linear region and the equation characterizing the discharge current is fairly complicated. In order to develop a tractable analytical expression for the resistive power dissipated during this period, the assumption,

$$\langle I_{DS}\rangle^2 = \langle I_{DS}^2\rangle, \quad (4.43)$$

is made. $\langle I_{DS}\rangle$ is the average current and $\langle I_{DS}^2\rangle$ is the time average of I_{DS}^2. $\langle I_{DS}\rangle$ is defined as

$$\langle I_{DS}\rangle = \frac{1}{t_{0.1} - \tau_{sat}}\int_{\tau_{sat}}^{t_{0.1}} I_{DS}(t)dt. \quad (4.44)$$

This equation can be solved by using (4.9) and (4.10). The results of $\langle I_{DS}\rangle$ is

$$\langle I_{DS}\rangle = \frac{I_{DSAT}V_A}{V_{DSAT}}\tau[\frac{t_{0.1}-\tau_{sat}}{\tau} - ln(2 + \frac{V_C}{V_{DSAT}}e^{\frac{t_{0.1}-\tau_{sat}}{\tau}}) + ln(2+\frac{V_C}{V_{DSAT}})], \quad (4.45)$$

where V_C and V_A are defined in (4.10) and (4.14), respectively. I_{DSAT} and V_{DSAT} are defined in (4.10) and (4.8), respectively. The power dissipated in this region is

$$P_{r_{III}} = R\langle I_{DS}\rangle^2 f. \quad (4.46)$$

The total power dissipated by the load resistance during the high-to-low transition is

$$P_{r_{HL}} = P_{r_I} + P_{r_{II}} + P_{r_{III}}. \tag{4.47}$$

Similarly, the resistive power consumption of the low-to-high transition P_{rLH} can also be obtained. The average power dissipated by the resistive load is

$$P_r = P_{r_{HL}} + P_{r_{LH}}. \tag{4.48}$$

4.4.4 Total Power Dissipation

The total average power dissipated during the time when the CMOS inverter switches is the summation of the dynamic power, short-circuit power, and resistive power,

$$P_{total} = P_{dy} + P_{sc} + P_r. \tag{4.49}$$

This expression provides a closed form solution based on the input transition time and load condition to estimate the total transient power dissipation, including the short-circuit power and resistive power components.

4.5 Application to Circuit Analysis

The device parameters of the nth power law model of a 0.5 μm MOS transistors with minimum size $W_n = 0.9\,\mu$m and $W_p = 1.8\,\mu$m are listed in Table 4.1. These parameters are extracted based on I-V data of the minimum size MOS transistors. The effect of velocity saturation is represented by n, whose value is between one and two. If $n = 2$, the nth power law model is the same as the classical Shichman-Hodges I-V model [46].

Table 4.1: Model parameters of 0.5 μm MOS transistors

Parameters	NMOSFET	PMOSFET
B_n (mA/V)	0.131398	0.087247
n	1.286399	1.683236
K	0.961756	1.351647
m	0.716586	0.726712
V_{th} (V)	0.707754	-0.915643

Close form expressions of the output voltage for a fast ramp input signal, as discussed in Section 4.2.1, are compared with SPICE simulation. Analytical expressions of the high-to-low propagation delay for both a fast ramp and slow ramp input signal, expressed in (4.11) and (4.20), respectively, are evaluated for different transistor sizes, input transition times, and load conditions.

4.5.1 Output Voltage of a CMOS Inverter

The definition of a fast ramp input signal is based on the relationship between the input transition time τ_r and the time τ_{sat} [as defined in (4.8)]. There are two terms in the expression of τ_{sat}. The first term is proportional to the load capacitance and decreases as the load resistance increases. The second term is proportional to the input transition time τ_r. To determine whether an input is a fast ramp signal, the input transition time τ_r is not the only concern because the decision also depends upon the load conditions. Even for the same input transition time τ_r, different conclusions exist under different load conditions.

For a fast ramp input signal, the output voltage of a CMOS inverter based on these analytical equations is compared with SPICE simulation. The results are shown in Figure 4.5. In Figure 4.5(a), the load condition is $R = 100\ \Omega$, $C = 0.5$ pF, input transition time $\tau_r = 1$ ns, and $W_n = 0.9\ \mu$m. For this case,

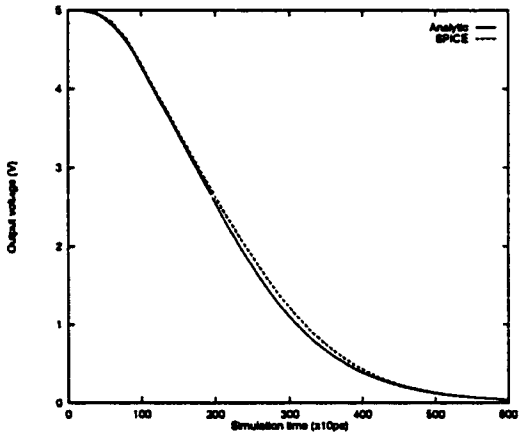
$\tau_{vdsat} = 1.89$ ns, which is greater than τ_r, therefore the input is considered to be a fast ramp signal. For a large resistive load, the resulting simulation is depicted in Figure 4.5(b), while the simulation in which the load is a large capacitance is illustrated in Figure 4.5(c). For a medium resistive and capacitive load, the resulting simulation is shown in Figure 4.5(d).

Note that the output voltage based on the analytical expression is quite close to the SPICE simulation of each condition. The error of the propagation delay can be found in Table 4.2. These analytical expressions can therefore be used to approximate the output voltage for a fast ramp input signal. These expressions avoid the computational complexity required by SPICE while providing intuition into the effects of the physical parameters and related circuit sensitivities.

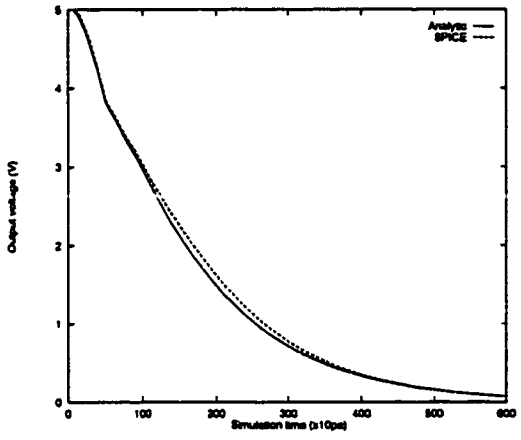
4.5.2 Propagation Delay Comparison with SPICE

The high-to-low propagation delay of a CMOS inverter driving a resistive-capacitive load is shown in Table 4.2 under a variety of transistor sizes, input transition times, and load conditions. The geometric width of both the NMOS and PMOS transistors are listed in the first two columns. The load resistance, load capacitance, and rise time of the input signal, respectively, are listed in the following three columns. Results of the SPICE simulation are listed in column six and in the seventh column, the high-to-low propagation delay estimated from (4.11) or (4.20) are listed. Whether the input is a fast ramp signal and the error of the delay as compared to SPICE simulation are listed in the final two columns.

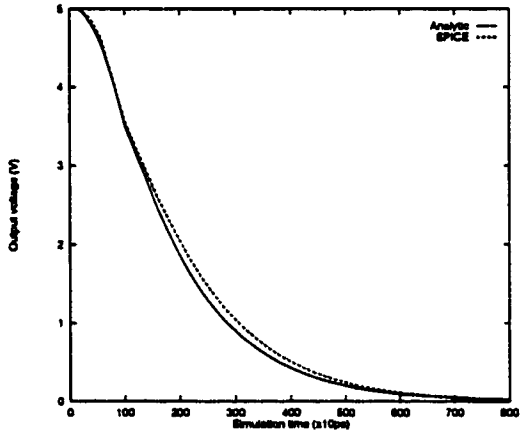
The size of the NMOS transistor varies from $0.9\,\mu$m to $9.0\,\mu$m and the input transition time ranges from 0.5 ns to 2.0 ns. For a variety of load conditions, the error of the high-to-low propagation delay is less than 7% as compared to SPICE simulation. Note in particular the case of $W_n = 0.9\,\mu$m and $R = 300\,\Omega$ where



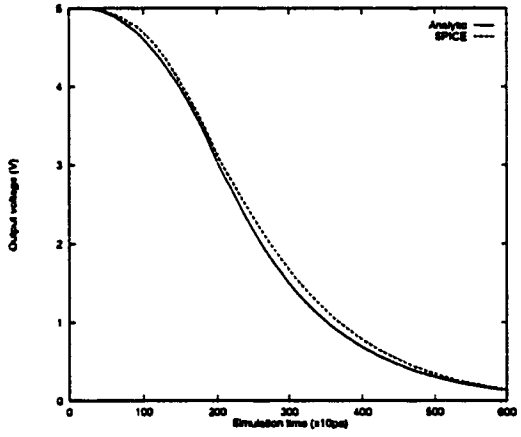
(a) $W_n = 0.9\,\mu\text{m}$, $W_p = 1.8\,\mu\text{m}$, $R = 100\,\Omega$, $C = 0.5\,\text{pF}$, and $\tau_r = 1\,\text{ns}$.



(b) $W_n = 0.9\,\mu\text{m}$, $W_p = 1.8\,\mu\text{m}$, $R = 1000\,\Omega$, $C = 0.5\,\text{pF}$, and $\tau_r = 0.5\,\text{ns}$.



(c) $W_n = 9.0\,\mu\text{m}$, $W_p = 18.0\,\mu\text{m}$, $R = 100\,\Omega$, $C = 5\,\text{pF}$, and $\tau_r = 2.0\,\text{ns}$.



(d) $W_n = 3.6\,\mu\text{m}$, $W_p = 7.2\,\mu\text{m}$, $R = 200\,\Omega$, $C = 2\,\text{pF}$, and $\tau_r = 1.0\,\text{ns}$.

Figure 4.5: Comparison of the output voltage for a fast ramp input signal with SPICE simulation.

Table 4.2: High-to-low propagation delay

Transistor size					t_{pHL} (ns)			
W_n (μm)	W_p (μm)	R (Ω)	C (pF)	τ_r (ns)	SPICE	Analytic	Fast Ramp	Error (%)
0.9	1.8	100	0.5	0.5	1.51	1.47	Yes	2.6
0.9	1.8	500	0.5	0.5	1.32	1.27	Yes	3.7
0.9	1.8	1000	0.5	0.5	1.09	1.03	Yes	5.5
3.6	7.2	100	2.0	0.5	1.35	1.32	Yes	2.2
3.6	7.2	500	2.0	0.5	0.57	0.54	Yes	5.3
3.6	7.2	1000	2.0	0.5	0.17	0.16	No	5.8
9.0	18.0	100	5.0	0.5	1.12	1.08	Yes	3.8
9.0	18.0	200	5.0	0.5	0.57	0.54	Yes	5.5
9.0	18.0	300	5.0	0.5	0.24	0.23	No	4.2
0.9	1.8	100	0.5	1.0	1.58	1.53	Yes	3.2
0.9	1.8	500	0.5	1.0	1.38	1.33	Yes	3.6
0.9	1.8	1000	0.5	1.0	1.16	1.08	Yes	6.9
3.6	7.2	100	2.0	1.0	1.42	1.38	Yes	2.8
3.6	7.2	500	2.0	1.0	0.68	0.64	No	5.8
3.6	7.2	800	2.0	1.0	0.37	0.39	No	5.4
9.0	18.0	100	5.0	1.0	1.17	1.09	Yes	6.8
9.0	18.0	200	5.0	1.0	0.70	0.67	No	4.3
9.0	18.0	300	5.0	1.0	0.42	0.42	No	0.0
0.9	1.8	100	0.5	2.0	1.72	1.66	Yes	3.5
0.9	1.8	500	0.5	2.0	1.53	1.45	Yes	5.2
0.9	1.8	1000	0.5	2.0	1.28	1.21	Yes	5.8
3.6	7.2	100	2.0	2.0	1.57	1.38	Yes	3.8
3.6	7.2	500	2.0	2.0	0.89	0.90	No	1.1
3.6	7.2	800	2.0	2.0	0.62	0.64	No	3.2
9.0	18.0	100	5.0	2.0	1.28	1.21	Yes	5.4
9.0	18.0	200	5.0	2.0	0.90	0.90	No	0.0
9.0	18.0	300	5.0	2.0	0.67	0.68	No	1.5

the load resistance is greater than the effective output resistance of the CMOS inverter (280 Ω); the delay predicted based on the slow ramp input signal is still quite accurate.

4.6 Summary

The assumption of a fast ramp input signal, which is widely used in the transient analysis of CMOS logic gates, has been quantified in this chapter. The criterion for characterizing the input signal depends upon the input transition time, the device parameters, and the load conditions. Simple, general, yet accurate analytical expressions characterizing the output voltage of a CMOS inverter driving a resistive-capacitive load under the condition of a fast ramp input signal have been presented.

Based on the analysis of the output voltage of a CMOS inverter, the effect of the interconnect resistance has been evaluated. The interconnect resistance shields the load capacitance in the saturation region as compared to a capacitive load condition. In addition, the signal quality is also degraded by the interconnect resistance due to the degraded waveform shape of the output voltage, causing added short-circuit power and subthreshold current in the following logic stage.

The propagation delay model for both a fast ramp and slow ramp input signal has also been presented. The error of the propagation delay model as compared to SPICE based on these analytical expressions is less than 7% for a variety of transistor sizes, input transition times, and load conditions.

Analytical expressions for both the short-circuit and resistive power consumption have also been presented. Two different methods to estimate the short-circuit power have been discussed. Expressions characterizing the total transient power

dissipation, which can be used to estimate circuit power at the system level, have also been described.

Chapter 5

A CMOS Logic Gate Driving an Inductive Interconnect

5.1 Introduction

Before the emergence of high speed VLSI circuits, such as gigahertz microprocessors, interconnect was modeled as a simple capacitor, a lumped *RC*, or as a distributed *RC* line in medium and high speed applications [15, 74]. The transient analysis of a CMOS logic gate driving a capacitive [52] or a resistive-capacitive load [76] has been addressed in the literatures in terms of the propagation delay [48, 72, 73] and short-circuit power [47, 68, 71, 90].

If the transition times in high speed VLSI circuits are comparable to the time of flight of the signals propagating along the low resistivity interconnect line, or the inductive time constant of an interconnection exceeds the resistive time constant, the inductance should also be considered in the interconnect model [44, 45]. The interconnect in these high speed circuits should therefore be modeled as a lumped or distributed *RLC* line.

In order to evaluate the effects of on-chip inductance on the behavior of a CMOS inverter, the interconnect is modeled as a lumped *RLC*, which is the load impedance of an interconnect line. The nth power law model [41] is used to char-

acterize the submicrometer MOS transistors. The nth power law model is more accurate in the linear region and in determining the drain-to-source saturation voltage as compared to the alpha power law model [52], avoiding any discontinuity between the linear and saturation regions. The input transition times are considered in the expressions for the propagation delay and the output voltage of a CMOS inverter. Large inductive loads and fast input transition times can result in significant short-circuit currents. The short-circuit power of a CMOS inverter driving a lossless transmission line is presented in [91], in which the device is modeled by the alpha power law model. The short-circuit current is included in deriving the analytical expressions characterizing the output voltage. Analytical equations for the short-circuit power are derived based on the load conditions and the shape of the input waveform. The waveform of the output voltage based on these analytical equations are quite close to SPICE for fast ramp input signals. The predicted propagation delay is within 10% and the estimated peak short-circuit current is less than 7% as compared to SPICE.

The close form expressions characterizing the output voltage of a CMOS inverter driving an *RLC* load are addressed in Section 5.2. Analytical equations describing the propagation delay are derived for both fast ramp and slow ramp input signals in Section 5.3. The effects of the inductive load on the output voltage, propagation delay, and short-circuit power are discussed in Section 5.4. A discussion on the short-circuit power is addressed in Section 5.5 followed by some concluding remarks in Section 5.6.

5.2 Waveform Shape of the Output Voltage

The equivalent circuit of a CMOS inverter driving an RLC load is shown in Figure 5.1(a). R, L, and C are the effective load resistance, inductance, and capacitance of an interconnect line, respectively. V_o and V_1 are the output voltage of the CMOS inverter and the voltage across the load capacitance C. The initial state of the input voltage is assumed to be 0 volts and both V_o and V_1 are initially at logic high (V_{dd}). The input voltage is a ramp signal,

$$V_{in}(t) = \frac{t}{\tau_r} V_{dd} \qquad \text{for} \quad 0 \leq t \leq \tau_r, \tag{5.1}$$

where τ_r is the rise time of the input signal.

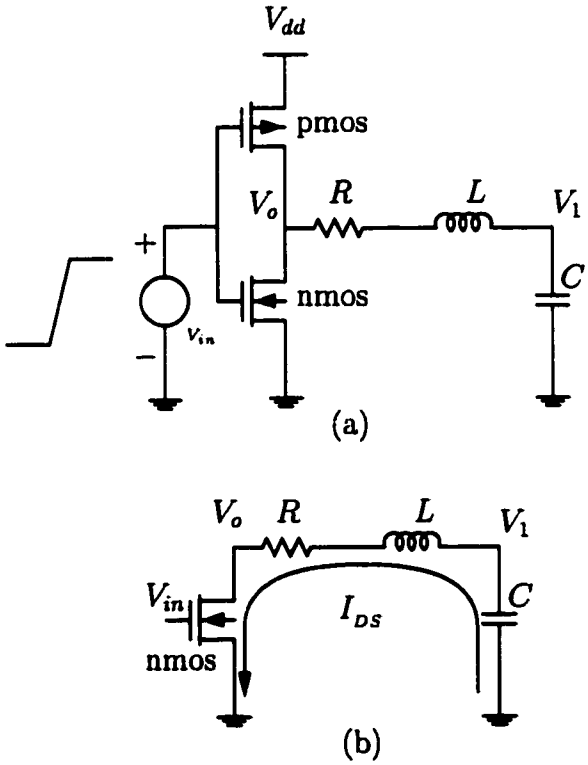


Figure 5.1: A CMOS inverter driving an RLC load

A fast ramp signal is assumed in this discussion, where the input slope exceeds one-third of the output slope [69]. The effect of the PMOS transistor is neglected based on the assumption of a fast ramp input signal. This assumption is not valid if the input is a slow ramp signal as compared to the output waveform. A simplified circuit is shown in Figure 5.1(b). The operating regions of the NMOS transistor during a high-to-low output transition are shown in Figure 5.2.

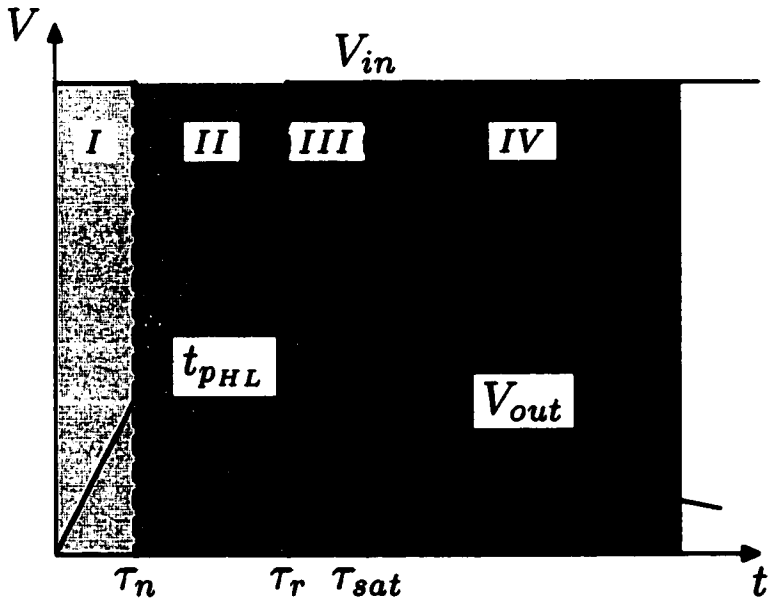


Figure 5.2: Operating regions of an NMOS transistor during the high-to-low output transition.

Before the input voltage reaches V_{TN}, the NMOS transistor is OFF and no current can flow (Region I). Therefore, the output voltage V_o remains at V_{dd} until τ_n, *i.e.*, the time for the input voltage to reach V_{TN}.

If the input voltage is greater than V_{TN}, the NMOS transistor is ON and operates in the saturation region (Region II). The output voltage satisfies the

following equations,

$$V_1(t) = L\frac{dI_{DS}}{dt} + RI_{DS} + V_o(t), \tag{5.2}$$

$$C\frac{dV_1(t)}{dt} = -I_{DS}. \tag{5.3}$$

The drain-to-source current I_{DS} of the NMOS transistor is

$$I_{DS} = B_n(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}. \tag{5.4}$$

The solution of $V_o(t)$ is

$$\begin{aligned} V_o(t) &= V_{dd} - V_c(t) - V_r(t) - V_l(t), \\ V_c(t) &= \frac{B_n\tau_r}{C(n_n+1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1}, \\ V_r(t) &= RB_n(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}, \\ V_l(t) &= LB_n\frac{n_nV_{dd}}{\tau_r}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n-1}, \end{aligned} \tag{5.5}$$

where $\tau_n \leq t \leq \tau_r$. $V_c(t)$ is the voltage change related to the load capacitance, $V_r(t)$ is the voltage drop across the load resistance, and $V_l(t)$ is the voltage induced by the load inductance, respectively.

After τ_r, the input voltage is fixed at V_{dd} and the NMOS transistor continues to operate in the saturation region (Region III). Therefore, the discharge current is equal to the saturated drain-to-source current of the NMOS transistor, *i.e.*, I_{nsat}, which is a constant. The output voltage $V_o(t)$ in this region is

$$V_o(t) = V_1(\tau_r) - \frac{B_n}{C}(V_{dd} - V_{TN})^{n_n}(t - \tau_r) - RB_n(V_{dd} - V_{TN})^{n_n}, \tag{5.6}$$

where

$$V_1(\tau_r) = V_{dd} - \frac{B_n\tau_r(V_{dd} - V_{TN})^{n_n+1}}{C(n_n+1)V_{dd}}, \tag{5.7}$$

and $\tau_r \leq t \leq \tau_{nsat}$. τ_{nsat} is the time when the NMOS transistor leaves the saturation region and is determined from (5.6)

$$\tau_{nsat} = \frac{V_1(\tau_r) - V_{nsat} - RI_{nsat}}{B_n(V_{dd} - V_{TN})^{n_n}} C + \tau_r, \tag{5.8}$$

where $V_{nsat} = K_n(V_{dd} - V_{TN})^{m_n}$.

After V_o drops below V_{nsat}, the NMOS transistor enters the linear region (Region IV) and the drain-to-source current of the NMOS transistor is

$$I_{DS} = B_n(V_{dd} - V_{TN})^{n_n}(2 - \frac{V_o(t)}{V_{nsat}})\frac{V_o(t)}{V_{nsat}}. \tag{5.9}$$

However, there is no tractable solution of (5.2) and (5.3) in this region. In order to derive an analytical solution, the drain-to-source current of the NMOS transistor is approximated by the effective output conductance,

$$I_{DS} = \gamma_n V_o(t). \tag{5.10}$$

The output voltage in this region is

$$V_o = C_1 e^{-\alpha_1 t} + C_2 e^{-\alpha_2 t} \qquad \text{for } t \geq \tau_{nsat}, \tag{5.11}$$

where

$$\begin{aligned} \alpha_1 &= \frac{\frac{1+R\gamma_n}{L\gamma_n} + \sqrt{(\frac{1+R\gamma_n}{L\gamma_n})^2 - \frac{4}{LC}}}{2}, \\ \alpha_2 &= \frac{\frac{1+R\gamma_n}{L\gamma_n} - \sqrt{(\frac{1+R\gamma_n}{L\gamma_n})^2 - \frac{4}{LC}}}{2}. \end{aligned} \tag{5.12}$$

C_1 and C_2 can be determined by $V_o(\tau_{nsat})$ and $V_o'(\tau_{nsat})$. Therefore, closed form expressions of the CMOS inverter output voltage in each region are derived based on the assumption of a fast ramp input signal.

However, the effective output conductance of the NMOS transistor in (5.10) depends upon the the output voltage in the linear region,

$$\gamma_n = \frac{I_{nsat}}{V_{nsat}}(2 - \frac{V_o(t)}{V_{nsat}}) = \gamma_{nsat}(2 - \frac{V_o(t)}{V_{nsat}}). \tag{5.13}$$

If $V_o(t)$ is close to V_{nsat}, the effective output conductance can be approximated as

$$\gamma_n \approx \gamma_{nsat} = \frac{B_n}{K_n}(V_{dd} - V_{TN})^{n_n - m_n}. \tag{5.14}$$

If $V_o(t)$ is close to zero, the effective output conductance is

$$\gamma_n \approx 2\gamma_{nsat} = 2\frac{B_n}{K_n}(V_{dd} - V_{TN})^{n_n - m_n}. \tag{5.15}$$

Therefore, in order to accurately characterize the output voltage, γ_n is chosen between γ_{nsat} and $2\gamma_{nsat}$ in (5.12).

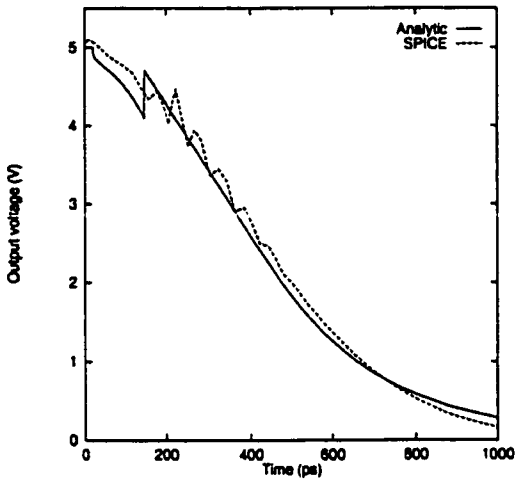
The output voltages predicted by these analytical expressions are compared to SPICE simulation. The results are shown in Figure 5.3. Note that the output voltage waveforms are quite close to the waveforms derived from the SPICE simulation.

5.3 Propagation Delay

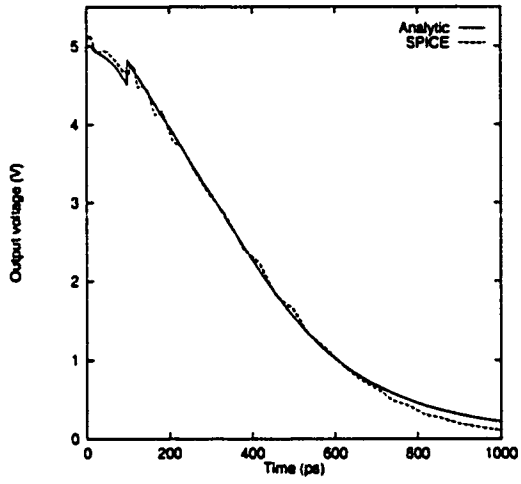
Analytical expressions characterizing the propagation delay of both a fast ramp and a slow ramp input signal are presented in this section. Therefore, the effect of the on-chip inductance on the propagation delay can be analyzed quantitatively. The propagation delay can be determined from the waveform of the output voltage derived in Section 5.2.

5.3.1 Propagation Delay of a Fast Ramp Signal

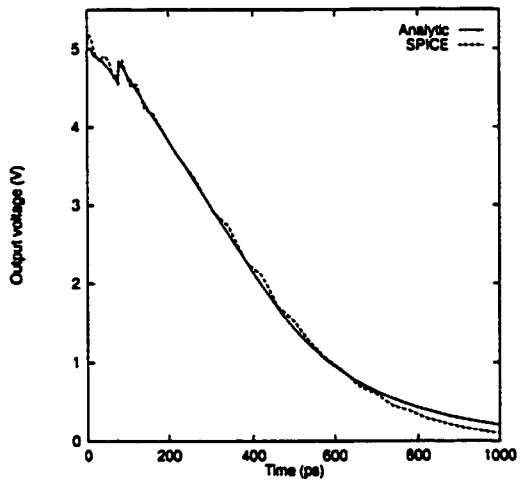
$t_{0.5}$ is the time between when the input and output voltages reach the 50% point. For a fast ramp signal, $t_{0.5}$ is typically in region IV since V_{nsat} is generally greater than $0.5V_{dd}$. The output voltage in region IV is described by (5.11) and $t_{0.5}$ can be determined using a Newton-Raphson iteration. However, α_1 is typically



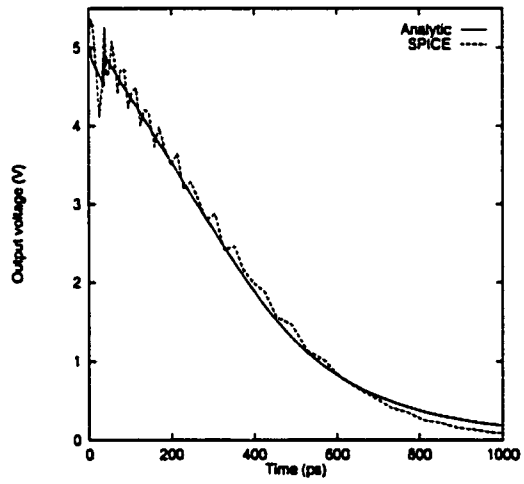
(a) τ_r=150 ps, R=10 Ω, L=4 nH, C=1 pF.



(b) τ_r=100 ps, R=10 Ω, L=2 nH, C=1 pF.



(c) τ_r=80 ps, R=5 Ω, L=1 nH, C=1 pF.



(d) τ_r=40 ps, R=5 Ω, L=1 nH, C=1 pF.

Figure 5.3: Comparison of the analytically derived output voltage with SPICE simulation.

much greater than α_2, therefore the output voltage can be approximated as

$$V_o = V_{nsat} e^{-\alpha_2 (t - \tau_{nsat})}. \tag{5.16}$$

The high-to-low propagation delay t_{pHL} of a CMOS inverter is

$$T_{pHL} = \frac{1}{\alpha_2} ln \frac{2V_{nsat}}{V_{dd}} + \tau_{nsat} - \frac{\tau_r}{2}. \tag{5.17}$$

The output transition time can also be calculated based on the assumption of a fast ramp input signal. $t_{0.9}$ is the time when the output voltage reaches $0.9V_{dd}$ and $t_{0.1}$ is the time when the output voltage reaches $0.1V_{dd}$. $t_{0.9}$ and $t_{0.1}$ can be determined by (5.5) and (5.11), respectively, using the Newton-Raphson technique. The transition time of the output voltage is

$$\tau_o = \frac{t_{0.1} - t_{0.9}}{0.8}. \tag{5.18}$$

5.3.2 Propagation Delay of a Slow Ramp Signal

All of these analyses are based on an assumption of a fast ramp input signal, *i.e.*, the NMOS transistor remains in the saturation region before the input transition is completed. If τ_r is greater than τ_{nsat}, *i.e.*, the NMOS transistor enters the linear region before the input transition is completed, the input is assumed to be a slow ramp signal.

For a slow ramp input signal, when the input signal exceeds V_{TN}, the NMOS transistor turns ON and begins operating in the saturation region. Therefore, the

output voltage can be expressed as

$$\begin{aligned} V_o(t) =& V_{dd} - V_c(t) - V_r(t) - V_l(t), \\ V_c(t) =& \frac{B_n \tau_r}{C(n_n+1)V_{dd}} (\frac{t}{\tau_r} V_{dd} - V_{TN})^{n_n+1}, \\ V_r(t) =& RB_n (\frac{t}{\tau_r} V_{dd} - V_{TN})^{n_n}, \\ V_l(t) =& LB_n \frac{n_n V_{dd}}{\tau_r} (\frac{t}{\tau_r} V_{dd} - V_{TN})^{n_n-1}, \end{aligned} \tag{5.19}$$

where $\tau_n \leq t \leq \tau_{nsat}$. τ_{nsat} is also the time when the NMOS transistor leaves the saturation region. In this case, τ_{nsat} is calculated from

$$K_n (\frac{\tau_{nsat}}{\tau_r} V_{dd} - V_{TN})^{m_n} = V_{dd} - V_c(\tau_{nsat}) - V_r(\tau_{nsat}) - V_l(t_{nsat}). \tag{5.20}$$

This equation is solved using a Newton-Raphson iteration.

The time when the output voltage V_o reaches $0.5V_{dd}$ can be approximated from (5.19),

$$\frac{V_{dd}}{2} = V_c(t_{0.5}) + V_r(t_{0.5}) + V_l(t_{0.5}). \tag{5.21}$$

The solution of $t_{0.5}$ can also be obtained by using a Newton-Raphson routine.

In the derivation of $t_{0.5}$ for a slow ramp signal, the effect of the PMOS transistor is neglected. In order to accurately estimate the propagation delay for a slow ramp input signal, some modifications are necessary and the high-to-low propagation is approximated as

$$t_{pHL} = \frac{\tau_r}{\tau_{nsat}} (t_{0.5} - \frac{\tau_r}{2}), \tag{5.22}$$

where the ratio τ_r/τ_{nsat} characterizes the deviation of the input signal from a fast ramp input signal. Both τ_{nsat} and $t_{0.5}$ can be obtained from (5.20) and (5.21). Therefore, the propagation delay for both fast ramp and slow ramp input signals is described in (5.17) and (5.22), respectively.

5.4 Effects of an Inductive Load

An inductive load may cause large short-circuit currents if the input transition time is short, as described by the term $V_i(t)$ in (5.5). SPICE simulation results depicted in Figures. 5.4 and 5.5 demonstrate that for a fast ramp input signal or large inductive load, the short-circuit current cannot be neglected. The spikes shown in Figures. 5.4 and 5.5 are caused by large short-circuit currents.

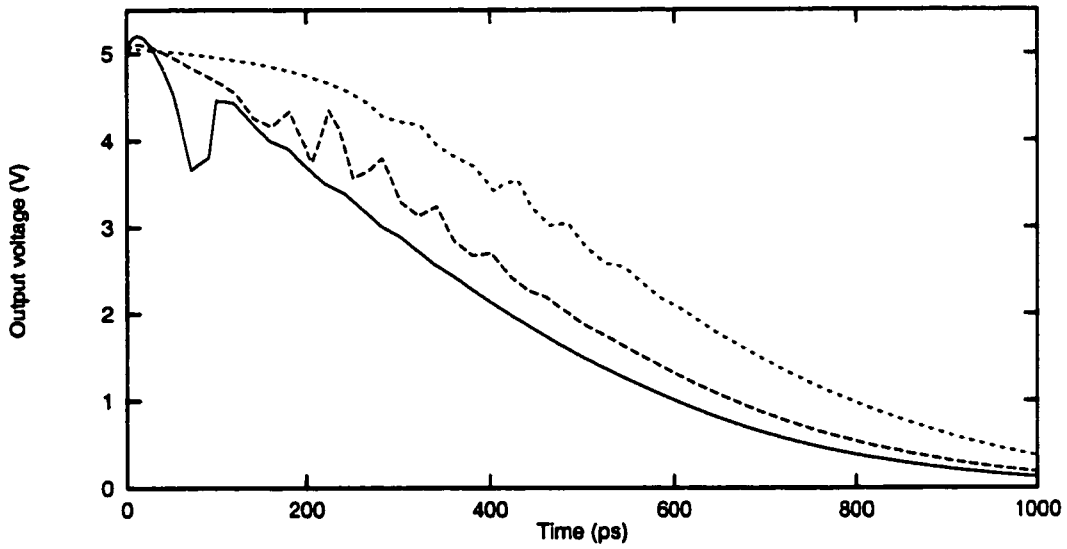


Figure 5.4: Dependence of the output voltage on the input ramp time. The solid line, dashed line, and dotted line are for 0.1 ns, 0.2 ns, and 0.4 ns rise times, respectively.

A circuit diagram of a CMOS inverter driving an *RLC* load is shown in Figure 5.6. The short-circuit current through the PMOS transistor I_3 reduces the discharge current I_2. The PMOS transistor operates in the linear region when the NMOS transistor turns on initially (assuming a fast ramp input signal). The currents through the NMOS transistor, the short-circuit current through the PMOS

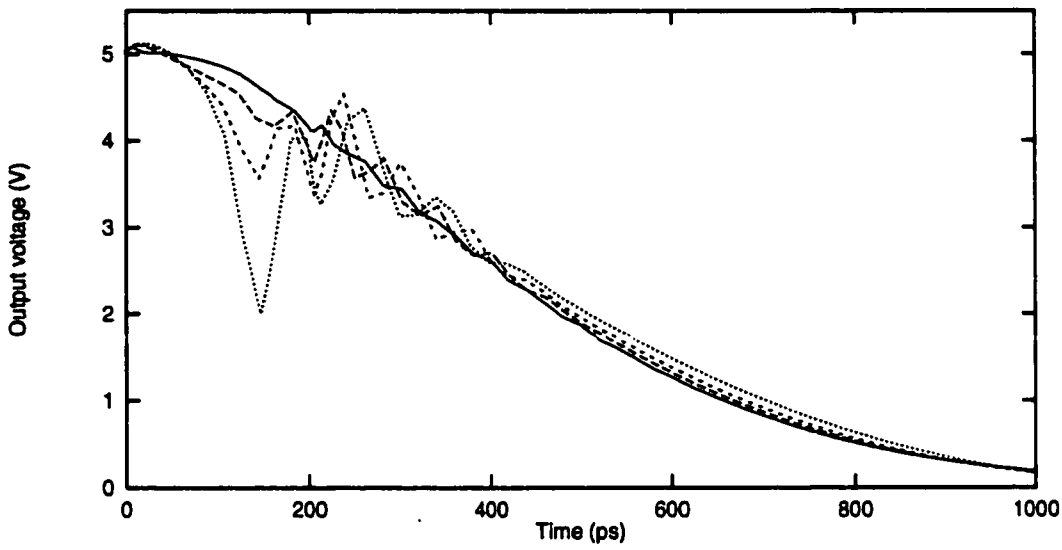


Figure 5.5: Dependence of the output voltage on the inductive load. The inductive loads are 1 nH, 5 nH, 10 nH, and 20 nH from the top to the bottom line, respectively.

transistor, and the discharge current satisfy

$$I_2 = I_1 - I_3. \tag{5.23}$$

The current through the PMOS transistor can be approximated by an effective output conductance in the linear region,

$$I_1 = B_n(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}, \tag{5.24}$$

$$I_3 \approx \alpha_p \frac{B_p}{K_p}(V_{dd} - \frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p - m_p}(V_{dd} - V_o), \tag{5.25}$$

where α_p is between 1.0 and 2.0 depending upon V_o and V_{TP} is the absolute value of the PMOS threshold voltage.

For the extreme condition, in which the inductive load is large or the input transition time is short, the current through the PMOS transistor is almost equal to the current through the NMOS transistor and the discharge current is negligible.

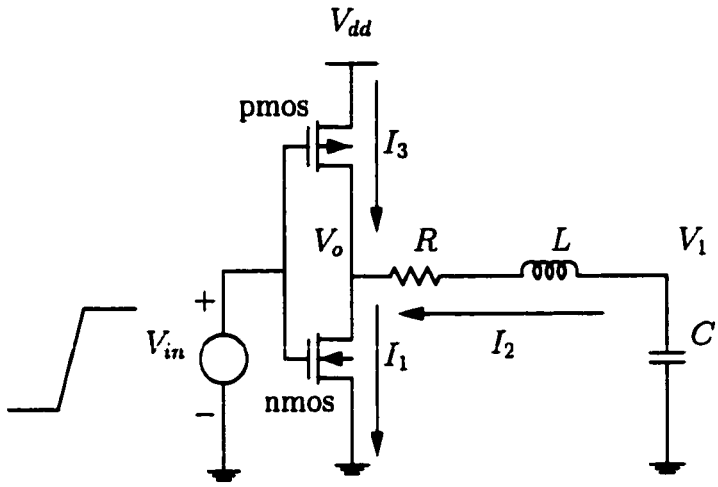


Figure 5.6: Discharge current is reduced by the current through the PMOS transistor

The output voltage can therefore be approximated as

$$V_o(t) \approx V_{dd} - \frac{B_n(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}}{\alpha_p \frac{B_p}{K_p}(V_{dd} - \frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p - m_p}}. \tag{5.26}$$

The solid line shown in Figure 5.7 depicts a SPICE simulation for a 50 ps rise

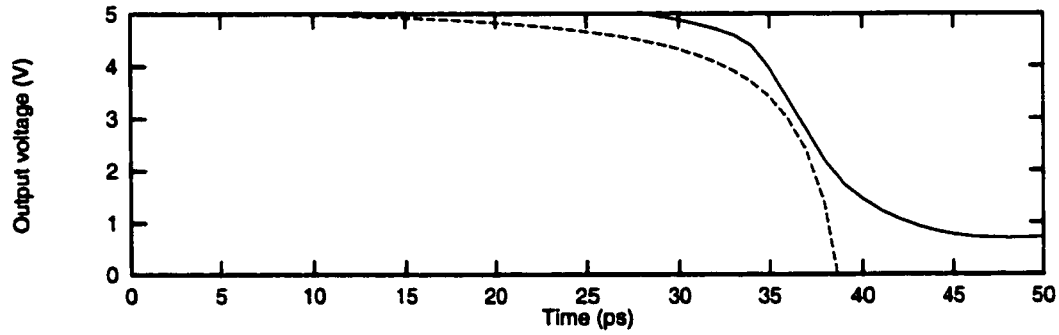


Figure 5.7: Output voltage for a fast ramp input and large inductive load.

time and 20 nH inductive load. The dashed line is from (5.26). Note that SPICE is quite close to (5.26) in the range from 30 ps to 38 ps.

The relationship between $V_o(t)$ and the current through the NMOS transistor I_1, the discharge current I_2, and the short-circuit current I_3 is

$$-\frac{I_2}{C} - \frac{dV_o(t)}{dt} = R\frac{dI_2}{dt} + L\frac{d^2I_2}{d^2t} \qquad \tau_n \leq t \leq \tau_{poff}, \tag{5.27}$$

where τ_{poff} is the time when the PMOS transistor is turned off. In order to simplify this analysis, the voltage across the load capacitance $V_1(t)$ is assumed to remains at V_{dd} when the PMOS transistor operates in the linear region. The output voltage is

$$V_{dd} - V_o(t) = RI_2 + L\frac{dI_2}{dt} \qquad \tau_n \leq t \leq \tau_{psat}, \tag{5.28}$$

where τ_{psat} is the time when the PMOS transistor enters the saturation region. To derive an analytical solution of $V_o(t)$, it is assumed that $V_o(t)$ changes sufficiently slowly such that $\frac{dV_o(t)}{dt}$ can be neglected. The approximated solution is listed in Table 5.1.

If $V_{dd} - V_o(t)$ is greater than $V_{psat}(t)$, the PMOS transistor starts operating in the saturation region. The time when the PMOS transistor operates in the saturation region can be determined by solving

$$V_{dd} - V_o(\tau_{psat}) = K_P(V_{dd} - \frac{\tau_{psat}}{\tau_r}V_{dd} - V_{TP})^{m_P}, \tag{5.44}$$

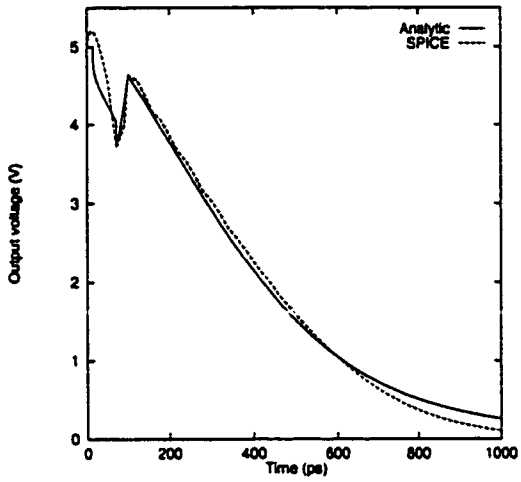
using the Newton-Raphson technique. After τ_{psat}, the short-current I_3 is expressed as

$$I_3 = B_p(V_{dd} - \frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p}. \tag{5.45}$$

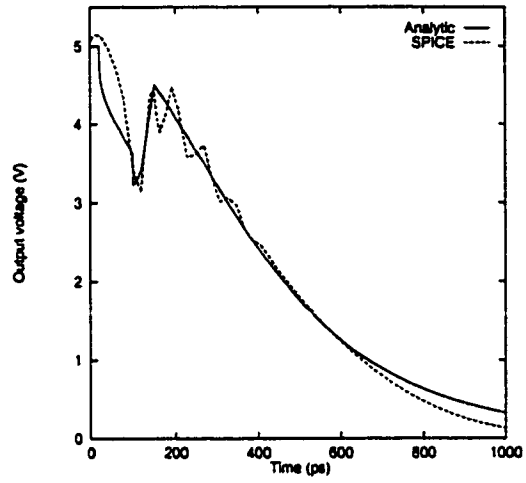
V_1 is no longer assumed to remain at V_{dd} after τ_{psat}. The analytical solutions of $V_o(t)$ and $V_1(t)$ during the input transition are listed in Table 5.1, where C_1, C_2, C_3, and C_4 can be determined by the initial conditions of $V_o(t)$ and $V_1(t)$, respectively.

Table 5.1: Analytical expressions of the output voltage including the short-circuit current

Time region	Analytical expressions of the output voltage $V_o(t)$ and $V_1(t)$
$\tau_n \leq t \leq \tau_{psat}$	$V_o(t) = V_{dd} - \frac{RI_1 + LI_1'}{1 + R\gamma_p - L\gamma_p'}$ (5.29) $I_1' = \frac{B_n n_n V_{dd}}{\tau_r}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n - 1}$ (5.30) $\gamma_p = \frac{\alpha_p B_p}{K_p}(V_{dd} - \frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p - m_p}$ (5.31) $\gamma_p' = \frac{\alpha_p B_p (n_p - m_p) V_{dd}}{K_p \tau_r}(V_{dd} - \frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p - m_p - 1}$ (5.32)
$\tau_{psat} \leq t \leq \tau_{poff}$	$V_o(t) = C_1 - \frac{V_{0,1}(t)}{C} - RV_{o,2}(t) - LV_{o,3}(t)$ (5.33) $V_{o,1}(t) = \frac{B_n \tau_r}{(n_n + 1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{(n_n+1)} + \frac{B_p \tau_r}{(n_p + 1)V_{dd}}(V_{dd} - \frac{t}{\tau_r}V_{dd} - V_{TP})^{(n_p+1)}$ (5.34) $V_{o,2}(t) = B_n(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n} - B_p(V_{dd} - \frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p}$ (5.35) $V_{o,3}(t) = \frac{B_n n_n V_{dd}}{\tau_r}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{(n_n-1)} + \frac{B_p n_p V_{dd}}{\tau_r}(V_{dd} - \frac{t}{\tau_r}V_{dd} - V_{TP})^{(n_p-1)}$ (5.36) $V_1(t) = C_2 - \frac{V_{1,1}(t)}{C}$ (5.37) $V_{1,1}(t) = \frac{B_n \tau_r}{(n_n + 1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{(n_n+1)} + \frac{B_p \tau_r}{(n_p + 1)V_{dd}}(V_{dd} - \frac{t}{\tau_r}V_{dd} - V_{TP})^{(n_p+1)}$ (5.38)
$\tau_{poff} \leq t \leq \tau_r$	$V_o(t) = C_3 - \frac{V_{0,4}(t)}{C} - RV_{o,5}(t) - LV_{o,6}(t)$ (5.39) $V_{o,4}(t) = \frac{B_n \tau_r}{(n_n + 1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{(n_n+1)}$ (5.40) $V_{o,6}(t) = \frac{B_n n_n V_{dd}}{\tau_r}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{(n_n-1)}$ (5.41) $V_1(t) = C_4 - \frac{V_{1,2}(t)}{C}$ (5.42) $V_{1,2}(t) = \frac{B_n \tau_r}{(n_n + 1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{(n_n+1)}$ (5.43)



(a) τ_r=100 ps, R=10 Ω, L=5 nH, C=1 pF.



(b) τ_r=150 ps, R=20 Ω, L=10 nH, C=1 pF.

Figure 5.8: Comparison of the analytically derived output voltage with SPICE simulation.

The output voltage based on the analytical expressions listed in Table 5.1 are compared to SPICE for a large inductive load, as shown in Figure 5.8. Note that these analytical expressions predict the voltage spike during the input transition, permitting the peak short-circuit current to be accurately estimated.

Similar to the analysis used in Section 5.2, τ_{nsat} is determined based on $V_1(\tau_r)$. The propagation delay can also be determined by (5.17). The load inductance affects the propagation delay of a CMOS inverter as described in (5.17). These analytical expressions are used to estimate the propagation delay of a CMOS inverter. The estimated delays as compared to SPICE simulations are shown in Table 5.2. The error is within 10% for most operating regimes.

Table 5.2: Propagation delay of a CMOS inverter driving an *RLC* load

τ_r (ps)	R (Ω)	L (nH)	C (pF)	t_{pHL} (ps)		Error (%)
				SPICE	Analytic	ϵ
40.0	5.0	1.0	1.0	344.0	329.0	4.4
50.0	5.0	1.0	1.0	377.0	353.0	6.4
50.0	5.0	2.0	1.0	350.0	323.0	7.7
50.0	10.0	5.0	1.0	325.0	305.0	6.2
50.0	20.0	5.0	1.0	325.0	302.0	7.1
100.0	30.0	10.0	1.0	325.0	351.0	8.0
100.0	20.0	10.0	1.0	322.0	353.0	9.6
100.0	10.0	10.0	1.0	322.0	356.0	10.6
100.0	20.0	10.0	2.0	678.0	695.0	2.5
150.0	20.0	10.0	1.0	419.0	390.0	6.9
Maximum error						10.6%
Average error						7.1%

5.5 Short-Circuit Power

A *DC* path from V_{dd} to ground exists when the input signal transitions from low to high or from high to low. For example, if the input signal switches from V_{TN} to $V_{dd} - V_{TP}$, the short-circuit current will flow through the PMOS transistor and dissipate extra power. The short-circuit current cannot be neglected because short transition times and large inductive loads can cause a significant amount of short-circuit current, as addressed in the previous section.

To develop an expression for the short-circuit power, the NMOS transistor is assumed to operate in the saturation region during most of the time when the short-circuit current flows. Based on this assumption, expressions in Table 5.1 can be used to approximate the output voltage to provide an expression for the short-circuit power dissipation. The short-circuit power during the high-to-low

transition $P_{sc_{HL}}$ is

$$P_{sc_{HL}} = fV_{dd}\int I_p(t)dt, \tag{5.46}$$

where f is the switching frequency of the inverter and $I_p(t)$ is the current through the PMOS transistor. The absolute value of the drain-to-source voltage of the PMOS transistor is

$$V_{DSP}(t) = V_{dd} - V_o(t). \tag{5.47}$$

During the time interval from τ_n to τ_{psat}, the PMOS transistor operates in the linear region. $I_p(t)$ can be expressed as

$$I_p(t) = I_{psat}(2 - \frac{V_{DSP}(t)}{V_{psat}})\frac{V_{DSP}(t)}{V_{psat}}, \tag{5.48}$$

where

$$\begin{aligned} I_{psat} &= B_p(V_{dd} - \frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p}, \\ V_{psat} &= K_p(V_{dd} - \frac{t}{\tau_r}V_{dd} - V_{TP})^{m_p}. \end{aligned} \tag{5.49}$$

The short-circuit power in this region is

$$P_{sc_{HL_I}} = fV_{dd}\int_{\tau_n}^{\tau_{psat}} I_p(t)dt. \tag{5.50}$$

This integral does not have an analytical solution after substituting $I_p(t)$ from (5.48).

The peak short-circuit current occurs in the time interval between τ_n and τ_{psat} because $I_p(t)$ decreases from τ_{psat} to τ_{poff}. The time when the peak current occurs, from (5.48), is

$$I_p'(t_{peak}) = 0. \tag{5.51}$$

This equation can be solved by using a Newton-Raphson iteration, requiring only two to four iterations to obtain the solution of t_{peak}, permitting the peak short-circuit current to be determined.

Table 5.3: Peak short-circuit current of a CMOS inverter driving a *RLC* load

τ_r (ps)	R (Ω)	L (nH)	C (pF)	I_{peak} (mA) SPICE	I_{peak} (mA) Analytic	Error %
150.0	20.0	10.0	1.0	2.0	1.92	5.9
100.0	30.0	10.0	1.0	2.70	2.62	3.0
100.0	20.0	10.0	1.0	2.70	2.68	0.8
100.0	10.0	10.0	1.0	2.70	2.56	5.2
100.0	20.0	10.0	2.0	2.62	2.59	1.2
50.0	10.0	5.0	1.0	3.38	3.20*	5.3
50.0	20.0	5.0	1.0	3.36	3.15*	6.3
40.0	5.0	1.0	1.0	4.2	4.01*	4.5
Maximum error				6.3%		
Average error				4.6%		

However, based on the assumption that the peak current occurs near the middle of the input waveform for a balanced inverter [76], the peak current is

$$I_{peak} = B_p(\frac{V_{dd}}{2} - V_{TP})^{n_p}(2 - \frac{V_{DSP}(\frac{\tau_r}{2})}{K_p(\frac{V_{dd}}{2} - V_{TP})^{m_p}})\frac{V_{DSP}(\frac{\tau_r}{2})}{K_p(\frac{V_{dd}}{2} - V_{TP})^{m_p}}. \quad (5.52)$$

Note, consistent with the literature [69], that the peak short-circuit current depends on both the input waveform and the load impedance.

Knowing I_{peak}, the short-circuit current $I_{sc}(t)$ can be approximated by a triangle [76]. The short-circuit power during the high-to-low transition can therefore be approximated by the product of the area of the triangle and V_{dd}, *i.e.*,

$$P_{sc_{HL}} = \frac{1}{2}I_{peak}(\tau_{poff} - \tau_n)V_{dd}f, \quad (5.53)$$

where f is the switching frequency of the inverter and I_{peak} can be determined from (5.51) or (5.52).

Similarly, the short-circuit current during the low-to-high transition $P_{sc_{LH}}$ can also be derived using the peak short-circuit current during the charge-up process. The peak current based on these analytical equations is compared to SPICE simulation and the results are listed in Table 5.3. The analytical results of the final

three rows are calculated from (5.51). The accuracy of these analytical expressions is within 7% as compared to SPICE.

5.6 Summary

The effects of on-chip inductance on a CMOS inverter are discussed in terms of the output voltage, propagation delay, and short-circuit power. Fast transition times and large inductive loads increase the short-circuit current. Therefore, short-circuit power cannot be neglected when estimating the total power caused by an inductive load. A simple technique is presented to estimate the short-circuit power based on the peak short-circuit current. Analytical expressions for the output voltage are derived for a CMOS inverter driving an *RLC* load. The propagation delay based on these analytical equations is within 11% as compared to SPICE simulation. The error of the estimated peak short-circuit current is less than 7%.

Chapter 6

Capacitively Coupled On-Chip Interconnect

6.1 Introduction

On-chip coupling noise in CMOS integrated circuits, until recently considered a second order effect [21, 26], has become an important issue in deep submicrometer (DSM) CMOS integrated circuits [23, 92, 93]. With decreasing feature size and increasing average length of on-chip interconnections, the interconnect capacitance has become comparable to or larger than the gate capacitance [1, 7, 15].

Interconnections in a CMOS integrated circuit are conductors deposited on dielectric insulation layers [94, 95]. The mutual electric field flux between neighboring interconnect lines results in a coupling (or fringing) capacitance [57, 58, 60–62, 96]. The coupling capacitance increases as the spacing between adjacent interconnect lines is reduced and/or the aspect ratio of the interconnect thickness-to-width is increased [1, 7]. The coupling capacitance may become comparable to the line-to-ground interconnect capacitance [62, 96, 97]. Therefore, capacitive coupling has emerged as one of the primary issues in evaluating the signal integrity of CMOS integrated circuits [22, 27, 34, 37, 39].

The importance of interconnect coupling capacitances depends upon the signal behavior of a CMOS logic gate [98]. If a CMOS logic gate driving a coupled interconnection is in transition, the coupling capacitance can affect the propagation delay and the waveform shape of the output voltage signal [99]. For a capacitively coupled system, if one of these CMOS logic gates is quiet and the other logic gates are in transition, the coupling capacitance can not only change the propagation delay of the active logic gates, but can also induce a voltage change at the output of the quiet logic gate [100, 101]. If the voltage change is greater than the threshold voltage of the following logic gates, circuit malfunctions and unexpected power dissipation in the fanout stages may occur [23]. Furthermore, a change in voltage may cause overshoots (the signal rises above the voltage supply) or undershoots (the signal falls below ground) [18, 102]. The overshoots and undershoots may cause carrier injection or collection within the substrate [18].

In order to reduce both design cost and time, coupling effects should be estimated at the system level. The coupling noise voltage on a quiet interconnect has been analyzed by Shoji using a simple linear *RC* circuit in [23]. The effects of the coupling capacitance have also been addressed by Sakurai using a resistive-capacitive interconnect model in [78], in which the CMOS logic gates are approximated by the effective output resistance and similar interconnect lines are assumed. Estimating coupling noise voltage based on coupled transmission line model is presented in [103]. The nonlinear behavior of the MOS transistors is neglected in these analyses [23, 78, 103]. The maximum effective load capacitance, *i.e.*, the intrinsic load capacitance plus two times the coupling capacitance ($C + 2C_c$), is typically used to estimate the worst case propagation delay of an active logic gate [23, 78].

In this chapter, a transient analysis of two capacitively coupled logic gates is presented based on the signal activity. The nonlinear behavior of the MOS transistors is characterized by the nth power law model in the saturation region [41] and the effective output conductance in the linear region. The interconnect-to-ground capacitance (or self capacitance) and the gate capacitance of the following logic stage are included in the intrinsic load capacitance (C_1 or C_2). An analysis of the in-phase transition, in which two coupled logic gates transition in the same direction, demonstrates that the effective load capacitances may deviate from the intrinsic load capacitances if the logic gates and intrinsic load capacitances are different. The same conclusion can also be observed for an out-of-phase transition, where the transition changes in the opposite direction, making the effective load capacitances deviate from $C_1 + 2C_c$ or $C_2 + 2C_c$.

If one logic gate is active and the other is quiet, the coupling capacitance may cause the effective load capacitance of the active logic gate to be less than $C_1 + C_c$ or $C_2 + C_c$ when the active logic gate transitions from high-to-low and the quiet state is at a logic low (ground). However, if the quiet state is high (V_{dd}), the effective load capacitance of the active logic gate exceeds $C_1 + C_c$ or $C_2 + C_c$. If the active logic gate transitions from high-to-low and the quiet state is at a logic low, the coupling noise voltage causes the quiet state to drop below ground (undershoots). Overshoots occur when the inverter transitions from low-to-high and the quiet state is at a logic high (V_{dd}). Overshoots or undershoots may cause

current to flow through the substrate, possibly corrupting data in dynamic logic circuits [18]. This issue is also of significant concern in the logic elements within a bistable latch structure [104].

Analytical expressions characterizing the output voltages for each condition are presented based on an assumption of a fast ramp input signal. Delay estimates based on the analytical expressions are within 3% as compared to SPICE, while the estimate based on C_1 (C_2), $C_1 + 2C_c$ ($C_2 + 2C_c$), and $C_1 + C_c$ ($C_2 + C_c$) for an in-phase, an out-of-phase, and one active transition can reach 48%, 16%, and 12%, respectively. The peak noise voltage based on the analytical prediction is within 4% of SPICE.

The dependence of the coupling capacitance on signal activity is discussed in Section 6.2. Analytical expressions characterizing the effective load capacitance, output voltage, and propagation delay during an in-phase and out-of-phase transition are addressed in Sections 6.3 and 6.4, respectively, as well as a comparison between the analytical estimates and SPICE. An analytical expression characterizing the coupling noise voltage of a quiet logic gate is presented for both step and ramp input signals. The accuracy of these analytical expressions are compared to SPICE in Section 6.5. Strategies to reduce the effects of coupling capacitance are discussed in Section 6.6, followed by some concluding remarks in Section 6.7.

6.2 Signal Activity

A physical structure of two coplanar interconnect lines is shown in Figure 6.1. The self interconnect capacitance includes the parallel plate capacitance and the sidewall-to-ground capacitance, which is often described as the fringing capacitance. The sidewall-to-sidewall electric field between these two lines results in the

coupling capacitance C_c. Interconnect lines are typically driven by CMOS logic gates in VLSI circuits. The logic gates driving these interconnect lines are capacitively coupled. A circuit diagram of two capacitively coupled CMOS inverters is shown in Figure 6.2(a). In order to simplify this analysis, the interconnection is modeled as a capacitive load where C_1 includes both the interconnect capacitance of line 1 and the gate capacitance of Inv_3. C_2 includes both the interconnect capacitance of line 2 and the gate capacitance of Inv_4.

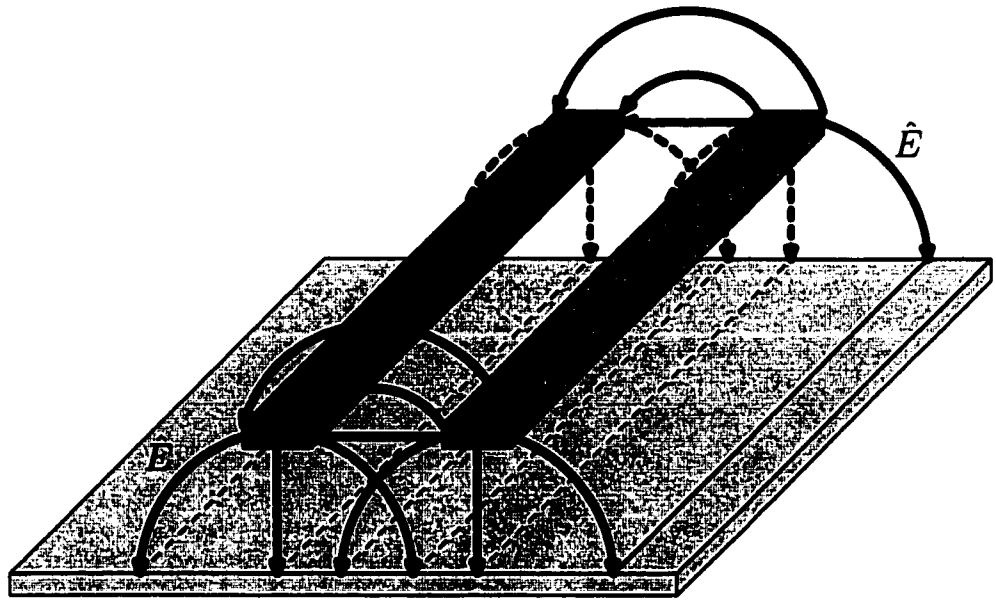


Figure 6.1: Physical layout of two capacitively coupled interconnect lines

The equivalent circuit and the current directions are shown in Figure 6.2(b). The output voltages of Inv_1 and Inv_2 are V_1 and V_2, respectively. The differential equations characterizing the behavior of this capacitively coupled system are

$$I_{DS1} = (C_1 + C_c)\frac{dV_1}{dt} - C_c\frac{dV_2}{dt}, \tag{6.1}$$

$$I_{DS2} = (C_2 + C_c)\frac{dV_2}{dt} - C_c\frac{dV_1}{dt}. \tag{6.2}$$

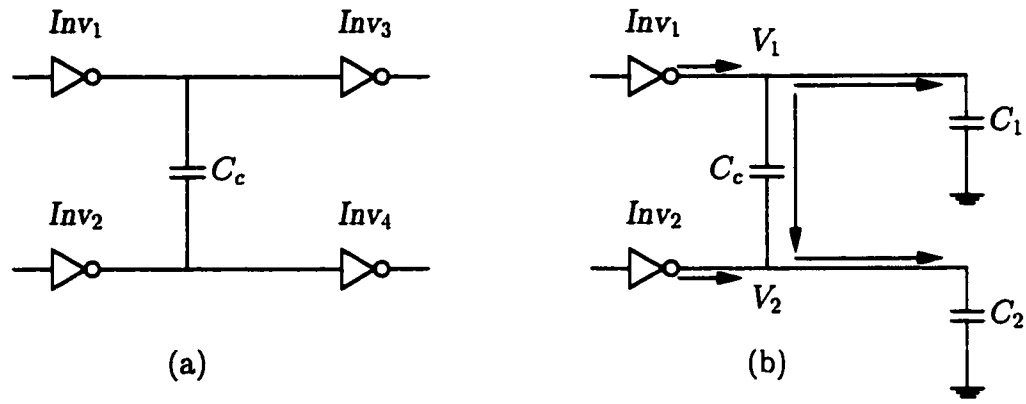


Figure 6.2: Circuit model of two capacitively coupled inverters. (a) A circuit diagram of two capacitively coupled CMOS inverters. (b) An equivalent circuit of the two coupled CMOS inverters.

The effects of the coupling capacitance on the transient response of these two coupled inverters also depend on the behavior of each inverter, *i.e.*, the signal activity. There are three possible conditions for each inverter, a high-to-low transition, a low-to-high transition, and a quiet state in which the output voltage of the inverter remains at either the voltage supply (V_{dd}) or ground. Both the high-to-low and low-to-high transitions are included in the dynamic transition. If the input signals at each inverter are purely random and uncorrelated, there are nine different combinations which can occur for a system composed of two capacitively coupled inverters. These combinations are listed in Table 6.1.

Assuming equal probability for each condition, the probability of an in-phase transition, in which both inverters have the same dynamic transitions, is 2/9. The probability of an out-of-phase transition, in which these two inverter have different dynamic transitions, is also 2/9. The probability of no dynamic transition is 1/9. The condition in which one inverter is quiet and the other is in transition has the highest probability, 4/9.

Table 6.1: Combinations of the signal activity for a system of two capacitively coupled inverters

V_{in1}	Inv_1	V_{in2}	Inv_2	
0 to V_{dd}	High-to-low	0 to V_{dd}	High-to-low	In-Phase
		V_{dd} to 0	Low-to-high	Out-of-Phase
		V_{dd} or 0	Quiet	One Active/One Quiet
V_{dd} to 0	Low-to-high	0 to V_{dd}	High-to-low	Out-of-Phase
		V_{dd} to 0	Low-to-high	In-Phase
		0 or V_{dd}	Quiet	One Active/One Quiet
V_{dd} or 0	Quiet	0 to V_{dd}	High-to-low	One Active/One Quiet
		V_{dd} to 0	Low-to-high	One Active/One Quiet
		0 or V_{dd}	Quiet	No Transition

In the following analysis, if both inverters are in transition, it is assumed that these inverters are triggered at the same time with the same input slew rate. During the logic transition, only the active transistors are considered in the development of the analytical expressions. The MOS transistors are characterized by the *nth* power law model in the saturation region and the effective output resistance in the linear region.

6.3 In-Phase Transition

The in-phase transition is an optimistic condition in terms of the effect of the coupling capacitance on the propagation delay of a CMOS inverter. With an in-phase transition, both inverters are assumed to transition from high-to-low. The PMOS transistors are neglected based on an assumption of a fast ramp input signal [69].

The simplified circuit diagram is shown in Figure 6.3. $NMOS_1$ and $NMOS_2$ are the active transistors in each inverter and may have different geometric sizes.

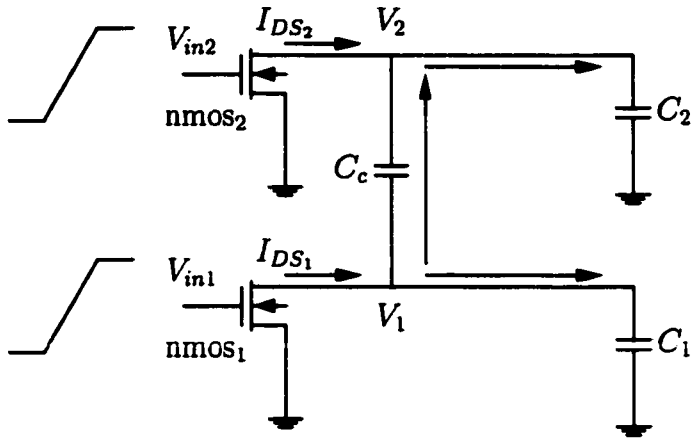


Figure 6.3: Inv_1 and Inv_2 during a high-to-low transition

The shape of the input signals driving both inverters is characterized by

$$V_{in1} = V_{in2} = \frac{t}{\tau_r} V_{dd} \qquad 0 \leq t \leq \tau_r. \tag{6.3}$$

6.3.1 Waveform of the Output Voltages

An assumption of a fast ramp input signal permits the condition that both inverters operate in the saturation region before the input transition is completed. When the input voltage exceeds the threshold voltage V_{TN}, *i.e.*, $t \geq \tau_n$, both of the NMOS transistors are ON and begin operating in the saturation region.

After the input transition is completed, the input voltage is fixed at V_{dd} and both of the NMOS transistors remain in the saturation region. The times at which $NMOS_1$ and $NMOS_2$ leave the saturation region are τ_{nsat1} and τ_{nsat2}, respectively. For the condition where these NMOS transistors are not equally sized, $NMOS_1$ and $NMOS_2$ may leave the saturation region at different times. If $NMOS_1$ leaves the saturation region first after a time τ_{nsat1}, $NMOS_1$ operates in the linear region and the drain-to-source current is approximated by the effective output conductance

Table 6.2: Analytical expressions characterizing the output voltage for an in-phase transition

Operating region	Output voltage $V_1(t)$ and $V_2(t)$
$[\tau_n, \tau_r]$	$V_1 = V_{dd} - \beta_1 \frac{\tau_r}{(n_n+1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1}$ (6.4) $V_2 = V_{dd} - \beta_2 \frac{\tau_r}{(n_n+1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1}$ (6.5) $\beta_1 = \frac{C_c B_{n2} + (C_2+C_c)B_{n1}}{C_1C_2 + C_c(C_1+C_2)}$ (6.6) $\beta_2 = \frac{C_c B_{n1} + (C_1+C_c)B_{n2}}{C_1C_2 + C_c(C_1+C_2)}$ (6.7)
$[\tau_r, \tau_{sat}^{min}]$	$V_1 = V_{dd} - \beta_1(V_{dd} - V_{TN})^{n_n}(t - \frac{n_n V_{dd} + V_{TN}}{(n_n+1)V_{dd}}\tau_r)$ (6.8) $V_2 = V_{dd} - \beta_2(V_{dd} - V_{TN})^{n_n}(t - \frac{n_n V_{dd} + V_{TN}}{(n_n+1)V_{dd}}\tau_r)$ (6.9) $\tau_{sat}^{min} = \min(\tau_{nsat1}, \tau_{nsat2})$ (6.10) $\tau_{sat}^{max} = \max(\tau_{nsat1}, \tau_{nsat2})$ (6.11)
$[\tau_{sat}^{min}, \tau_{sat}^{max}]$	$V_1 = -V_{1_a} + (V_{nsat} + V_{1_a})e^{-\alpha_{n1}(t\tau_{nsat1})}$ (6.12) $V_2 = V_2(\tau_{nsat1}) - V_{2_a}(t - \tau_{nsat1}) - \frac{C_c}{C_2+C_c}(V_{nsat} + V_{1a})$ $(1 - e^{-\alpha_{n1}(t-\tau_{nsat1})})$ (6.13) $V_{1_a} = \frac{C_c}{(C_2+C_c)\gamma_{n1}}B_{n2}(V_{dd} - V_{TN})^{n_n}$ (6.14) $\alpha_{n1} = \frac{C_2+C_c}{C_1C_2 + C_c(C_1+C_2)}\gamma_{n1}$ (6.15) $V_{2_a} = \frac{1}{C_2+C_c}B_{n2}(V_{dd} - V_{TN})^{n_n}$ (6.16)

$\gamma_{n1}V_{DS}$. Expressions characterizing the output voltages are listed in Table 6.2 for $t \leq \tau_{sat}^{max}$ [defined in (6.11)] where in this discussion τ_{sat}^{max} is equal to τ_{nsat2}.

After τ_{nsat2}, both of these transistors operate in the linear region. Both of the NMOS transistors are modeled by the effective output conductance γ_{n1} and γ_{n2}. A general solution of the output voltages is provided in the Appendix A with the initial conditions, $V_1(\tau_l) = V_1(\tau_{nsat2})$ and $V_2(\tau_l) = K_n(V_{dd} - V_{TN})^{m_n}$.

Both β_1 and β_2 described by (6.6) and (6.7), respectively, include the effects of the coupling capacitance C_c and the intrinsic load capacitances C_1 and C_2. If the ratio of B_{n1}/B_{n2} is the same as that of C_1/C_2, *i.e.*, these MOS transistors have the same ratio of the output current drive to the corresponding intrinsic load capacitance, the coupling capacitance has no effect on the waveform of V_1 and V_2 (note that C_c is eliminated from the expressions for β_1 and β_2). In practical CMOS VLSI circuits, this condition cannot be satisfied due to the size difference between the MOS transistors, different interconnect geometric parameters, and different gate capacitances of the following logic stages. Therefore, the coupling capacitance affects the waveform shape of the output voltages, V_1 and V_2. It is therefore necessary to consider the interconnect capacitance so as to determine the proper size of the MOS transistors.

Assuming B_{n1} is equal to B_{n2}, *i.e.*, both NMOS transistors have the same geometric sizes or output gain, the effective load capacitance of each inverter is

$$C_{1_{eff}} = \frac{C_1C_2 + C_c(C_1 + C_2)}{C_2 + 2C_c}, \tag{6.17}$$

$$C_{2_{eff}} = \frac{C_1C_2 + C_c(C_1 + C_2)}{C_1 + 2C_c}. \tag{6.18}$$

The solid lines shown in Figure 6.4 depict the ratio of $C_{1_{eff}}$ to C_1 and the dotted lines represent the ratio of $C_{2_{eff}}$ to C_2. The horizontal axis represents the ratio of C_2 to C_1, which characterizes the difference between the intrinsic load capacitances.

Ratios of coupling capacitance C_c to C_1 of 0.3, 0.5, and 0.7 are considered. Note that the deviation of the effective load capacitances from the intrinsic capacitances (C_1 and C_2) increases if the difference between the intrinsic load capacitances increases. The deviation also increases with increasing coupling capacitance for the same ratio of C_2/C_1.

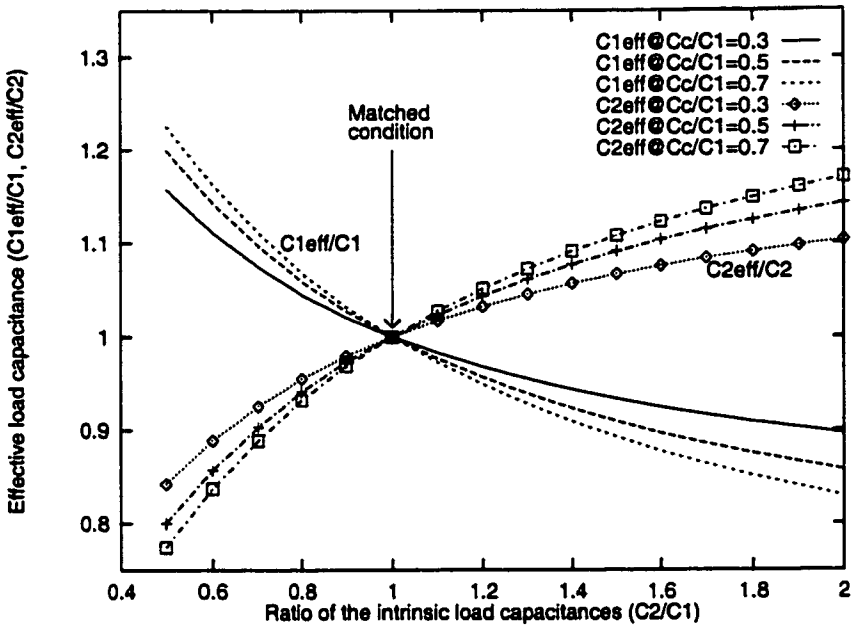


Figure 6.4: The ratio of the effective load capacitances $C_{1_{eff}}$ and $C_{2_{eff}}$ to C_1 and C_2, respectively, for an in-phase transition assuming $B_{n1} = B_{n2}$.

Note in Figure 6.4 that the effective load capacitance of one inverter increases above the corresponding intrinsic load capacitance while the effective load capacitance of the second inverter drops below the corresponding intrinsic load capacitance. The deviation of the effective load capacitances from the intrinsic load capacitances results in different propagation delays.

Note in Figure 6.4 that the effective load capacitance of one inverter increases above the intrinsic load capacitance while the effective load capacitance of the other inverter drops below the intrinsic load capacitance. The difference between

the effective load capacitances results in different propagation delays of these two coupled inverters.

6.3.2 Propagation Delay Time of a Fast Ramp Input Signal

The propagation delay $t_{0.5}$ of a CMOS inverter is defined as the time from 50% V_{dd} of the input to 50% V_{dd} of the output. The high-to-low propagation delays of the CMOS coupled inverters can be approximated as

$$T_{HL1} = \frac{V_{dd}}{2\beta_1(V_{dd} - V_{TN})^{n_n}} + \frac{n_n V_{dd} + V_{TN}}{(n_n + 1)V_{dd}}\tau_r - \frac{\tau_r}{2}, \tag{6.19}$$

$$T_{HL2} = \frac{V_{dd}}{2\beta_2(V_{dd} - V_{TN})^{n_n}} + \frac{n_n V_{dd} + V_{TN}}{(n_n + 1)V_{dd}}\tau_r - \frac{\tau_r}{2}. \tag{6.20}$$

Similarly, the low-to-high propagation delays of the coupled inverters can be similarly determined.

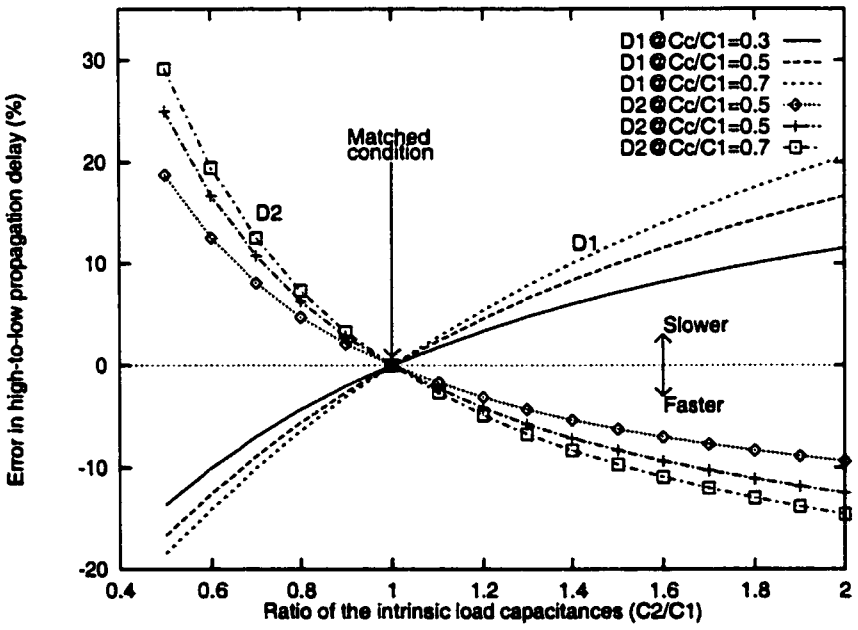


Figure 6.5: Deviation of the high-to-low propagation delay from the estimate based on C_1 and C_2, for an in-phase transition assuming $B_{n1} = B_{n2}$.

The effect of the coupling capacitance on the propagation delay is similar to the analysis of the effective load capacitances, which is summarized in Figure 6.5. If the error is positive (negative), the delay is greater (less) than the delay estimated based on C_1 or C_2. For the condition of $C_c/C1 = 0.5$ and $C_2/C_1 = 1.5$, the error of the propagation delays is about 10% for $NMOS_1$ and -8.3% for $NMOS_2$ as compared to an estimate based on the intrinsic load capacitances.

6.3.3 Propagation Delay of a Slow Ramp Input Signal

In the previous discussion, the analyses are based on an assumption of a fast ramp input signal, *i.e.*, the NMOS transistors remains in the saturation region before the input transition is completed. If τ_r is greater than $\min(\tau_{nsat1}, \tau_{nsat2})$, *i.e.*, one of these two NMOS transistors enters the linear region before the input transition is completed, the input signal is characterized as a slow ramp signal.

For a slow ramp input signal, the output voltages of these coupled inverters are also described by (6.4) and (6.5) after both of the NMOS transistors are ON. τ_{nsat1} and τ_{nsat2} are the times when $NMOS_1$ and $NMOS_2$ leave the saturation region, respectively, but in this case these times are calculated based on

$$V_{nsat} = V_{dd} - \beta_1 \frac{\tau_r}{(n_n+1)V_{dd}} (\frac{\tau_{nsat1}}{\tau_r} V_{dd} - V_{TN})^{n_n+1}, \tag{6.21}$$

$$V_{nsat} = V_{dd} - \beta_2 \frac{\tau_r}{(n_n+1)V_{dd}} (\frac{\tau_{nsat2}}{\tau_r} V_{dd} - V_{TN})^{n_n+1}, \tag{6.22}$$

where

$$V_{nsat} = K_n (\frac{t}{\tau_r} V_{dd} - V_{TN})^{m_n}. \tag{6.23}$$

Both τ_{nsat1} and τ_{nsat2} can be obtained from applying a Newton-Raphson numerical solver.

The time when the output voltages V_1 and V_2 reach $0.5V_{dd}$ can be approximated from (6.4) and (6.5),

$$t_{1_{0.5}} = [(\frac{V_{dd}^2(n_n+1)}{2\beta_1\tau_r})^{\frac{1}{n_n+1}} + V_{TN}]\frac{\tau_r}{V_{dd}}, \tag{6.24}$$

$$t_{2_{0.5}} = [(\frac{V_{dd}^2(n_n+1)}{2\beta_2\tau_r})^{\frac{1}{n_n+1}} + V_{TN}]\frac{\tau_r}{V_{dd}}. \tag{6.25}$$

In the derivation of $t_{1_{0.5}}$ and $t_{2_{0.5}}$, the PMOS transistors are neglected. In order to accurately estimate the propagation delay for a slow ramp input signal, some modifications are necessary and the high-to-low propagation delay is approximated as

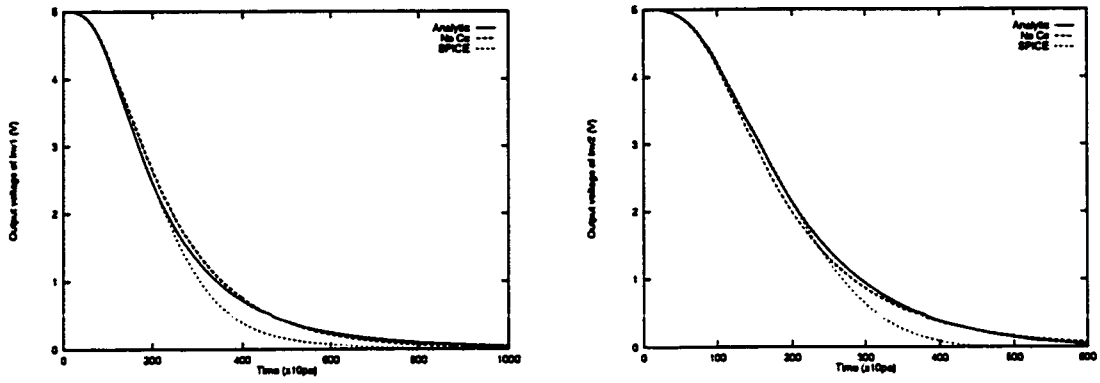
$$T_{HL1} = \frac{\tau_r}{\tau_{nsat1}}(t_{1_{0.5}} - \frac{\tau_r}{2}) \tag{6.26}$$

$$T_{HL2} = \frac{\tau_r}{\tau_{nsat2}}(t_{2_{0.5}} - \frac{\tau_r}{2}), \tag{6.27}$$

where the ratio τ_r/τ_{nsat1} or τ_r/τ_{nsat1} characterizes how far the input signal deviates from a fast ramp input signal. Therefore, the high-to-low propagation delays for both the fast ramp and slow ramp signals are described analytically in (6.19), (6.20), (6.26) and (6.27) for these coupled inverters.

6.3.4 Comparison with SPICE

The waveform of the output voltage of each inverter are compared with SPICE simulation in Figure 6.6. The condition of *No Cc* describes the case where the delays are estimated based on the intrinsic load capacitance, $C1$ and C_2, respectively. The long tail of the analytical result is caused by the output conductance of the MOS transistors in the linear region changing from γ_{sat} to $2\gamma_{sat}$. In the derivation, the output conductance is assumed to be γ_{sat}. However, note that the analytical result is quite close to SPICE during most of this region.



(a) Output voltage of Inv1

(b) Output voltage of Inv2

Figure 6.6: Comparison of the output voltage with SPICE simulation with $w_{n1} = 1.8\,\mu$m, $w_{n2} = 2.4\,\mu$m, $C_1 = 1.0\,$pF, $C_2 = 1.0\,$pF, and $Cc = 0.6\,$pF

A comparison of the propagation delay based on these analytical expressions with SPICE is listed in Table 6.3. The delay is estimated based on the intrinsic load capacitance, *i.e.*, C_1 and C_2, respectively, for the no coupling condition.

Note that the error of the delay based on the intrinsic load capacitance can reach 48% while the delay based on the analytical equations (6.19) and (6.20) is within 1% as compared to SPICE simulation.

6.4 Out-of-Phase Transition

The out-of-phase transition has the same probability as the in-phase transition. The out-of-phase transition is a pessimistic condition in terms of the effect of the coupling capacitance on the propagation delay of the CMOS inverters. It is assumed that Inv_1 transitions from high-to-low while Inv_2 transitions from low-to-high. A simplified circuit schematic is shown in Figure 6.7. $NMOS_1$ and $PMOS_2$

Table 6.3: Comparison of the in-phase transition with SPICE

	Size of Inv		Load Capacitance			SPICE		No Coupling				Analytic			
τ_r (ns)	W_{n1} (μm)	W_{n2} (μm)	C_1 (pF)	C_2 (pF)	C_c (pF)	τ_1 (ns)	τ_2 (ns)	τ_1 (ns)	τ_2 (ns)	δ_1 %	δ_2 %	τ_1 (ns)	τ_2 (ns)	δ_1 %	δ_2 %
1.0	1.8	1.8	1.0	1.0	0.4	1.60	1.60	1.60	1.60	< 1.0	< 1.0	1.60	1.60	<1.0	< 1.0
1.0	1.8	1.8	0.8	1.0	0.3	1.29	1.25	1.30	0.65	< 1.0	48.0	1.29	1.24	<1.0	< 1.0
0.8	1.8	2.4	1.2	0.8	0.4	1.53	1.45	1.57	1.02	2.6	29.7	1.54	1.45	<1.0	< 1.0
1.0	2.4	1.8	1.2	0.8	0.4	1.43	1.35	1.45	0.78	1.7	42.0	1.42	1.34	<1.0	< 1.0
1.0	1.8	3.6	0.5	1.5	0.5	1.29	1.25	1.30	0.65	< 1.0	48.2	1.28	1.24	<1.0	< 1.0
1.0	1.8	3.6	1.0	1.0	0.8	1.27	1.00	1.60	0.62	25.6	38.2	1.28	1.00	<1.0	< 1.0

are the active transistors in each inverter. The input signals are

$$V_{in1} = \frac{t}{\tau_r} V_{dd} \qquad 0 \le t \le \tau_r, \tag{6.28}$$

$$V_{in2} = (1 - \frac{t}{\tau_r}) V_{dd} \qquad 0 \le t \le \tau_r. \tag{6.29}$$

The initial states of V_1 and V_2 are V_{dd} and ground, respectively.

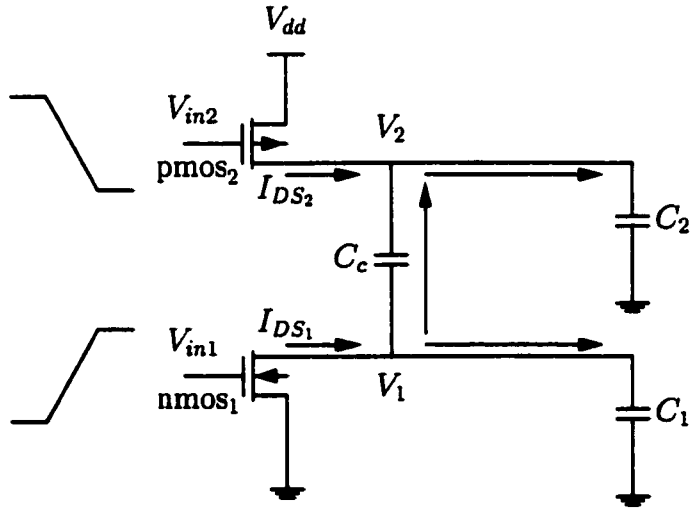


Figure 6.7: Inv_1 transitions from high-to-low and Inv_2 transitions from low-to-high.

6.4.1 Waveform of the Output Voltages

Table 6.4: Analytical expressions characterizing the output voltages for an out-of-phase transition

Operating region	Output voltage $V_1(t)$ and $V_2(t)$
$[\tau_n(\tau_p), \tau_r]$	$V_1 = V_{dd} - \frac{(C_2 + C_c)V_{n,1} - C_c V_{p,1}}{C_1C_2 + C_c(C_1 + C_2)}$ (6.30) $V_2 = \frac{(C_1 + C_c)V_{p,1} - C_c V_{n,1}}{C_1C_2 + C_c(C_1 + C_2)}$ (6.31) $V_{n,1} = B_{n1}\frac{\tau_r}{(n_n + 1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1}$ (6.32) $V_{p,1} = B_{p2}\frac{\tau_r}{(n_p + 1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p+1}$ (6.33)
$[\tau_r, \tau_{sat}^{min}]$	$V_1 = V_{dd} - \frac{(C_2 + C_c)V_{n,2} - C_c V_{p,2}}{C_1C_2 + C_c(C_1 + C_2)}$ (6.34) $V_2 = \frac{(C_1 + C_c)V_{p,2} - C_c V_{n,2}}{C_1C_2 + C_c(C_1 + C_2)}$ (6.35) $V_{n,2} = B_{n1}(V_{dd} - V_{TN})^{n_n}(t - \frac{n_n V_{dd} + V_{TN}}{(n_n + 1)V_{dd}}\tau_r)$ (6.36) $V_{p,2} = B_{p2}(V_{dd} - V_{TP})^{n_p}(t - \frac{n_p V_{dd} + V_{TP}}{(n_p + 1)V_{dd}}\tau_r)$ (6.37) $\tau_{sat}^{min} = \min(\tau_{nsat1}, \tau_{psat2})$ (6.38) $\tau_{sat}^{max} = \max(\tau_{nsat1}, \tau_{sat2})$ (6.39)

It is assumed that the absolute value of the threshold voltages of both of the NMOS and PMOS transistors are approximately equal. In the following analysis, all of the parameters describing the PMOS voltages are absolute values. When t is greater than τ_n, both $NMOS_1$ and $PMOS_2$ are ON and operate within the saturation region. Note in (6.30) and (6.31) that the coupling component $V_{p,1}$

in (6.30) causes V_1 to decrease slowly while the coupling component $V_{n,1}$ in (6.31) causes V_2 to increase slowly. The solutions of the output voltage V_1 and V_2 are listed in Table 6.4 before one of these transistors operates in the linear region.

Assuming $V_{n,1}$ is equal to $V_{p,1}$, the effective load capacitances of $NMOS_1$ and $PMOS_2$ are

$$C_{1_{eff}} = \frac{C_1C_2 + C_c(C_1 + C_2)}{C_2}, \tag{6.40}$$

$$C_{2_{eff}} = \frac{C_1C_2 + C_c(C_1 + C_2)}{C_1}. \tag{6.41}$$

If C_1 is identical to C_2, $C_{1_{eff}}$ and $C_{2_{eff}}$ are equal to $C_1 + 2C_c$ or $C_2 + 2C_c$. The solid lines shown in Figure 6.8 describe the ratio of $C_{1_{eff}}$ to $C_1 + 2C_c$, and the dotted lines depict the ratio of $C_{2_{eff}}$ to $C_2 + 2C_c$. The horizontal axis represents the ratio of C_2 to C_1, and ratios of C_c to C_1 of 0.3, 0.5, and 0.7 are considered for each condition. Note that the effective load capacitance of Inv_1 (Inv_2) may not be equal to $C_1 + 2C_c$ ($C_2 + 2C_c$) due to the difference between the load capacitances.

It is assumed in this discussion that the situation, $[(C_2 + C_c)V_{n,11} - C_cV_{p,1}] < 0$ or $[(C_1 + C_c)V_{p,1} - C_cV_{n,1}] < 0$, does not occur. This situation can occur if one transistor has a much stronger output drive current than another, *i.e.*, $V_{n,1} \gg V_{p,1}$ or $V_{n,1} \ll V_{p,1}$, while C_c is comparable to C_1 or C_2. Under this condition, V_1 and V_2 may be greater than V_{dd} or less than ground, permitting overshoots or undershoots to occur.

When the input signal reaches V_{dd} at τ_r, both $NMOS_1$ and $PMOS_2$ continue to operate in the saturation region. For a nonideal condition in which $NMOS_1$ and $PMOS_2$ are not sized equally, $NMOS_1$ and $PMOS_2$ may leave the saturation region at different times. The analysis after $\min(\tau_{nsat1}, \tau_{psat2})$ is the same as that of the in-phase transition.

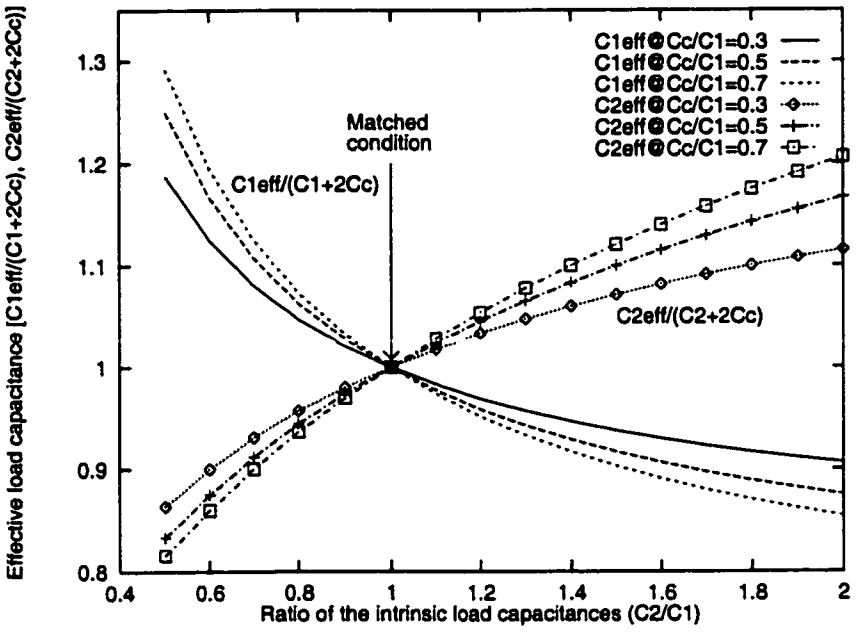


Figure 6.8: The ratio of the effective load capacitances $C_{n1_{eff}}$ and $C_{n2_{eff}}$ to C_1+2C_c and C_2+2C_c, respectively, for an out-of-phase transition assuming $B_{n1} = B_{p2}$.

6.4.2 Propagation Delay Time

For a fast ramp input signal, $t_{0.5}$ can be approximated by (6.30) and (6.31). The effect of the coupling capacitance on the propagation delay is analyzed based on the following assumptions: $V_{TN} = V_{TP}$, $n_n = n_p$, and $B_{n1} = B_{p2}$. The difference between the delays calculated based on (6.40) and (6.41), and the delays calculated based on the load capacitances of $C_1 + 2C_c$ and $C_2 + 2C_c$ are shown in Figure 6.9. The test condition is the same as that of the in-phase transition.

For a slow ramp input signal, $NMOS_1$ and $PMOS_2$ begin operating in the linear region before the input signal transition is completed. The output voltages of these coupled inverters can also be described by (6.30) and (6.31). The propagation delay of a slow ramp input signal can be determined the same way as the in-phase transition.

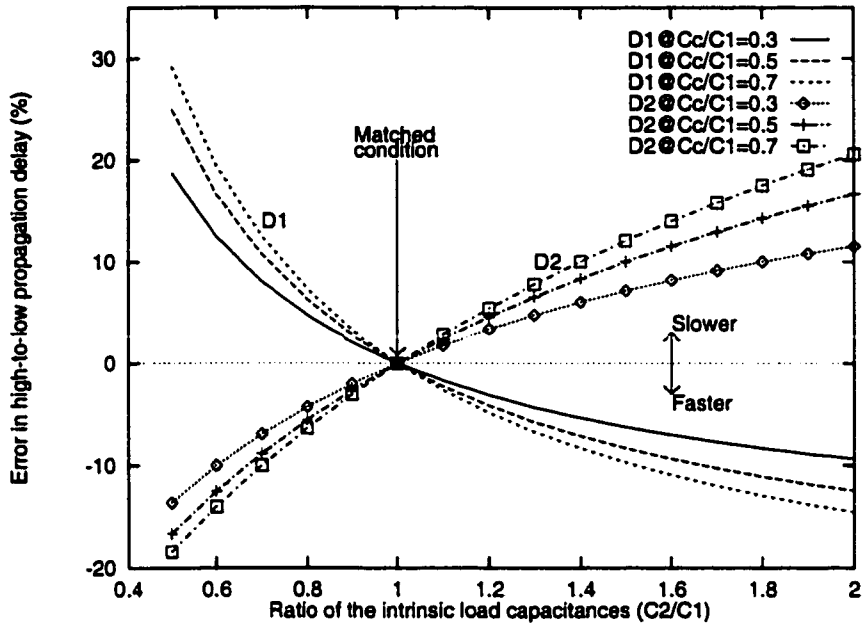


Figure 6.9: Deviation of the propagation delay from the estimate based on C_1+2C_c and C_2+2C_c, for an out-of-phase transition assuming $B_{n1} = B_{p2}$.

6.4.3 Comparison with SPICE

The waveform of the output voltage of Inv_1 is compared with SPICE in Figure 6.10. The condition of *No Cc* describes the case where the delays are estimated based on an intrinsic load capacitance $C1 + 2C_c$. Note that the analytical result is quite close to SPICE.

A comparison of these analytical expressions with SPICE simulation is listed in Table 6.5. The delay is estimated based on the intrinsic load capacitance plus two times the coupling capacitance, *i.e.*, $C_1 + 2C_c$ and $C_2 + 2C_c$, respectively, for the no coupling condition. Note that the error of the delay based on $C_1 + 2C_c$ and $C_2 + 2C_c$ can reach 16% while the delay based on the analytical equation listed in Table 6.4 is within 3% as compared to SPICE simulation.

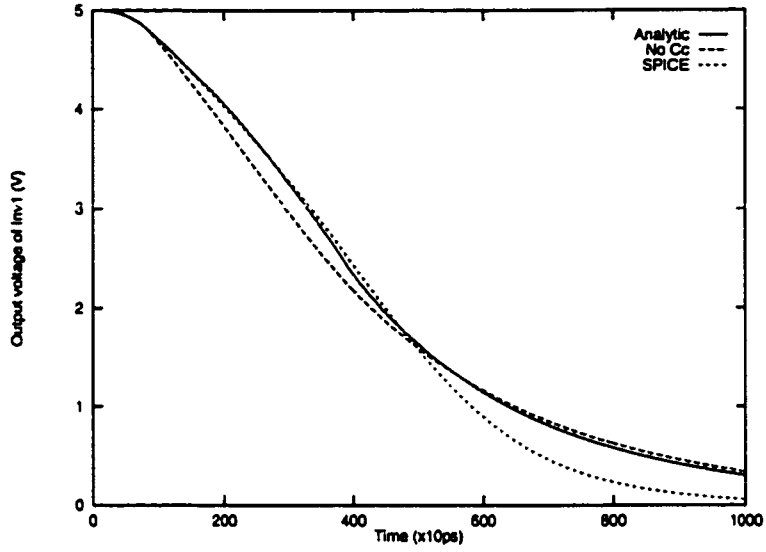


Figure 6.10: Comparison of the output voltage with SPICE simulation with $w_{n1} = 1.8\,\mu$m, $w_{n2} = 2.4\,\mu$m, $C_1 = 1.0\,$pF, $C_2 = 1.0\,$pF, and $Cc = 0.5\,$pF

Table 6.5: Comparison of out-of-phase transition with SPICE

	Size of Inv		Load Capacitance			SPICE		No Coupling				Analytic			
τ_r (ns)	W_{n1} (μm)	W_{n2} (μm)	C_1 (pF)	C_2 (pF)	C_c (pF)	τ_1 (ns)	τ_2 (ns)	τ_1 (ns)	τ_2 (ns)	δ_1 %	δ_2 %	τ_1 (ns)	τ_2 (ns)	δ_1 (ns)	δ_2 %
1.0	1.8	1.8	1.0	1.0	0.4	2.80	2.62	2.77	2.52	1.1	3.8	2.80	2.64	< 1.0	< 1.0
1.0	1.8	2.4	0.8	1.0	0.3	3.04	1.87	2.75	1.80	9.5	3.7	2.96	1.92	2.6	2.6
1.0	2.4	2.4	1.5	0.8	0.4	2.89	1.65	2.64	1.61	8.6	2.4	2.83	1.69	2.1	2.4
1.0	2.4	2.4	1.5	0.8	0.8	3.96	2.24	3.49	2.30	11.8	2.7	3.90	2.22	1.5	< 1.0
1.0	2.4	3.6	1.0	1.5	1.0	3.97	2.21	3.35	2.22	15.6	< 1.0	3.89	2.21	2.0	< 1.0

6.5 One Inverter Active and the Other Quiet

The condition where one inverter is active and the other is quiet has the highest probability of occurrence. For the in-phase and out-of-phase transitions, the coupling capacitance affects the waveform of the output voltage and the propagation delay of each inverter. If one inverter is active and the other is quiet, the active transition can induce a voltage change at the quiet inverter through the coupling capacitance. The coupling noise voltage may therefore seriously affect the circuit behavior and power consumption.

In the following analysis, Inv_1 is assumed to transition from high-to-low while the input of Inv_2 is fixed at V_{dd}. Therefore, the initial voltage of V_1 and V_2 are V_{dd} and ground, respectively. A simplified circuit model, shown in Figure 6.11, is used

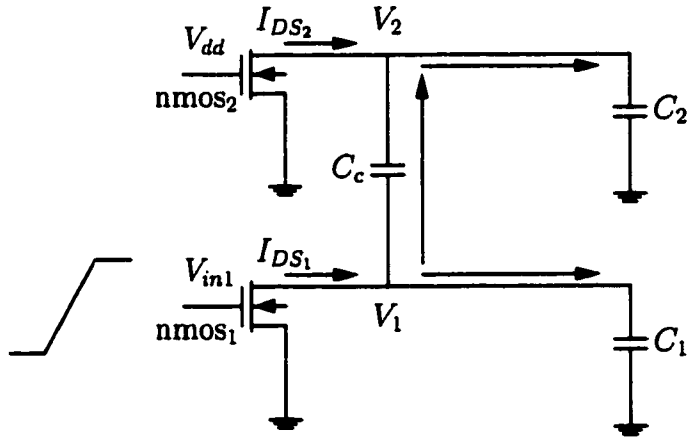


Figure 6.11: Inv_1 transitions from high-to-low and Inv_2 is quiet.

to analyze the coupling noise voltage at the quiet inverter and the propagation delay of the active inverter. The signal at the input of Inv_1 is

$$V_{in1} = \frac{t}{\tau_r} V_{dd} \qquad 0 \leq t \leq \tau_r. \tag{6.42}$$

When the input voltage exceeds V_{TN}, $NMOS_1$ is ON and starts to operate in the saturation region. $NMOS_2$ starts to operate in the linear region due to the voltage change at the output. The differential equations, (6.1) and (6.2), therefore change to

$$(C_1 + C_c)\frac{dV_1}{dt} - C_c\frac{dV_2}{dt} = -B_{n1}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}, \tag{6.43}$$

$$(C_2 + C_c)\frac{dV_2}{dt} - C_c\frac{dV_1}{dt} = -\gamma_{n2}V_2, \tag{6.44}$$

where $\tau_n \leq t \leq \tau_r$. There are no tractable solutions to these coupled differential equations. In order to derive a tractable solutions, it is necessary to make certain simplifying assumptions.

6.5.1 Step Input Approximation

If the transition time of the input signal is small as compared to the delay of the CMOS inverters and the output transition time, the input can be approximated as a step input.

The output voltages are

$$V_1 = V_{dd} - \frac{B_{n1}}{C_1 + C_c}(V_{dd} - V_{TN})^{n_n}t + \frac{C_c}{C_1 + C_c}V_2, \tag{6.45}$$

$$V_2 = -\frac{C_c}{(C_1 + C_c)\gamma_{n2}}B_{n1}(V_{dd} - V_{TN})^{n_n}(1 - e^{-\alpha_{n2}t}) \tag{6.46}$$

where

$$\alpha_{n2} = \frac{C_1 + C_c}{C_1C_2 + C_c(C_1 + C_2)}\gamma_{n2}. \tag{6.47}$$

The time τ_{nsat1} when $NMOS_1$ leaves the saturation region can be determined from (6.45) by using a Newton-Raphson iteration. After τ_{nsat1}, $NMOS_1$ operates in the linear region.

The propagation delay of Inv_1 can be approximated using (6.45) and a Newton-Raphson iteration. Since the current through $NMOS_2$ discharges the capacitor C_1, the propagation delay is less than the delay estimated based on $C_1 + C_c$.

After τ_{nsat1}, both of the NMOS transistors operate in the linear region. The solutions for the peak voltage can be obtained from the initial values of V_1 and V_2, as described in the Appendix A. Note that V_2 decreases exponentially in the linear region and the peak noise occurs at τ_{nsat1},

$$V_2(peak) = -\frac{C_c}{(C_1 + C_c)\gamma_{n2}} B_{n1}(V_{dd} - V_{TN})^{n_n}(1 - e^{-\alpha_{n2}\tau_{nsat1}}). \tag{6.48}$$

6.5.2 Current through $NMOS_2$ Is Negligible

The analysis described in this section is based on the assumption that the current through $NMOS_2$ can be neglected, *i.e.*, $\gamma_{n2}V_2$ is small as compared to $C_c\frac{dV_1}{dt}$. The solutions of V_1 and V_2 are

$$V_1 = V_{dd} - \beta_1 \frac{\tau_r}{(n_n + 1)V_{dd}} (\frac{t}{\tau_r} V_{dd} - V_{TN})^{n_n+1}, \tag{6.49}$$

$$V_2 = -\beta_2 \frac{\tau_r}{(n_n + 1)V_{dd}} (\frac{t}{\tau_r} V_{dd} - V_{TN})^{n_n+1}, \tag{6.50}$$

where $\tau_n \leq t \leq \tau_r$ and

$$\beta_1 = \frac{C_2 + C_c}{C_1C_2 + C_c(C_1 + C_2)} B_{n1}, \tag{6.51}$$

$$\beta_2 = \frac{C_c}{C_1C_2 + C_c(C_1 + C_2)} B_{n1}. \tag{6.52}$$

The effective load capacitance of Inv_1 is

$$C_{1_{eff}} = (C1 + \frac{C_2}{C_2 + C_c} C_c) < (C_1 + C_c). \tag{6.53}$$

When the input signal reaches V_{dd} at τ_r, $NMOS_1$ still operates in the saturation region. However, the coupling noise voltage V_2 at τ_r is

$$V_2(\tau_r) = -\beta_2 \frac{\tau_r}{(n_n + 1)V_{dd}} (V_{dd} - V_{TN})^{n_n+1}. \tag{6.54}$$

Note that $\gamma_2 V_2$ cannot be neglected after the input transition is completed since $\gamma_2 V_2$ may be comparable to $C_c \frac{dV_1}{dt}$. Therefore, the output voltages are

$$V_1 = V_{dd} - \frac{1}{C_1 + C_c} B_{n1} V_{n1_a} - \frac{C_c}{C_1 + C_c} V_{n1_b}, \tag{6.55}$$

$$V_2 = -V_{n2_a} + (V_2(\tau_r) + V_{n2_a}) e^{-\alpha_{n2}(t-\tau_r)}, \tag{6.56}$$

for $\tau_r \leq t \leq \tau_{nsat1}$ and where

$$V_{n1_a} = (V_{dd} - V_{TN})^{n_n} (t - \frac{n_n V_{dd} + V_{TN}}{(n_n + 1) V_{dd}} \tau_r), \tag{6.57}$$

$$V_{n1_b} = (V_2(\tau_r) + V_{n2a})(1 - e^{-\alpha_{n2}(t-\tau_r)}), \tag{6.58}$$

$$V_{n2_a} = \frac{C_c}{(C_1 + C_c)\gamma_{n2}} B_{n1} (V_{dd} - V_{TN})^{n_n}, \tag{6.59}$$

$$\alpha_{n2} = \gamma_{n2} \frac{C_1 + C_c}{C_1 C_2 + C_c (C_1 + C_2)}. \tag{6.60}$$

τ_{nsat1} and $t_{0.5}$ are determined from (6.55) by applying a Newton-Raphson iteration. The peak coupling noise voltage can be approximated at τ_{nsat1} for this case and is equal to $V_2(\tau_{nsat1})$ as determined by (6.56).

6.5.3 Approximation of the Drain-Source Current

The simplification in which the current through $NMOS_2$ is neglected is appropriate when $\gamma_{n2} V_2$ is small as compared to $C_c \frac{dV_1}{dt}$. If $\gamma_{n2} V_2$ is comparable to $C_c \frac{dV_1}{dt}$, the current through $NMOS_2$ cannot be neglected.

In order to derive tractable solutions, the drain-to-source current of $NMOS_1$ can be approximated using a second order polynomial expansion,

$$B_{n1} (\frac{t}{\tau_r} V_{dd} - V_{TN})^{n_n} \approx A_0 + A_1 \xi + A_2 \xi^2, \tag{6.61}$$

where $\xi = \frac{t}{\tau_r} - \frac{V_{TN}}{V_{dd}}$ and A_0, A_1, and A_2 are determined by a polynomial expansion.

The solutions of the differential equations represented by (6.43) and (6.44) are

$$V_1 = V_{dd} - \frac{1}{C_1 + C_c} V_{1_a} + \frac{C_c}{C_1 + C_c} V_2, \tag{6.62}$$

$$V_2 = B_1 \xi + B_2 \xi^2 + (1 - B_0) e^{-\alpha_{n2}(t - \tau_n)}, \tag{6.63}$$

where

$$V_{1_a} = B_{n1} \frac{\tau_r}{(n_n + 1) V_{dd}} (\frac{t}{\tau_r} V_{dd} - V_{TN})^{n_n + 1}, \tag{6.64}$$

and

$$B_0 = - \frac{C_c}{(C_1 + C_c)\gamma_{n2}} A_0 + \frac{C_c C_t}{(C_1 + C_c)^2 \gamma_{n2}^2 \tau_r} A_1 - 2 \frac{C_c C_t^2}{(C_1 + C_c)^3 \gamma_{n2}^3 \tau_r^2} A_2, \tag{6.65}$$

$$B_1 = 2 \frac{C_c C_t}{(C_1 + C_c)^2 \gamma_{n2}^2 \tau_r} A_2 - \frac{C_c}{(C_1 + C_c)\gamma_{n2}} A_1, \tag{6.66}$$

$$B_2 = - \frac{C_c}{(C_1 + C_c)\gamma_{n2}} A_2, \tag{6.67}$$

where $C_t = C_1 C_2 + C_c(C_1 + C_2)$ and $\tau_n \leq t \leq \tau_r$.

After the input transition is completed, $NMOS_1$ still operates in the saturation region. The output voltages are

$$V_1 = V_{dd} - \frac{1}{C_1 + C_c} V_{1_a} - \frac{C_c}{C_1 + C_c} V_{1_b}, \tag{6.68}$$

$$V_2 = -V_{2_a} + (V_2(\tau_r) + V_{2_a}) e^{-\alpha_{n2}(t - \tau_r)}, \tag{6.69}$$

where

$$V_{1_a} = (V_{dd} - V_{TN})^{n_n} (t - \frac{n_n V_{dd} + V_{TN}}{(n_n + 1) V_{dd}} \tau_r), \tag{6.70}$$

$$V_{1_b} = \frac{C_c}{(C_1 + C_c)\gamma_{n2}} B_{n1} (V_{dd} - V_{TN})^{n_n}, \tag{6.71}$$

$$V_{2_a} = \frac{C_c}{(C_1 + C_c)\gamma_{n2}} B_{n1} (V_{dd} - V_{TN})^{n_n}. \tag{6.72}$$

$V_2(\tau_r)$ can be determined from (6.63). τ_{nsat1} and $t_{0.5}$ can also be determined from (6.68) using a Newton-Raphson iteration. V_2 exhibits an exponential decay when both transistors operate in the linear region. Therefore, the peak coupling noise can be approximated at τ_{nsat1}.

6.5.4 Delay Uncertainty of the Active Logic Gate

In the previous analysis, Inv_1 is assumed to transition from high-to-low and the input of Inv_2 is fixed at V_{dd}. Note that the current through $NMOS_2$ discharges C_1, and the estimated delay is smaller than the estimate based on $C_1 + C_c$. If the input of Inv_2 is at ground and $PMOS_2$ is ON, the coupling capacitance affects the propagation delay of Inv_1 differently.

The effect of the initial state can be demonstrated with a step input signal. If the initial values of both V_1 and V_2 are V_{dd}, since $NMOS_1$ operates in the saturation region, the output voltages are

$$V_1 = V_{dd} - \frac{B_{n1}}{C_1 + C_c}(V_{dd} - V_{TN})^{n_n} t + \frac{C_c}{C_1 + C_c} V_{p2}, \tag{6.73}$$

$$V_2 = V_{dd} - \frac{C_c B_{n1}(V_{dd} - V_{TN})^{n_n}}{(C_1 + C_c)\gamma_{p2}}(1 - e^{-\alpha_{p2} t}), \tag{6.74}$$

where

$$V_{p2} = \frac{C_c}{C_1 + C_c} B_{n1}(V_{dd} - V_{TN})^{n_n}(1 - e^{-\alpha_{p2} t}), \tag{6.75}$$

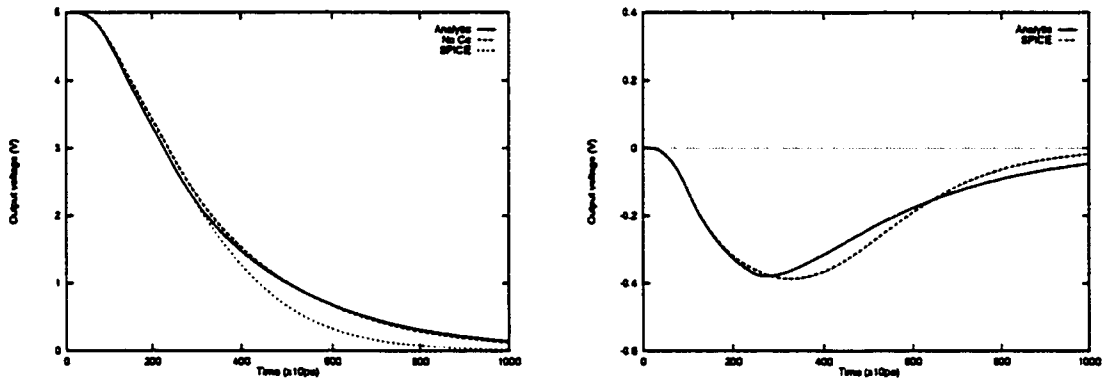
$$\alpha_{p2} = \gamma_{p2} \frac{C_1 + C_c}{C_1 C_2 + C_c(C_1 + C_2)}. \tag{6.76}$$

The propagation delay of Inv_1 can be approximated from (6.73). Since the current through $PMOS_2$ slows down the discharge process, the propagation delay is greater than the the delay calculated from $C_1 + C_c$. The peak coupling noise voltage also occurs at the time when $NMOS_1$ leaves the saturation region. A similar analysis can also be applied for a fast ramp input signal.

Undershoots are exhibited when the active inverter transitions from high to low and the quiet state is at a logic low (ground). Overshoots may occur when the active inverter transitions from low to high and the quiet state is at a logic high (V_{dd}). Overshoots or undershoots may cause carrier injection or collection in the substrate, possibly corrupting data in dynamic circuits [18].

6.5.5 Comparison with SPICE

The output voltage waveform of each inverter is compared with SPICE simulation in Figure 6.12. The condition of *No Cc* describes the case where the delays are estimated based on an intrinsic load capacitance, $C1 + C_c$ or $C_2 + C_c$. Note



(a) Output voltage of Inv1

(b) Output voltage of Inv2

Figure 6.12: Comparison of the output voltage with SPICE simulation with $w_{n1} = 1.8\,\mu$m, $w_{n2} = 1.8\,\mu$m, $C_1 = 1.0\,$pF, $C_2 = 1.0\,$pF, and $Cc = 0.4\,$pF

that the analytical result is quite close to SPICE.

A comparison of the analytical expressions with SPICE simulation is listed in Table 6.6. The delay is estimated based on the intrinsic load capacitance plus the coupling capacitance, *i.e.*, $C_1 + C_c$ or $C_2 + C_c$, for the no coupling condition.

Table 6.6: Comparison of Inv_1 active and Inv_2 quiet with SPICE

	Size of Inv		Load Capacitance			Initial	Delay of Inv1					Peak voltage of Inv2		
							SPICE	No Coupling		Analytic		SPICE	Analytic	
τ_r (ns)	W_{n1} (μm)	W_{n2} (μm)	C_1 (pF)	C_2 (pF)	C_c (pF)	state of Inv2	τ_1 (ns)	τ_1 (ns)	δ_1 %	τ_1 (ns)	δ_1 %	V_2 (V)	V_2 (V)	δ_2 %
1.0	1.8	1.8	1.0	1.0	0.4	Low	2.11	2.18	3.3	2.11	<1.0	-0.328	-0.32	2.4
1.0	1.8	1.8	1.0	1.0	0.4	High	2.09	2.18	4.3	2.09	<1.0	4.58	4.61	<1.0
1.0	1.8	2.4	1.0	1.0	0.4	Low	2.12	2.18	2.8	2.12	<1.0	-0.258	-0.26	<1.0
1.0	1.8	2.4	1.0	1.0	0.4	High	2.10	2.18	3.8	2.11	<1.0	4.67	4.68	<1.0
1.0	1.8	1.8	1.0	1.0	0.8	Low	2.52	2.77	9.9	2.52	<1.0	-0.528	-0.51	3.4
1.0	1.8	1.8	1.0	1.0	0.8	High	2.47	2.77	12.1	2.48	<1.0	4.32	4.38	1.4
1.0	1.8	2.4	1.0	1.0	0.8	Low	2.57	2.77	7.8	2.57	<1.0	-0.414	-0.42	1.5
1.0	1.8	2.4	1.0	1.0	0.8	High	2.52	2.77	9.9	2.53	<1.0	4.46	4.49	<1.0

Note that the error of the delay based on C_1+C_c or C_2+C_c can reach 16% while the delay based on the analytical equation is within 3% as compared to SPICE. The peak noise based on the analytical expression is within 4% as compared to SPICE

6.6 Minimizing Coupling Effects

Coupling effects can be minimized or even eliminated if the circuit elements are appropriately sized for an in-phase transitions, as discussed in Section 6.3.1. For an out-of-phase transition, the coupling capacitance has a strong effect on the propagation delay. If the circuit elements are proportionally sized, *i.e.*, B_{n1}/C_1 is equal to B_{n2}/C_2, the effective load capacitances from $C_1 + 2C_c$ and $C_2 + 2C_c$ are still different. The ratio of the effective load capacitances to $C_1 + 2C_c$ and $C_2 + 2C_c$ for this condition are shown in Figure 6.13 as the solid lines and dotted lines, respectively. The horizontal axis represents the ratio of C_2 to C_1.

Any uncertainty can be eliminated when both of the inverters and load capacitances are the same, $B_{n1} = B_{n2}$ and $C_1 = C_2$. To reduce the propagation delay of the coupled inverters, the probability of an out-of-phase transition should be minimized because of the large effective load capacitance. In order to minimize any delay uncertainty, all of these circuit elements should be designed as similar to each other as possible.

The coupling noise voltage is proportional to B_{n1}/γ_{n2} and C_c, as described in (6.48). If the effective output conductance of the quiet inverter is increased, the peak noise voltage can be reduced. This conclusion suggests that the size of the MOS transistors within the quiet inverter should be increased, contradicting the observation for the propagation delay. Therefore, a tradeoff exists in choosing

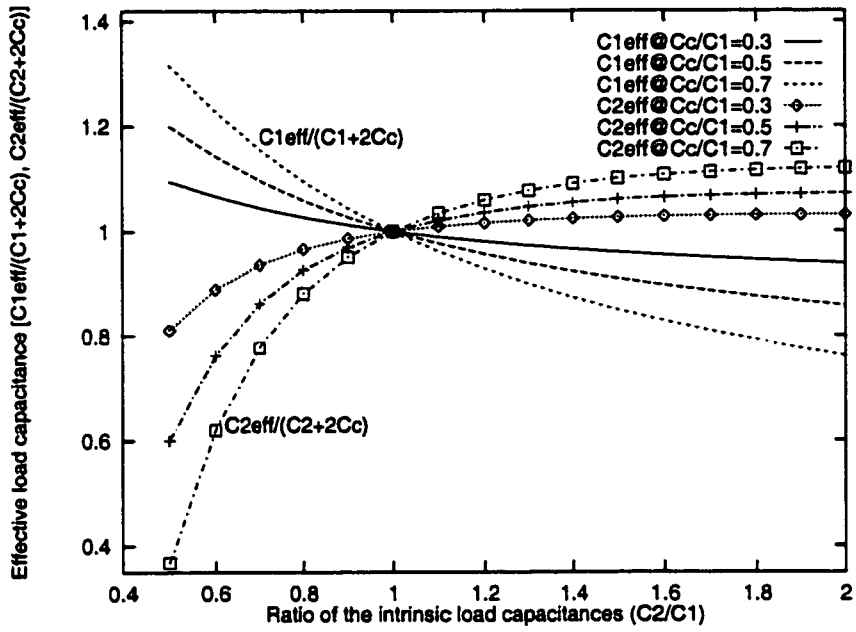


Figure 6.13: The ratio of the effective load capacitances $C_{n1_{eff}}$ and $C_{n2_{eff}}$ to C_1+2C_c and C_2+2C_c, respectively, assuming $\frac{B_{n1}}{C_1} = \frac{B_{n2}}{C_2}$

the appropriate size of the transistors for capacitively coupled inverters. The optimal size of these transistors is also related to the signal activity and other circuit constraints.

6.7 Summary

An analysis of capacitively coupled CMOS inverters is presented in this chapter. The uncertainty of the effective load capacitance and the propagation delay is noted for both in-phase and out-of-phase transitions if the circuit elements are not sized the same. The coupling noise voltage at the interconnection driven by the quiet inverter is also analyzed. Finally, some design strategies are suggested to reduce the effects of the interconnect coupling capacitance.

Chapter 7

Coupled Resistive-Capacitive Interconnections

7.1 Introduction

In most current integrated circuit (IC) design processes, coupling effects cannot be accurately estimated until the physical layout of a CMOS integrated circuit is determined. Therefore, several design iterations may be required to minimize the effects of interconnect coupling capacitance to satisfy a target performance requirement [22, 34]. In order to reduce both the design cost and time, coupling effects should also be estimated at the system level [105]. The coupling noise voltage on a quiet interconnect line has been analyzed by Shoji in [23] using a simple linear *RC* circuit. Delay uncertainty and noise expressions of coupled resistive interconnect have been presented by Kahng using π and L lumped circuit models in [106] and [107]. The effects of the coupling capacitance have also been addressed by Sakurai in [78] based on a coupled *RC* transmission line model. Estimates of the peak coupling noise voltage based on a coupled *RLC* transmission line model have been presented by the authors in [103]. A two-line coupled system is presented in the literature [23, 78, 98, 103, 106] to analyze this coupling

effect. A three-line coupled system is presented in [108] using an RC transmission line model. The CMOS logic gates are approximated by the effective output resistance; the nonlinear behavior of the MOS transistors is therefore neglected in these analyses [23, 78, 103, 106, 108]. Similar interconnect structures (or line impedances) are also assumed in [78, 103, 108] where the impedance differences among the on-chip interconnections are neglected. The maximum effective load capacitance, *i.e.*, the intrinsic load capacitance plus two times the coupling capacitance ($C + 2C_c$), is typically used to estimate the worst case propagation delay of an active CMOS logic gate [23, 78, 108].

In this chapter, a transient analysis of a CMOS logic gate driving a coupled resistive-capacitive interconnect based on the signal activity is presented. The interconnect-to-ground capacitance (or the self-capacitance) and the gate capacitance of the following logic stage are included in the intrinsic load capacitance (C_1, C_2, or C_3 for a three-line coupled structure). An analysis of an in-phase transition in which two (or three) coupled logic gates transition in the same direction demonstrates that the effective load capacitance of a CMOS logic gate depends upon the intrinsic load capacitance, the coupling capacitance, the signal activity, and the transistor size of the CMOS logic gates within the coupled system. Therefore, the effective load capacitance may deviate from the intrinsic load capacitances if the CMOS logic gates and intrinsic load capacitances are different within a coupled system. The same conclusion can also be observed for an out-of-phase transition, where the transition changes in the opposite direction for a two-line coupled system, making the effective load capacitances deviate from $C_1 + 2C_c$ or $C_2 + 2C_c$, which is typically assumed in a system level analysis [23, 78, 108].

Analytical expressions characterizing the output voltages for each CMOS logic gate are presented for both a two-line and a three-line coupled system. Delay estimates based on the analytical expressions are within 10% as compared to SPICE [49], while the error of the estimates neglecting the nonlinear behavior of a CMOS logic gate for an in-phase, an out-of-phase, and one active/one quiet transition can reach 50%, 18%, and 16% of SPICE, respectively, for a two-line coupled system. The peak noise voltage based on the analytical prediction is within 7% and 13% of SPICE for a two-line and a three-line coupled system, respectively.

The dependence of the interconnect coupling capacitance on the signal activity is discussed for both a two-line and a three-line coupled system in Section 7.2. Analytical expressions characterizing the effective load capacitance, the output voltage, and the propagation delay during an in-phase and an out-of-phase transition are presented in Sections 7.3 and 7.4, respectively, for a two-line and a three-line coupled system. In Section 7.5, an analytical expression characterizing the coupling noise voltage at the output of a quiet logic gate is presented for a two-line coupled system. This analytical model is also applied to a three-line coupled system to predict the peak coupling noise voltage. Strategies to manage the effects of interconnect coupling capacitance are discussed in Section 7.6, followed by some concluding remarks in Section 7.7.

7.2 Signal Activity of Coupled Interconnect

A physical structure of two coplanar interconnect lines is shown in Figure 7.1. A self-interconnect capacitance includes a parallel plate capacitance and a sidewall-to-ground capacitance [15, 61, 97]. The sidewall-to-sidewall electric field between

these two lines results in a fringing (or coupling) capacitance as shown in Figure 7.1 [57, 58, 60, 62, 96].

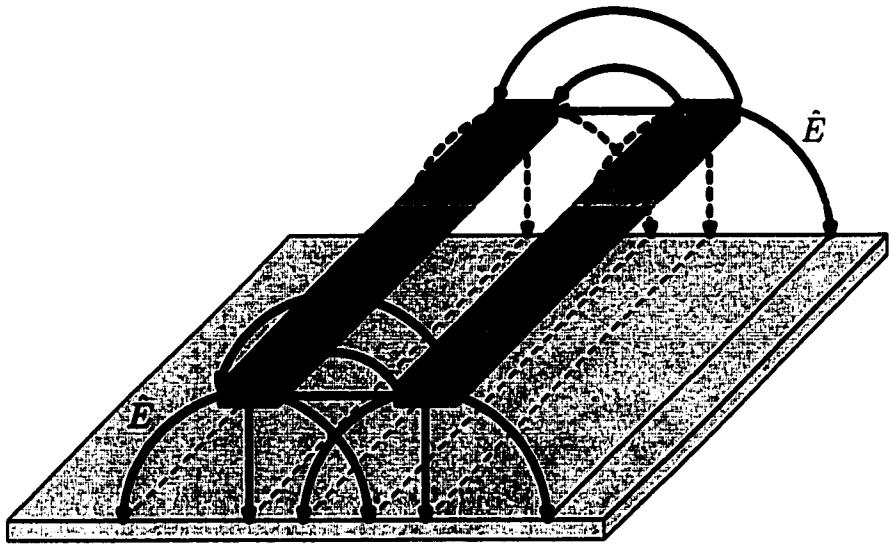


Figure 7.1: Physical structure of two capacitively coupled interconnect lines.

In a CMOS integrated circuit, interconnect lines are typically driven by CMOS logic gates. Therefore, the CMOS logic gates driving adjacent interconnect lines are capacitively coupled. A circuit diagram of N capacitively coupled interconnect lines driven by N CMOS inverters is shown in Figure 7.2. This coupled system can be analyzed by applying a two-line coupled structure to line 1 and 2 as well as line $N-1$ and N, and modeling the remaining adjacent lines using a three-line coupled structure.

In order to simplify this analysis as well as emphasize the nonlinear behavior of a CMOS inverter during a logic transition, the interconnect is modeled as a lumped resistive-capacitive load where R_1 (R_2, R_3) is the parasitic resistance of line 1 (2, 3) and C_1 (C_2, C_3) includes both the self-interconnect capacitance of line 1 (2, 3) and the gate capacitance of the following logic stage. C_c is the coupling

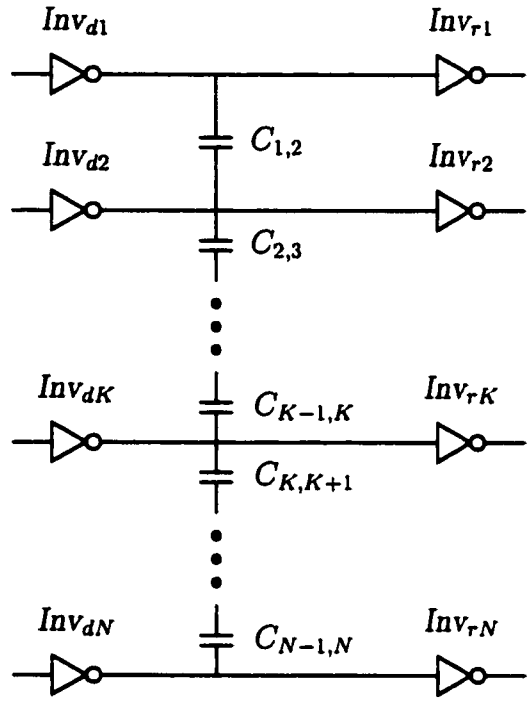


Figure 7.2: A circuit structure of N coupled interconnect lines driven by CMOS inverters.

(or fringing) capacitance in a two-line structure while C_{12} and C_{23} are the coupling (or fringing) capacitances between two neighboring interconnect lines 1 and 2, and 2 and 3, respectively, in a three-line system. The output voltages (V_1, V_2, and V_3) and current (I_1, I_2, and I_3) are shown in Figures 7.3 and 7.4 for a two-line and a three-line coupled structure, respectively. Differential equations characterizing the behavior of a coupled system are listed in Table 7.1 for both a two-line and a three-line coupled structure [108].

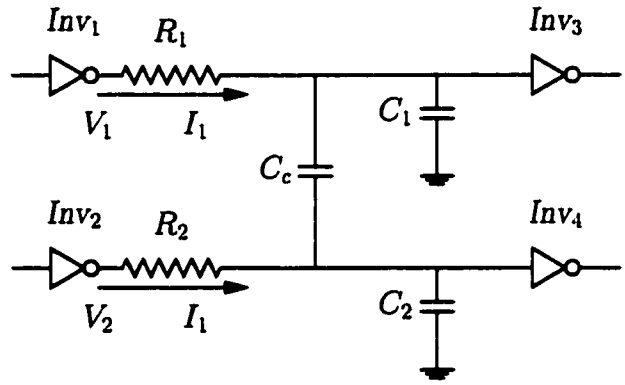


Figure 7.3: A circuit diagram of two coupled resistive-capacitive interconnections driven by CMOS inverters.

The transient response of a single CMOS inverter within a coupled system strongly depends upon the signal activity of each inverter. There are three possible conditions for each inverter, a high-to-low transition, a low-to-high transition, and a quiet state in which the output voltage of the inverter remains at either the voltage supply level (V_{dd}) or ground. A high-to-low or low-to-high transition is described as a dynamic transition. If the signal at the input of each inverter is purely random and uncorrelated, there are a total of nine (9) (as listed in Table 7.2) and twenty seven (27) (as listed in Table 7.3) possible signal combinations which can occur for a two-line and a three-line coupled system, respectively.

Table 7.1: Differential equations characterizing a system of coupled resistive-capacitive interconnections

Two coupled resistive-capacitive interconnections

$$(C_1 + C_c)\frac{dV_1}{dt} - C_c\frac{dV_2}{dt} = I_1 + R_1(C_1 + C_c)\frac{dI_1}{dt} - R_2C_c\frac{dI_2}{dt} \quad (7.1)$$

$$(C_2 + C_c)\frac{dV_2}{dt} - C_c\frac{dV_1}{dt} = I_2 + R_2(C_2 + C_c)\frac{dI_2}{dt} - R_1C_c\frac{dI_1}{dt} \quad (7.2)$$

Three coupled resistive-capacitive interconnections

$$(C_1 + C_{12})\frac{dV_1}{dt} - C_{12}\frac{dV_2}{dt} = I_1 + R_1(C_1 + C_{12})\frac{dI_1}{dt} - R_2C_{12}\frac{dI_2}{dt} \quad (7.3)$$

$$(C_2 + C_{12} + C_{23})\frac{dV_2}{dt} - C_{12}\frac{dV_1}{dt} - C_{23}\frac{dV_3}{dt} = I_2 + R_2(C_2 + C_{12} + C_{23})\frac{dI_2}{dt} - R_1C_{12}\frac{dI_1}{dt} - R_3C_{23}\frac{dI_3}{dt} \quad (7.4)$$

$$(C_3 + C_{23})\frac{dV_3}{dt} - C_{23}\frac{dV_2}{dt} = I_3 + R_3(C_3 + C_{23})\frac{dI_3}{dt} - R_2C_{23}\frac{dI_2}{dt} \quad (7.5)$$

Table 7.2: Possible signal activities for a two-line coupled system

V_{in1}	Inv_1	V_{in2}	Inv_2	
0 to V_{dd}	High-to-low	0 to V_{dd}	High-to-low	In-Phase
		V_{dd} to 0	Low-to-high	Out-of-Phase
		V_{dd} or 0	Quiet	One Active/One Quiet
V_{dd} to 0	Low-to-high	0 to V_{dd}	High-to-low	Out-of-Phase
		V_{dd} to 0	Low-to-high	In-Phase
		0 or V_{dd}	Quiet	One Active/One Quiet
V_{dd} or 0	Quiet	0 to V_{dd}	High-to-low	One Active/One Quiet
		V_{dd} to 0	Low-to-high	One Active/One Quiet
		0 or V_{dd}	Quiet	No Transition

Table 7.3: Possible signal activities for a three-line coupled system

V_{in1}	Inv_1	V_{in2}	Inv_2	V_{in3}	Inv_3
0 to V_{dd}	High-to-low	0 to V_{dd}	High-to-low	0 to V_{dd}	High-to-low
				V_{dd} to 0	Low-to-high
				V_{dd} or 0	Quiet
		V_{dd} to 0	Low-to-high	0 to V_{dd}	High-to-low
				V_{dd} to 0	Low-to-high
				V_{dd} or 0	Quiet
		0 or V_{dd}	Quiet	0 to V_{dd}	High-to-low
				V_{dd} to 0	Low-to-high
				V_{dd} or 0	Quiet
V_{dd} to 0	Low-to-high	0 to V_{dd}	High-to-low	0 to V_{dd}	High-to-low
				V_{dd} to 0	Low-to-high
				V_{dd} or 0	Quiet
		V_{dd} to 0	Low-to-high	0 to V_{dd}	High-to-low
				V_{dd} to 0	Low-to-high
				V_{dd} or 0	Quiet
		0 or V_{dd}	Quiet	0 to V_{dd}	High-to-low
				V_{dd} to 0	Low-to-high
				V_{dd} or 0	Quiet
V_{dd} or 0	Quiet	0 to V_{dd}	High-to-low	0 to V_{dd}	High-to-low
				V_{dd} to 0	Low-to-high
				V_{dd} or 0	Quiet
		V_{dd} to 0	Low-to-high	0 to V_{dd}	High-to-low
				V_{dd} to 0	Low-to-high
				V_{dd} or 0	Quiet
		0 or V_{dd}	Quiet	0 to V_{dd}	High-to-low
				V_{dd} to 0	Low-to-high
				V_{dd} or 0	Quiet

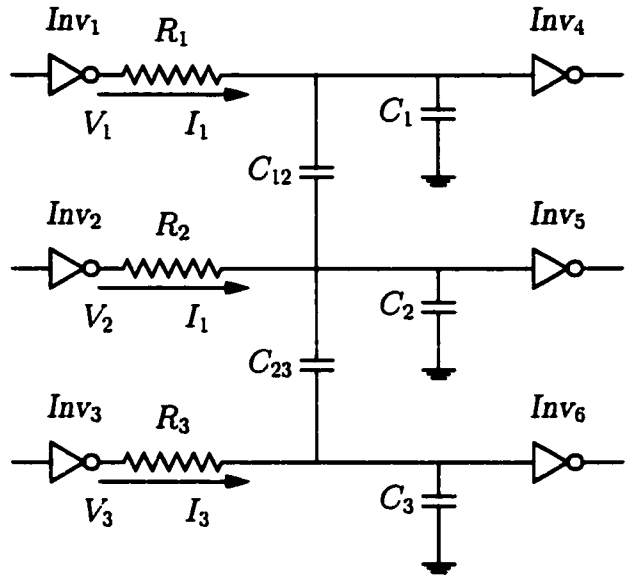


Figure 7.4: A circuit diagram of three coupled resistive-capacitive interconnections driven by CMOS inverters.

In the following analysis, if the CMOS inverters within a coupled system are dynamically transitioning, it is assumed that these inverters are triggered at the same time and at the same input slew rate. During a dynamic transition, only the active transistor in each inverter is considered in the development of the analytical expressions describing the waveform of the output voltage. The MOS transistors are characterized by the *nth* power law I-V model in the saturation region and the effective output conductance γ in the linear region [41, 52, 109].

7.3 In-Phase Transition

An in-phase transition, in which all inverters have the same dynamic transitions, is an optimistic condition in terms of the effect of the interconnect coupling capacitance on the propagation delay of a CMOS inverter [99, 108]. The proba-

bility of an in-phase transition is 2/9 for a two-line coupled system (as listed in Table 7.2) and 2/27 (see Table 7.3) for a three-line coupled system, respectively. In this section, analytical expressions characterizing the output voltage, the effective capacitive load, and the propagation delay of each CMOS inverter within a two-line and a three-line coupled system are presented. The analytic propagation delay is also compared in this section to SPICE [49].

7.3.1 The Output Voltage of Each CMOS Inverter

For a two-line coupled system, the outputs of both inverters are assumed to transition from high-to-low. The PMOS transistors are neglected based on an assumption of a fast ramp input signal [69]. $NMOS_1$ and $NMOS_2$ are the active transistors in each inverter and may have different geometric sizes. The shape of the input signals driving each inverter is characterized by a ramp signal,

$$V_{in} = \frac{t}{\tau_r} V_{dd} \quad \text{for} \quad 0 \leq t \leq \tau_r. \tag{7.6}$$

An assumption of a fast ramp input signal supports the condition that each inverter operates in the saturation region before the input transition is completed. Analytical expressions characterizing the output voltages, V_1 and V_2, are listed in Tables 7.4 and 7.5. τ_n is the time when the NMOS transistor turns ON where $\tau_n = \frac{V_{TN}}{V_{dd}}\tau_r$. τ^1_{nsat} and τ^2_{nsat} are the duration times when $NMOS_1$ and $NMOS_2$ operate in the saturation region, respectively. These times can be determined from (7.11) and (7.12). It is assumed in this analysis that $NMOS_1$ leaves the saturation region first, *i.e.*, $\tau^1_{nsat} < \tau^2_{nsat}$. After τ^{max}_{sat} [defined in (7.13)], both of the NMOS transistors operate in the linear region. K_1 and K_2 [defined in (7.20) and (7.21)] are integration constants which can be determined from $V_1(\tau^{max}_{sat})$ and $V_2(\tau^{max}_{sat})$ which are initial value of V_1 and V_2 at τ^{max}_{sat}, respectively .

Table 7.4: Analytical expressions characterizing the output voltage of a CMOS inverter driving an RC load within a two-line coupled system for an in-phase transition

Region	Output voltage $V_1(t)$ and $V_2(t)$
$[\tau_n, \tau_r]$	$V_1 = V_{dd} - \beta_{21}\frac{\tau_r}{(n_n+1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1}$ $-R_1B_{n1}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}$ (7.7)
	$V_2 = V_{dd} - \beta_{22}\frac{\tau_r}{(n_n+1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1}$ $-R_2B_{n2}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}$ (7.8)
	$\beta_{21} = \frac{(C_2+C_c)B_{n1} + C_cB_{n2}}{C_1C_2 + C_c(C_1+C_2)}$ (7.9)
	$\beta_{22} = \frac{(C_1+C_c)B_{n2} + C_cB_{n1}}{C_1C_2 + C_c(C_1+C_2)}$ (7.10)
$[\tau_r, \tau_{sat}^{min}]$	$V_1 = V_1(\tau_r) - \beta_{21}(V_{dd} - V_{TN})^{n_n}(t-\tau_r)$ (7.11)
	$V_2 = V_2(\tau_r) - \beta_{22}(V_{dd} - V_{TN})^{n_n}(t-\tau_r)$ (7.12)
	$\tau_{sat}^{min} = \min(\tau_{nsat}^1, \tau_{nsat}^2)$ (7.13)
	$\tau_{sat}^{max} = \max(\tau_{nsat}^1, \tau_{nsat}^2)$ (7.14)
$[\tau_{sat}^{min}, \tau_{sat}^{max}]$	$V_1 = -V_{1a} + (V_{nsat} + V_{1a})e^{-\alpha_{n1}(t-\tau_{nsat}^1)}$ (7.15)
	$V_2 = V_2(\tau_{nsat}^1) - \frac{B_{n2}}{C_2+C_c}(V_{dd} - V_{TN})^{n_n}(t-\tau_{nsat}^1) - V_{2a}$ (7.16)
	$V_{1a} = \frac{C_c}{(C_2+C_c)\gamma_{n1}}B_{n2}(V_{dd} - V_{TN})^{n_n}$ (7.17)
	$\alpha_{n1} = -\frac{\gamma_{n1}(C_2+C_c)}{(1+R_1\gamma_{n1})(C_1C_2 + C_c(C_1+C_2))}$ (7.18)
	$V_{2a} = \frac{C_c}{C_2+C_c}(1+R_1\gamma_{n1})(V_{nsat}+V_{1a})(1-e^{-\alpha_{n1}(t-\tau_{nsat}^1)})$ (7.19)

Table 7.5: Analytical expressions characterizing the output voltage of a CMOS inverter driving an RC load within a two-line coupled system for an in-phase transition (continued)

Region	Output voltage $V_1(t)$ and $V_2(t)$
$t \geq \tau_{sat}^{max}$	$V_1 = \frac{K_1}{2}[e^{-\nu_1 t} + e^{-\nu_2 t} + \frac{\chi_c}{\chi_a}(e^{-\nu_1 t} - e^{-\nu_2 t})]$ $+\frac{\chi_d}{\chi_a}K_2(e^{-\nu_1 t} - e^{-\nu_2 t})$ (7.20)
	$V_2 = \frac{K_2}{2}[e^{-\nu_1 t} + e^{-\nu_2 t} - \frac{\chi_c}{\chi_a}(e^{-\nu_1 t} - e^{-\nu_2 t})]$ $+\frac{\chi_e}{\chi_a}K_1(e^{-\nu_1 t} - e^{-\nu_2 t})$ (7.21)
	$\nu_1 = \frac{1 + R_1\gamma_{n1}}{1 + R_2\gamma_{n2}} \frac{\chi_b + \chi_a}{C_1C_2 + C_c(C_1 + C_2)}$ (7.22)
	$\nu_2 = \frac{1 + R_1\gamma_{n1}}{1 + R_2\gamma_{n2}} \frac{\chi_b - \chi_a}{C_1C_2 + C_c(C_1 + C_2)}$ (7.23)
	$\chi_a = \sqrt{\chi_c^2 + 4\gamma_{n1}\gamma_{n2}C_c^2(1 + R1\gamma_{n1})(1 + R_2\gamma_{n2})}$ (7.24)
	$\chi_b = \gamma_{n1}(1 + R_2\gamma_{n2})(C_2 + C_c) + \gamma_{n2}(1 + R1\gamma_{n1})(C_1 + C_c)$ (7.25)
	$\chi_c = \gamma_{n1}(1 + R_2\gamma_{n2})(C_2 + C_c) - \gamma_{n2}(1 + R1\gamma_{n1})(C_1 + C_c)$ (7.26)
	$\chi_d = \gamma_{n2}(1 + R_2\gamma_{n2})C_c$ (7.27)
	$\chi_e = \gamma_{n1}(1 + R_1\gamma_{n1})C_c$ (7.28)

For a three-line coupled system, $NMOS_1$, $NMOS_2$, and $NMOS_3$ are the active transistors in each CMOS inverter. Following the same procedure as for the two-line coupled system, analytical expressions characterizing the output voltage of each CMOS inverter are listed in Table 7.6 before one of these three active NMOS transistors starts to operate in the linear region. The analytical solutions of the output voltages, V_1, V_2, and V_3, after τ_{sat}^{min} [defined in (7.14)] are presented in Appendix B.

7.3.2 Effective Capacitive Load of Each CMOS Inverter

For a two-line coupled system, the effective capacitive load of each inverter in an in-phase transition is

$$C_{1_{eff}} = \frac{C_1C_2 + C_c(C_1 + C_2)}{C_2 + (1 + \frac{B_{n2}}{B_{n1}})C_c}, \tag{7.42}$$

$$C_{2_{eff}} = \frac{C_1C_2 + C_c(C_1 + C_2)}{C_1 + (1 + \frac{B_{n1}}{B_{n2}})C_c}, \tag{7.43}$$

respectively. Assuming B_{n1} is equal to B_{n2}, *i.e.*, both NMOS transistors have the same geometric sizes (or output gain), the effective load capacitance of each inverter is shown in Figure 7.5. The solid lines shown in Figure 7.5 depict the ratio of $C_{1_{eff}}$ to C_1 and the dotted lines represent the ratio of $C_{2_{eff}}$ to C_2. The horizontal axis represents the ratio of C_2 to C_1, which characterizes the difference between the intrinsic load capacitances. Ratios of the coupling capacitance to the line capacitance, C_c to C_1, of 0.3, 0.5, and 0.7 are considered. Note that the deviation of the effective load capacitances from the intrinsic capacitances (C_1 and C_2) increases if the difference between the intrinsic load capacitances increases. The deviation also increases with increasing coupling capacitance for the same ratio of C_2/C_1.

Table 7.6: Analytical expressions characterizing the output voltage of a CMOS inverter driving an RC load for an in-phase transition within a three-line coupled system

Region	Output voltage $V_1(t)$, $V_2(t)$, and $V_3(t)$
$[\tau_n, \tau_r]$	$V_1 = V_{dd} - \beta_{31}\frac{\tau_r}{(n_n+1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1}$ $-R_1 B_{n1}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}$ (7.29)
	$V_2 = V_{dd} - \beta_{32}\frac{\tau_r}{(n_n+1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1}$ $-R_2 B_{n2}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}$ (7.30)
	$V_3 = V_{dd} - \beta_{33}\frac{\tau_r}{(n_n+1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1}$ $-R_2 B_{n3}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}$ (7.31)
	$\beta_{31} = \frac{C_{2t} - \frac{C_{23}^2}{C_{3t}}}{C_{1t}(C_{2t} - \frac{C_{23}^2}{C_{3t}}) - C_{12}^2}[B_{n1} + \frac{C_{12}}{C_{2t} - \frac{C_{23}^2}{C_{3t}}}B_{n2}$ $+\frac{C_{23}}{C_{3t}}\frac{C_{12}}{C_{2t} - \frac{C_{23}^2}{C_{3t}}}B_{n3}]$ (7.32)
	$\beta_{32} = \frac{1}{C_{2t} - \frac{C_{12}^2}{C_{1t}} - \frac{C_{23}^2}{C_{3t}}}(\frac{C_{12}}{C_{1t}}B_{n1} + B_{n2} + \frac{C_{23}}{C_{3t}}B_{n3})$ (7.33)
	$\beta_{33} = \frac{C_{2t} - \frac{C_{12}^2}{C_{1t}}}{C_{1t}(C_{2t} - \frac{C_{12}^2}{C_{1t}}) - C_{23}^2}[B_{n3} + \frac{C_{23}}{C_{2t} - \frac{C_{12}^2}{C_{1t}}}B_{n2}$ $+\frac{C_{12}}{C_{1t}}\frac{C_{23}}{C_{2t} - \frac{C_{12}^2}{C_{1t}}}B_{n1}]$ (7.34)
	$C_{1t} = C_1 + C_{12}$ (7.35)
	$C_{2t} = C_2 + C_{12} + C_{23}$ (7.36)
	$C_{3t} = C_3 + C_{23}$ (7.37)
$[\tau_r, \tau_{sat}^{min}]$	$V_1 = V_1(\tau_r) - \beta_{31}(V_{dd} - V_{TN})^{n_n}(t - \tau_r)$ (7.38)
	$V_2 = V_2(\tau_r) - \beta_{32}(V_{dd} - V_{TN})^{n_n}(t - \tau_r)$ (7.39)
	$V_3 = V_3(\tau_r) - \beta_{33}(V_{dd} - V_{TN})^{n_n}(t - \tau_r)$ (7.40)
	$\tau_{sat}^{min} = \min(\tau_{nsat}^1, \tau_{nsat}^2, \tau_{nsat}^3)$ (7.41)

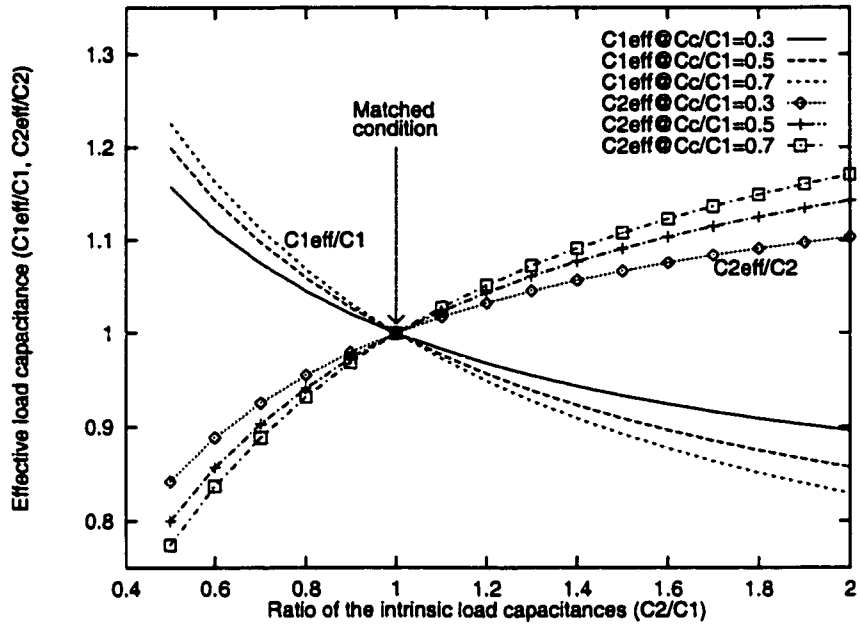


Figure 7.5: The ratio of the effective load capacitances $C_{1_{eff}}$ and $C_{2_{eff}}$ to C_1 and C_2, respectively, for an in-phase transition assuming $B_{n1} = B_{n2}$.

Note in Fig. 7.5 that the effective load capacitance of one inverter increases above the corresponding intrinsic load capacitance while the effective load capacitance of the second inverter drops below the corresponding intrinsic load capacitance. The deviation of the effective load capacitances from the intrinsic load capacitances results in different propagation delays.

For a three-line coupled system, the effective captive load of each CMOS inverter is

$$C_{1_{eff}} = \frac{C_{1t} - \frac{C_{12}^2}{C_{2t} - \frac{C_{23}^2}{C_{3t}}}}{1 + \frac{C_{12}}{C_{2t} - \frac{C_{23}^2}{C_{3t}}} \frac{B_{n2}}{B_{n1}} + \frac{C_{23}}{C_{3t}} \frac{C_{12}}{C_{2t} - \frac{C_{23}^2}{C_{3t}}} \frac{B_{n3}}{B_{n1}}}, \tag{7.44}$$

$$C_{2_{eff}} = \frac{C_{2t} - \frac{C_{12}}{C_{1t}} C_{12} - \frac{C_{23}}{C_{3t}} C_{23}}{\frac{C_{12}}{C_{1t}} \frac{B_{n1}}{B_{n2}} + 1 + \frac{C_{23}}{C_{3t}} \frac{B_{n3}}{B_{n2}}}, \tag{7.45}$$

$$C_{3_{eff}} = \frac{C_{3t} - \frac{C_{23}^2}{C_{2t} - \frac{C_{12}^2}{C_{1t}}}}{\frac{C_{12}}{C_{1t}} \frac{C_{23}}{C_{2t} - \frac{C_{12}^2}{C_{1t}}} \frac{B_{n1}}{B_{n3}} + \frac{C_{23}}{C_{2t} - \frac{C_{12}^2}{C_{1t}}} \frac{B_{n2}}{B_{n3}} + 1}, \tag{7.46}$$

respectively. Note that the effective capacitive load of each CMOS inverter depends not only upon the intrinsic load capacitance and the coupling capacitance but also the transconductance of each active transistor (the geometric size and device characteristics of each active transistor).

7.3.3 Propagation Delay Time

The propagation delay $t_{0.5}$ of a CMOS inverter is defined here as the time from 50% V_{dd} of the input to 50% V_{dd} of the output. For a high-to-low transition at the output, if V_{nsat} is greater than $0.5V_{dd}$, the time when the output voltage reaches $0.5V_{dd}$ can be determined from an analytic expression characterizing the transistor operating within the saturation region. If V_{nsat} is less than $0.5V_{dd}$, the time when the output voltage reaches $0.5V_{dd}$ occurs primarily when the transistor operates within the linear region. Note that the analytical expressions, (7.20) and (7.21), listed in Table 7.4 characterizing the output voltages in the linear region are intractable and do not permit a close form analytical expression characterizing the propagation delay of a CMOS inverter to be developed. In the following analysis, analytical expressions characterizing the transistor operating in the saturation

region are extrapolated to approximate the time for the output signal to reach $0.5V_{dd}$ [41, 52].

Therefore, based on this assumption, analytical expressions characterizing the propagation delay of each CMOS inverter within a two-line and a three-line coupled system are listed in Table 7.7. The effect of the interconnect coupling capac-

Table 7.7: Propagation delay of a CMOS inverter for an in-phase transition

Two coupled resistive-capacitive lines	
$t_{P_{HL1}} = \frac{0.5V_{dd} - R_1 B_{n1}(V_{dd} - V_{TN})^{n_n}}{\beta_{21}(V_{dd} - V_{TN})^{n_n}} - \frac{\tau_r(V_{dd} - V_{TN})}{(n_n + 1)V_{dd}} + \tau_r$	(7.47)
$t_{P_{HL2}} = \frac{0.5V_{dd} - R_2 B_{n2}(V_{dd} - V_{TN})^{n_n}}{\beta_{22}(V_{dd} - V_{TN})^{n_n}} - \frac{\tau_r(V_{dd} - V_{TN})}{(n_n + 1)V_{dd}} + \tau_r$	(7.48)
Three coupled resistive-capacitive lines	
$t_{P_{HL1}} = \frac{0.5V_{dd} - R_1 B_{n1}(V_{dd} - V_{TN})^{n_n}}{\beta_{31}(V_{dd} - V_{TN})^{n_n}} - \frac{\tau_r(V_{dd} - V_{TN})}{(n_n + 1)V_{dd}} + \tau_r$	(7.49)
$t_{P_{HL2}} = \frac{0.5V_{dd} - R_2 B_{n2}(V_{dd} - V_{TN})^{n_n}}{\beta_{32}(V_{dd} - V_{TN})^{n_n}} - \frac{\tau_r(V_{dd} - V_{TN})}{(n_n + 1)V_{dd}} + \tau_r$	(7.50)
$t_{P_{HL3}} = \frac{0.5V_{dd} - R_3 B_{n3}(V_{dd} - V_{TN})^{n_n}}{\beta_{33}(V_{dd} - V_{TN})^{n_n}} - \frac{\tau_r(V_{dd} - V_{TN})}{(n_n + 1)V_{dd}} + \tau_r$	(7.51)

itance on the propagation delay is characterized by β_{21} and β_{22} [defined by (7.9) and (7.10), respectively] for a two-line coupled system and β_{31}, β_{32}, and β_{33} [defined by (7.32), (7.32), and (7.32), respectively] for a three-line coupled system. Note that the propagation delay also depends upon the intrinsic capacitive loads, the coupling capacitances, and the size of each active transistor, which is the same observation as for the effective capacitive load of each CMOS inverter.

A comparison of the propagation delay based on these analytical expressions with SPICE is listed in Tables 7.8 and 7.9. *No coupling* is defined as the condition under which the propagation delay is estimated based solely on the intrinsic load

Table 7.8: Comparison of an in-phase transition with SPICE for a two-line coupled system

	Circuit parameters							SPICE		No coupling				Analytic estimation			
τ_r (ns)	w_{n1} (μm)	R_1 (Ω)	C_1 (pF)	w_{n2} (μm)	R_2 (Ω)	C_2 (pF)	C_c (pF)	τ_1 (ps)	τ_2 (ps)	τ_1 (ps)	τ_2 (ps)	δ_1 (%)	δ_2 (%)	τ_1 (ps)	τ_2 (ps)	δ_1 (%)	δ_2 (%)
0.2	1.8	100	0.2	1.8	100	0.2	0.1	312	312	297	297	4.8	4.8	297	297	4.8	4.8
0.2	1.8	100	0.1	1.8	100	0.2	0.1	210	270	160	296	23.8	9.6	195	252	7.2	6.7
0.2	1.8	100	0.2	1.8	100	0.1	0.1	270	210	296	160	9.6	23.8	252	195	6.7	7.2
0.2	1.8	300	0.1	3.6	100	0.3	0.1	177	219	82	202	53.7	7.8	165	213	6.8	2.7
0.2	3.6	100	0.3	1.8	300	0.1	0.1	219	177	202	82	7.8	53.7	213	165	2.7	6.8
0.2	1.8	100	0.2	3.6	100	0.4	0.1	310	294	160	276	48.4	6.1	298	281	3.8	4.4
0.2	3.6	100	0.4	1.8	100	0.2	0.1	294	310	276	160	6.1	48.4	281	298	4.4	3.8
0.3	1.8	200	0.2	3.6	200	0.4	0.2	310	270	163	249	47.4	7.8	290	258	6.5	4.4
0.3	3.6	200	0.4	1.8	200	0.2	0.2	270	310	249	163	7.8	47.4	258	290	4.4	6.5
0.3	1.8	100	0.2	3.6	100	0.3	0.2	300	251	173	226	42.3	10.0	282	243	6.0	3.2
0.3	3.6	100	0.3	1.8	100	0.2	0.2	251	300	226	173	10.0	42.3	243	282	3.2	6.0
0.5	1.8	100	0.2	3.6	100	0.4	0.1	355	337	198	314	44.2	6.8	335	318	5.6	5.6
0.5	3.6	100	0.4	1.8	100	0.2	0.1	337	355	314	198	6.8	44.2	318	335	5.6	5.6

Statistic analysis	No coupling	Analytic estimation
Maximum error (%)	53.7	7.2
Average error (%)	24.6	5.2

Table 7.9: Comparison of an in-phase transition with SPICE for a three-line coupled system

	Circuit parameters											SPICE	No coupling		Analytic	
τ_r (ns)	w_{n1} (μm)	R_1 (Ω)	C_1 (pF)	w_{n2} (μm)	R_2 (Ω)	C_2 (pF)	w_{n3} (μm)	R_3 (Ω)	C_3 (pF)	C_{12} (pF)	C_{23} (pF)	τ_2 (ps)	τ_2 (ps)	δ_2 (%)	τ_2 (ps)	δ_2 (%)
0.2	1.8	80	0.1	3.6	100	0.15	1.8	90	0.08	0.05	0.05	139	124	10.8	131	6.1
0.2	1.8	80	0.1	3.6	100	0.15	1.8	90	0.1	0.1	0.1	145	124	14.5	137	5.5
0.2	3.6	100	0.1	3.6	100	0.2	3.6	100	0.1	0.1	0.1	136	158	16.2	126	7.4
0.2	3.6	100	0.1	3.6	100	0.3	3.6	100	0.1	0.1	0.1	170	224	31.8	158	7.1
0.2	3.6	100	0.1	3.6	100	0.2	3.6	100	0.2	0.1	0.1	150	158	5.3	143	4.7
0.2	3.6	100	0.1	3.6	200	0.4	3.6	100	0.1	0.1	0.1	180	248	37.8	165	8.3
0.2	3.6	100	0.1	3.6	200	0.4	3.6	100	0.1	0.2	0.2	166	248	49.4	153	7.8
0.2	3.6	100	0.1	3.6	200	0.5	3.6	100	0.1	0.2	0.2	189	289	52.9	176	6.9
Statistic analysis					No coupling							Analytic estimation				
Maximum error (%)					52.9							8.3				
Average error (%)					27.3							6.7				

capacitance [23, 78, 108]. The maximum error under the *no coupling* condition can exceed 50% as compared to SPICE for a two-line and a three-line coupled system while the maximum error of the analytic propagation delay model listed in Table 7.7 is within 9% of SPICE.

7.4 Out-of-Phase Transition

An out-of-phase transition is a pessimistic condition in terms of the effect of the interconnect coupling capacitance on the propagation delay of a CMOS inverter [99, 108]. Analytical expressions characterizing the output voltage, the effective capacitive load, and the propagation delay of each CMOS inverter within a two-line and a three-line coupled system are developed in this section for an out-of-phase transition. A comparison of the analytic estimations with SPICE is also presented in this section.

7.4.1 The Output Voltage of Each CMOS Inverter

For a two-line coupled system, an out-of-phase transition has the same probability as an in-phase transition. It is assumed in this section that the output of Inv_1 transitions from high-to-low while the output of Inv_2 transitions from low-to-high. $NMOS_1$ and $PMOS_2$ are the active transistors in each inverter. The input signals are

$$V_{in1} = \frac{t}{\tau_r} V_{dd} \quad \text{for} \quad 0 \leq t \leq \tau_r, \tag{7.52}$$

$$V_{in2} = (1 - \frac{t}{\tau_r}) V_{dd} \quad \text{for} \quad 0 \leq t \leq \tau_r. \tag{7.53}$$

The initial states of V_1 and V_2 are V_{dd} and ground, respectively. It is assumed in this analysis that the absolute value of the threshold voltages of the NMOS and

PMOS transistors are approximately equal. In the following analysis, parameters describing the voltages of the PMOS transistor are absolute values. Analytical expressions characterizing the output voltage for a two-line coupled systems are listed in Table 7.10 assuming $PMOS_2$ starts operating in the linear region. When both active transistors operate in the linear region, a solution of the output voltages can be obtained by following the same procedure as for an in-phase transition, as elaborated in Appendix A.

For a three-line coupled system, as shown in Figure 7.4, an out-of-phase transition is defined where the middle line (driven by Inv_2) dynamically transitions opposite to that of the neighboring lines (driven by Inv_1 and Inv_3). The probability of this occurrence is 2/27 (see Table 7.3). For example, the output of Inv_2 transitions from high-to-low while the outputs of Inv_1 and Inv_3 transition from low-to-high. Assuming the input signal has the same waveform shape as a two-line coupled system, $PMOS_1$, $NMOS_2$, and $PMOS_3$ are the active transistors in each of the CMOS inverters. The initial value of V_1, V_2, and V_3 are ground, V_{dd}, and ground, respectively. Analytical expressions characterizing the output voltage of each CMOS inverter before one of these three active transistors starts operating in the linear region are listed in Tables 7.11 and 7.12.

For a three-line coupled system, there are several signal combinations where the effect of the interconnect coupling capacitance on the propagation delay of Inv_2 lies between an in-phase and an out-of-phase transition. These combinations have the probability of 4/27 (see Table 7.3). For example, the outputs of Inv_1 and Inv_2 transition from high-to-low while the output of Inv_3 transitions from low-to-high. Under this condition, $NMOS_1$, $NMOS_2$, and $PMOS_3$ are the active transistors in each CMOS inverter. The initial value of V_1, V_2, and V_3 are V_{dd},

Table 7.10: Analytical expressions characterizing the output voltage of a CMOS inverter driving an RC load within a two-line coupled system for an out-of-phase transition

Region	Output voltage $V_1(t)$ and $V_2(t)$
$[\tau_n(\tau_p), \tau_r]$	$V_1 = V_{dd} - \frac{(C_2+C_c)V_{n,1} - C_cV_{p,1}}{C_1C_2 + C_c(C_1+C_2)} - R_1B_{n1}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}$ (7.54)
	$V_2 = \frac{(C_1+C_c)V_{p,1} - C_cV_{n,1}}{C_1C_2 + C_c(C_1+C_2)} + R_2B_{p2}(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p}$ (7.55)
	$V_{n,1} = B_{n1}\frac{\tau_r}{(n_n+1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1}$ (7.56)
	$V_{p,1} = B_{p2}\frac{\tau_r}{(n_p+1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p+1}$ (7.57)
$[\tau_r, \tau_{sat}^{min}]$	$V_1 = V_1(\tau_r) - \frac{(C_2+C_c)V_{n,2} - C_cV_{p,2}}{C_1C_2 + C_c(C_1+C_2)}(t-\tau_r)$ (7.58)
	$V_2 = V_2(\tau_r) + \frac{(C_1+C_c)V_{p,2} - C_cV_{n,2}}{C_1C_2 + C_c(C_1+C_2)}(t-\tau_r)$ (7.59)
	$V_{n,2} = B_{n1}(V_{dd} - V_{TN})^{n_n}$ (7.60)
	$V_{p,2} = B_{p2}(V_{dd} - V_{TP})^{n_p}$ (7.61)
	$\tau_{sat}^{min} = \min(\tau_{nsat}^1, \tau_{psat}^2)$ (7.62)
	$\tau_{sat}^{max} = \max(\tau_{nsat}^1, \tau_{psat}^2)$ (7.63)
$[\tau_{sat}^{min}, \tau_{sat}^{max}]$	$V_1 = V_1(\tau_{sat}^{min}) + V_{n,3}(t-\tau_{sat}^{min}) + \frac{C_c(1+R_2\gamma_{p2})}{C_1+C_c}(V_{psat} - V_{p,3})$ $(1 - e^{-\alpha_{p2}(t-\tau_{sat}^{min})})$ (7.64)
	$V_2 = V_{dd} - V_{p,3} - (V_{psat} - V_{p,3})e^{-\alpha_{p2}(t-\tau_{sat}^{min})}$ (7.65)
	$V_{n,3} = \frac{1}{C_1+C_c}B_{n1}(V_{dd} - V_{TN})^{n_n}$ (7.66)
	$V_{p,3} = \frac{C_c}{(C_1+C_c)\gamma_{p2}}B_{n1}(V_{dd} - V_{TN})^{n_n}$ (7.67)
	$\alpha_{p2} = \frac{\gamma_{p2}(C_1+C_c)}{(1+R_2\gamma_{p2})(C_1C_2 + C_c(C_1+C_2))}$ (7.68)

Table 7.11: Analytical expressions characterizing the output voltage of a CMOS inverter driving an RC load within a three-line coupled system. Inv_2 transitions from high-to-low while Inv_1 and Inv_3 transition from low-to-high.

Region	Output voltage $V_1(t)$, $V_2(t)$, and $V_3(t)$
$[\tau_n, \tau_r]$	$V_1 = \frac{C_{2t} - \frac{C_{23}^2}{C_{3t}}}{C_{1t}(C_{2t} - \frac{C_{23}^2}{C_{3t}}) - C_{12}^2}(V_{p1,1} - \frac{C_{12}}{C_{2t} - \frac{C_{23}^2}{C_{3t}}}V_{n2,1} + \frac{C_{23}}{C_{3t}}\frac{C_{12}}{C_{2t} - \frac{C_{23}^2}{C_{3t}}}V_{p3,1})$ $+R_1 B_{p1}(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p}$ (7.69)
	$V_2 = V_{dd} - \frac{1}{C_{2t} - \frac{C_{12}^2}{C_{1t}} - \frac{C_{23}^2}{C_{3t}}}(V_{n2,1} - \frac{C_{12}}{C_{1t}}V_{p1,1} - \frac{C_{23}}{C_{3t}}V_{p3,1})$ $-R_2 B_{n2}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}$ (7.70)
	$V_3 = \frac{C_{2t} - \frac{C_{12}^2}{C_{1t}}}{C_{3t}(C_{2t} - \frac{C_{12}^2}{C_{1t}}) - C_{23}^2}(V_{p3,1} - \frac{C_{23}}{C_{2t} - \frac{C_{12}^2}{C_{1t}}}V_{n2,1} + \frac{C_{12}}{C_{1t}}\frac{C_{23}}{C_{2t} - \frac{C_{12}^2}{C_{1t}}}V_{p1,1})$ $+R_3 B_{p3}(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p}$ (7.71)
	$V_{p1,1} = \frac{\tau_r}{(n_p+1)V_{dd}}B_{p1}(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p+1}$ (7.72)
	$V_{n2,1} = \frac{\tau_r}{(n_n+1)V_{dd}}B_{n2}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1}$ (7.73)
	$V_{p3,1} = \frac{\tau_r}{(n_p+1)V_{dd}}B_{p3}(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p+1}$ (7.74)

Table 7.12: Analytical expressions characterizing the output voltage of a CMOS inverter driving an *RC* load within a three-line coupled system. Inv_2 transitions from high-to-low while Inv_1 and Inv_3 transition from low-to-high (continued).

Region	Output voltage $V_1(t)$, $V_2(t)$, and $V_3(t)$
$[\tau_r, \tau_{sat}^{min}]$	$V_1 = V_1(\tau_r) + \frac{C_{2t} - \frac{C_{23}^2}{C_{3t}}}{C_{1t}(C_{2t} - \frac{C_{23}^2}{C_{3t}}) - C_{12}^2}(V_{p1,2} - \frac{C_{12}}{C_{2t} - \frac{C_{23}^2}{C_{3t}}}V_{n2,2} + \frac{C_{23}}{C_{3t}}\frac{C_{12}}{C_{2t} - \frac{C_{23}^2}{C_{3t}}}V_{p3,2})(t - \tau_r)$ (7.75)
	$V_2 = V_2(\tau_r) - \frac{(t - \tau_r)}{C_{2t} - \frac{C_{12}^2}{C_{1t}} - \frac{C_{23}^2}{C_{3t}}}(V_{n2,2} - \frac{C_{12}}{C_{1t}}V_{p1,2} - \frac{C_{23}}{C_{3t}}V_{p3,2})$ (7.76)
	$V_3 = V_3(\tau_r) + \frac{C_{2t} - \frac{C_{12}^2}{C_{1t}}}{C_{3t}(C_{2t} - \frac{C_{12}^2}{C_{1t}}) - C_{23}^2}(V_{p3,2} - \frac{C_{23}}{C_{2t} - \frac{C_{12}^2}{C_{1t}}}V_{n2,2} + \frac{C_{12}}{C_{1t}}\frac{C_{23}}{C_{2t} - \frac{C_{12}^2}{C_{1t}}}V_{p1,2})(t - \tau_r)$ (7.77)
	$V_{p1,2} = B_{p1}(V_{dd} - V_{TP})^{n_p}$ (7.78)
	$V_{n2,2} = B_{n2}(V_{dd} - V_{TN})^{n_n}$ (7.79)
	$V_{p3,2} = B_{p3}(V_{dd} - V_{TP})^{n_p}$ (7.80)
	$\tau_{sat}^{min} = \min(\tau_{psat}^1, \tau_{nsat}^2, \tau_{psat}^3)$ (7.81)

V_{dd}, and ground, respectively. Analytical expressions characterizing the output voltage of each CMOS inverter before one of these three active transistors begins operating in the linear region are listed in Tables 7.13 and 7.14.

Table 7.13: Analytical expressions characterizing the output voltage of a CMOS inverter driving an *RC* load within a three-line coupled system. Inv_1 and Inv_2 transition from high-to-low while Inv_3 transitions from low-to-high.

Region	Output voltage $V_1(t)$, $V_2(t)$, and $V_3(t)$
$[\tau_n, \tau_r]$	$V_1 = V_{dd} - \frac{C_{2t} - \frac{C_{23}^2}{C_{3t}}}{C_{1t}(C_{2t} - \frac{C_{23}^2}{C_{3t}})}(V_{n1,1} + \frac{C_{12}}{C_{2t} - \frac{C_{23}^2}{C_{3t}}}V_{n2,1} - \frac{C_{23}}{C_{3t}}\frac{C_{12}}{C_{2t} - \frac{C_{23}^2}{C_{3t}}}V_{p3,1})$ $+R_1 B_{p1}(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p}$ (7.82)
	$V_2 = V_{dd} - \frac{1}{C_{2t} - \frac{C_{12}^2}{C_{1t}} - \frac{C_{23}^2}{C_{3t}}}(V_{n2,1} + \frac{C_{12}}{C_{1t}}V_{n1,1} - \frac{C_{23}}{C_{3t}}V_{p3,1})$ $-R_2 B_{n2}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}$ (7.83)
	$V_3 = \frac{C_{2t} - \frac{C_{12}^2}{C_{1t}}}{C_{3t}(C_{2t} - \frac{C_{12}^2}{C_{1t}})}(V_{p3,1} - \frac{C_{23}}{C_{2t} - \frac{C_{12}^2}{C_{1t}}}V_{n2,1} - \frac{C_{12}}{C_{1t}}\frac{C_{23}}{C_{2t} - \frac{C_{12}^2}{C_{1t}}}V_{n1,1})$ $+R_3 B_{p3}(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p}$ (7.84)
	$V_{n1,1} = \frac{\tau_r}{(n_n+1)V_{dd}}B_{n1}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1}$ (7.85)
	$V_{n2,1} = \frac{\tau_r}{(n_n+1)V_{dd}}B_{n2}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1}$ (7.86)
	$V_{p3,1} = \frac{\tau_r}{(n_p+1)V_{dd}}B_{p3}(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p+1}$ (7.87)

7.4.2 Effective Capacitive Load of Each CMOS Inverter

In order to simplify the analysis of the effective capacitive load of each CMOS inverter for an out-of-phase transition, it is assumed that both the NMOS and

Table 7.14: Analytical expressions characterizing the output voltage of a CMOS inverter driving an *RC* load within a three-line coupled system. Inv_1 and Inv_2 transition from high-to-low while Inv_3 transitions from low-to-high (continued).

Region	Output voltage $V_1(t)$, $V_2(t)$, and $V_3(t)$
$[\tau_r, \tau_{sat}^{min}]$	$V_1 = V_1(\tau_r) - \frac{C_{2t} - \frac{C_{23}^2}{C_{3t}}}{C_{1t}(C_{2t} - \frac{C_{23}^2}{C_{3t}})}(V_{n1,2} + \frac{C_{12}}{C_{2t} - \frac{C_{23}^2}{C_{3t}}}V_{n2,2}$ $-\frac{C_{23}}{C_{3t}}\frac{C_{12}}{C_{2t} - \frac{C_{23}^2}{C_{3t}}}V_{p3,2})(t - \tau_r)$ (7.88)
	$V_2 = V_2(\tau_r) - \frac{(t - \tau_r)}{C_{2t} - \frac{C_{12}^2}{C_{1t}} - \frac{C_{23}^2}{C_{3t}}}(V_{n2,2} + \frac{C_{12}}{C_{1t}}V_{n1,2} - \frac{C_{23}}{C_{3t}}V_{p3,2})$ (7.89)
	$V_3 = V_3(\tau_r) + \frac{C_{2t} - \frac{C_{12}^2}{C_{1t}}}{C_{3t}(C_{2t} - \frac{C_{12}^2}{C_{1t}})}(V_{p3,2} - \frac{C_{23}}{C_{2t} - \frac{C_{12}^2}{C_{1t}}}V_{n2,2}$ $-\frac{C_{12}}{C_{1t}}\frac{C_{23}}{C_{2t} - \frac{C_{12}^2}{C_{1t}}}V_{n1,2})(t - \tau_r)$ (7.90)
	$V_{n1,2} = B_{n1}(V_{dd} - V_{TN})^{n_n}$ (7.91)
	$V_{n2,2} = B_{n2}(V_{dd} - V_{TN})^{n_n}$ (7.92)
	$V_{p3,2} = B_{p3}(V_{dd} - V_{TP})^{n_p}$ (7.93)
	$\tau_{sat}^{min} = \min(\tau_{nsat}^1, \tau_{nsat}^2, \tau_{psat}^3)$ (7.94)

PMOS transistors have similar I-V characteristics in a dynamic transition, *i.e.*,

$$\frac{(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1}}{n_n+1} = \frac{(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p+1}}{n_p+1}, \tag{7.95}$$

where $\tau_n \leq t \leq \tau_r$, which is the ideal condition ensuring both rising and falling edges of the on-chip signals to be similar. For a two-line coupled system, the effective capacitive load of each inverter in an out-of-phase transition is approximated as

$$C_{1_{eff}} = \frac{C_1C_2 + C_c(C_1+C_2)}{C_2 + (1 - \frac{B_{p2}}{B_{n1}})C_c}, \tag{7.96}$$

$$C_{2_{eff}} = \frac{C_1C_2 + C_c(C_1+C_2)}{C_1 + (1 + \frac{B_{n1}}{B_{p2}})C_c}, \tag{7.97}$$

respectively. In this analysis, $B_{n1} = B_{p2}$ is assumed. The solid lines shown in Figure 7.6 describe the ratio of $C_{n1_{eff}}$ to $C_1 + 2C_c$, and the dotted lines depict the ratio of $C_{n2_{eff}}$ to $C_2 + 2C_c$. The horizontal axis represents the ratio of C_2 to C_1, and ratios of C_c to C_1 of 0.3, 0.5, and 0.7 are considered for each condition. If C_1 is identical to C_2, $C_{1_{eff}}$ and $C_{2_{eff}}$ are equal to $C_1 + 2C_c$ and $C_2 + 2C_c$, respectively. Note that the effective load capacitance of Inv_1 (Inv_2) may not be equal to C_1+2C_c ($C_2 + 2C_c$) due to the difference between the load capacitances.

For a three-line coupled system, the effective capacitive load of each CMOS inverter when the output of Inv_2 transitions from high-to-low while the outputs

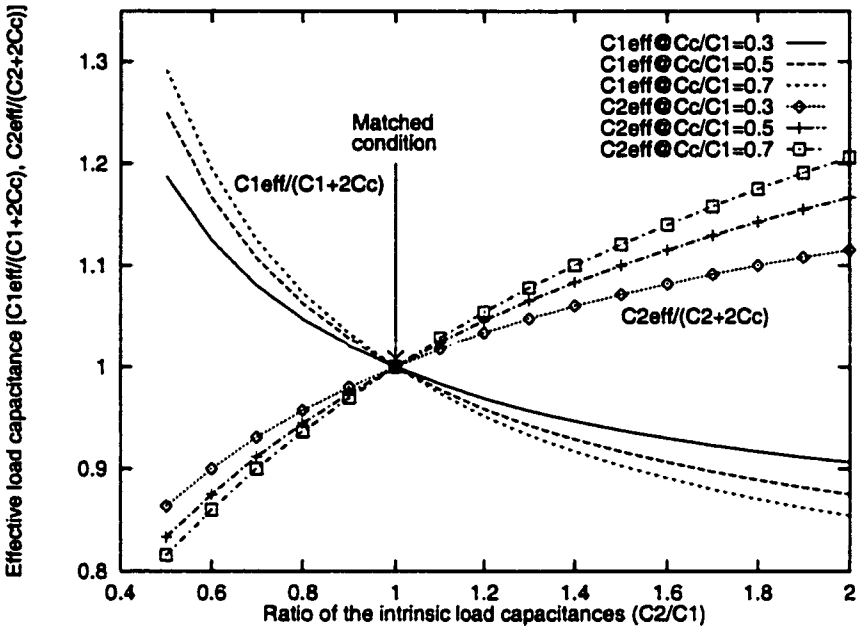


Figure 7.6: The ratio of the effective load capacitances $C_{1_{eff}}$ and $C_{2_{eff}}$ to $C_1 + 2C_c$ and $C_2 + 2C_c$, respectively, for an out-of-phase transition assuming $B_{n1} = B_{p2}$.

of Inv_1 and Inv_3 transition from low-to-high, is

$$C_{1_{eff}} = \frac{C_{1t} - \frac{C_{12}^2}{C_{2t} - \frac{C_{23}^2}{C_{3t}}}}{1 - \frac{C_{12}}{C_{2t} - \frac{C_{23}^2}{C_{3t}}} \frac{B_{n2}}{B_{p1}} + \frac{C_{23}}{C_{3t}} \frac{C_{12}}{C_{2t} - \frac{C_{23}^2}{C_{3t}}} \frac{B_{p3}}{B_{p1}}}, \tag{7.98}$$

$$C_{2_{eff}} = \frac{C_{1t} - \frac{C_{12}}{C_{1t}} C_{12} - \frac{C_{23}}{C_{3t}} C_{23}}{1 - \frac{C_{12}}{C_{1t}} \frac{B_{p1}}{B_{n2}} - \frac{C_{23}}{C_{3t}} \frac{B_{p3}}{B_{n2}}}, \tag{7.99}$$

$$C_{3_{eff}} = \frac{C_{3t} - \frac{C_{23}^2}{C_{2t} - \frac{C_{12}^2}{C_{1t}}}}{\frac{C_{12}}{C_{1t}} \frac{C_{23}}{C_{2t} - \frac{C_{12}^2}{C_{1t}}} \frac{B_{p1}}{B_{p3}} - \frac{C_{23}}{C_{2t} - \frac{C_{12}^2}{C_{1t}}} \frac{B_{n2}}{B_{p3}} + 1}, \tag{7.100}$$

respectively. When the outputs of Inv_1 and Inv_2 transition from high-to-low while the output of Inv_3 transitions from low-to-high, the effective capacitive load of

each CMOS inverter is

$$C_{1_{\text{eff}}} = \frac{C_{1t} - \frac{C_{12}^2}{C_{2t} - \frac{C_{23}^2}{C_{3t}}}}{1 + \frac{C_{12}}{C_{2t} - \frac{C_{23}^2}{C_{3t}}} \frac{B_{n2}}{B_{n1}} - \frac{C_{23}}{C_{3t}} \frac{C_{12}}{C_{2t} - \frac{C_{23}^2}{C_{3t}}} \frac{B_{p3}}{B_{n1}}}, \tag{7.101}$$

$$C_{2_{\text{eff}}} = \frac{C_{1t} - \frac{C_{12}}{C_{1t}} C_{12} - \frac{C_{23}}{C_{3t}} C_{23}}{\frac{C_{12}}{C_{1t}} \frac{B_{n1}}{B_{n2}} + 1 - \frac{C_{23}}{C_{3t}} \frac{B_{p3}}{B_{n2}}}, \tag{7.102}$$

$$C_{3_{\text{eff}}} = \frac{C_{3t} - \frac{C_{23}^2}{C_{2t} - \frac{C_{12}^2}{C_{1t}}}}{1 - \frac{C_{12}}{C_{1t}} \frac{C_{23}}{C_{2t} - \frac{C_{12}^2}{C_{1t}}} \frac{B_{n1}}{B_{n3}} - \frac{C_{23}}{C_{2t} - \frac{C_{12}^2}{C_{1t}}} \frac{B_{n2}}{B_{p3}}}, \tag{7.103}$$

respectively. The same conclusion for an out-of-phase transition can also be drawn as for an in-phase transition where the effective capacitive load of each CMOS inverter within a capacitively coupled system depends upon the intrinsic load capacitance, the coupling capacitance, and the transconductance of each active transistor.

7.4.3 Propagation Delay Time

Similar to the procedure of an in-phase transition, analytical expressions characterizing the propagation delay of each CMOS inverter during an out-of-phase transition within a two-line and a three-line coupled system are listed in Table 7.15.

Based on the same assumption, when the outputs of Inv_1 and Inv_2 transition from high-to-low while the output of Inv_3 transitions from low-to-high, the propagation delay of each CMOS inverter can be determined from (7.88), (7.89), and (7.90), respectively.

A comparison of the analytic propagation delay of a CMOS inverter with SPICE for an out-of-phase transition is listed in Tables 7.17 and 7.18 for a two-line and a three-line coupled system, respectively. The delay is estimated based on the intrinsic load capacitances plus two times the coupling capacitance for the

Table 7.15: Propagation delay of a CMOS inverter in a two-line and three-line coupled system

Out-of-phase transition for a two-line coupled system

$$t_{P_{HL1}} = \frac{(V_1(\tau_r) - 0.5V_{dd})(C_1C_2 + C_c(C_1 + C_2))}{(C_2 + C_c)B_{n1}(V_{dd} - V_{TN})^{n_n} - C_cB_{p2}(V_{dd} - V_{TP})^{n_p}} + \tau_r \tag{7.104}$$

$$t_{P_{LH2}} = \frac{(0.5V_{dd} - V_2(\tau_r))(C_1C_2 + C_c(C_1 + C_2))}{(C_2 + C_c)B_{p2}(V_{dd} - V_{TP})^{n_p} - C_cB_{n1}(V_{dd} - V_{TN})^{n_n}} + \tau_r \tag{7.105}$$

$$V_1(\tau_r) = V_{dd} - \frac{\frac{(C_2+C_c)\tau_r}{(n_n+1)V_{dd}}B_{n1}(V_{dd} - V_{TN})^{n_n+1} - \frac{C_c\tau_r}{(n_p+1)V_{dd}}B_{p2}(V_{dd} - V_{TP})^{n_p+1}}{C_1C_2 + C_c(C_1 + C_2)}$$
$$-R_1B_{n1}(V_{dd} - V_{TN})^{n_n} \tag{7.106}$$

$$V_2(\tau_r) = \frac{\frac{(C_1+C_c)\tau_r}{(n_p+1)V_{dd}}B_{p2}(V_{dd} - V_{TP})^{n_p+1} - \frac{C_c\tau_r}{(n_n+1)V_{dd}}B_{n1}(V_{dd} - V_{TN})^{n_n+1}}{C_1C_2 + C_c(C_1 + C_2)}$$
$$-R_2B_{p2}(V_{dd} - V_{TP})^{n_p} \tag{7.107}$$

no coupling condition [23, 78, 108]. The maximum error under the *no coupling* condition can exceed 18% of SPICE for a two-line coupled system and 35% of SPICE for a three-line coupled system, while the maximum error of the analytic propagation delay model listed in Table 7.15 is within 11% of SPICE.

7.5 At Least One Inverter is Quiet

For a two-line coupled system, the condition under which one inverter is active and the other is quiet has the highest probability of occurring, 4/9 (see Table 7.2). The probability of at least one inverter being quiet is 18/27 (excluding all three inverters being quiet at the same time) for a three-line coupled system (see Table 7.3). The propagation delay of an active inverter and the coupling noise voltage at the output of a quiet inverter are discussed in Section 7.5.1 for a two-line coupled system. A similar analysis of a three-line coupled system is

Table 7.16: Propagation delay of a CMOS inverter in a two-line and three-line coupled system (continued)

Out-of-phase transition for a three-line coupled system
Inv_2 transitions from high-to-low while Inv_1 and Inv_3 transition from low-to-high

$$t_{P_{LH1}} = \frac{[0.5V_{dd} - V_1(\tau_r)][C_{1t}(C_{2t} - \frac{C_{23}^2}{C_{3t}}) - C_{12}^2]}{B_{p1}(V_{dd} - V_{TP})^{n_p} - \frac{C_{12}}{C_{2t} - \frac{C_{23}^2}{C_{3t}}} B_{n2}(V_{dd} - VTN)^{n_n} + \frac{C_{23}}{C_{3t}} \frac{C_{12}}{C_{2t} - \frac{C_{23}^2}{C_{3t}}} B_{p3}(V_{dd} - V_{TP})^{n_p}} + \frac{\tau_r}{2} \quad (7.108)$$

$$t_{P_{HL2}} = \frac{[V_2(\tau_r) - 0.5V_{dd}][C_{2t} - \frac{C_{12}^2}{C_{1t}} - \frac{C_{23}^2}{C_{3t}}]}{B_{n2}(V_{dd} - VTN)^{n_n} - \frac{C_{12}}{C_{1t}} B_{p1}(V_{dd} - V_{TP})^{n_p} - \frac{C_{23}}{C_{3t}} B_{p3}(V_{dd} - V_{TP})^{n_p}} + \tau_r \quad (7.109)$$

$$t_{P_{LH3}} = \frac{[0.5V_{dd} - V_3(\tau_r)][C_{3t}(C_{2t} - \frac{C_{13}^2}{C_{1t}}) - C_{23}^2]}{B_{p3}(V_{dd} - V_{TP})^{n_p} - \frac{C_{23}}{C_{2t} - \frac{C_{12}^2}{C_{1t}}} B_{n2}(V_{dd} - VTN)^{n_n} + \frac{C_{12}}{C_{1t}} \frac{C_{23}}{C_{2t} - \frac{C_{12}^2}{C_{1t}}} B_{p1}(V_{dd} - V_{TP})^{n_p}} + \frac{\tau_r}{2} \quad (7.110)$$

$$V_1(\tau_r) = \frac{C_{2t} - \frac{C_{23}^2}{C_{3t}}}{C_{1t}(C_{2t} - \frac{C_{23}^2}{C_{3t}}) - C_{12}^2} \left(\frac{\tau_r B_{p1}(V_{dd} - V_{TP})^{n_p+1}}{(n_p+1)V_{dd}} - \frac{C_{12}}{C_{2t} - \frac{C_{23}^2}{C_{3t}}} \frac{\tau_r B_{n2}(V_{dd} - V_{TN})^{n_n+1}}{(n_n+1)V_{dd}} \right.$$
$$\left. + \frac{C_{23}}{C_{3t}} \frac{C_{12}}{C_{2t} - \frac{C_{23}^2}{C_{3t}}} \frac{\tau_r B_{p3}(V_{dd} - V_{TP})^{n_p+1}}{(n_p+1)V_{dd}} \right) + R_1 B_{p1}(V_{dd} - V_{TP})^{n_p} \quad (7.111)$$

$$V_2(\tau_r) = V_{dd} - \frac{1}{C_{2t} - \frac{C_{12}^2}{C_{1t}} - \frac{C_{23}^2}{C_{3t}}} \left(\frac{\tau_r B_{n2}(V_{dd} - V_{TN})^{n_n+1}}{(n_n+1)V_{dd}} - \frac{C_{12}}{C_{1t}} \frac{\tau_r B_{p1}(V_{dd} - V_{TP})^{n_p+1}}{(n_p+1)V_{dd}} \right.$$
$$\left. - \frac{C_{23}}{C_{3t}} \frac{\tau_r B_{p3}(V_{dd} - V_{TP})^{n_p+1}}{(n_p+1)V_{dd}} \right) - R_2 B_{n2}(V_{dd} - V_{TN})^{n_n} \quad (7.112)$$

$$V_3(\tau_r) = \frac{C_{2t} - \frac{C_{12}^2}{C_{1t}}}{C_{3t}(C_{2t} - \frac{C_{12}^2}{C_{1t}}) - C_{23}^2} \left(\frac{\tau_r B_{p3}(V_{dd} - V_{TP})^{n_p+1}}{(n_p+1)V_{dd}} - \frac{C_{23}}{C_{2t} - \frac{C_{12}^2}{C_{1t}}} \frac{\tau_r B_{n2}(V_{dd} - V_{TN})^{n_n+1}}{(n_n+1)V_{dd}} \right.$$
$$\left. + \frac{C_{12}}{C_t} \frac{C_{23}}{C_{2t} - \frac{C_{12}^2}{C_{1t}}} \frac{\tau_r B_{p3}(V_{dd} - V_{TP})^{n_p+1}}{(n_p+1)V_{dd}} \right) + R_3 B_{p3}(V_{dd} - V_{TP})^{n_p} \quad (7.113)$$

Table 7.17: Comparison of an out-of-phase transition with SPICE for a two-line coupled system assuming $w_p = 2w_n$

	Circuit parameters							SPICE		No coupling				Analytic estimation			
τ_r (ns)	w_{n1} (μm)	R_1 (Ω)	C_1 (pF)	w_{n2} (μm)	R_2 (Ω)	C_2 (pF)	C_c (pF)	τ_1 (ns)	τ_2 (ns)	τ_1 (ns)	τ_2 (ns)	δ_1 (%)	δ_2 (%)	τ_1 (ns)	τ_2 (ns)	δ_1 (%)	δ_2 (%)
0.2	3.6	100	0.1	3.6	100	0.2	0.1	200	321	218	267	9.0	16.8	186	314	7.0	2.2
0.2	3.6	100	0.2	3.6	100	0.1	0.1	321	200	267	218	16.8	9.0	314	186	2.2	7.0
0.2	3.6	100	0.2	5.4	100	0.3	0.1	311	225	276	202	11.3	10.2	307	212	1.3	5.8
0.2	5.4	100	0.3	3.6	100	0.2	0.1	225	311	202	276	10.2	11.3	212	307	5.8	1.3
0.2	3.6	100	0.2	5.4	100	0.2	0.1	341	184	276	201	19.1	9.2	367	177	7.5	3.8
0.2	5.4	100	0.2	3.6	100	0.2	0.1	184	341	201	276	9.2	19.1	177	367	3.8	7.5
0.4	5.4	100	0.2	5.4	100	0.4	0.2	270	437	235	355	12.9	18.8	281	423	4.1	3.2
0.4	5.4	100	0.4	3.6	100	0.2	0.2	437	270	355	235	18.8	12.9	423	281	3.2	4.1
0.4	5.4	100	0.2	5.4	100	0.4	0.3	329	515	368	425	11.9	17.5	304	505	7.6	2.0
0.4	5.4	100	0.4	5.4	100	0.2	0.3	515	329	425	368	17.5	11.9	505	304	2.0	7.6

Statistic analysis	No coupling	Analytic estimation
Maximum error (%)	19.1	7.6
Average error (%)	13.7	4.4

Table 7.18: Comparison of an out-of-phase transition with SPICE for a three-line coupled system

	Circuit parameters											SPICE	No coupling		Analytic	
τ_r (ns)	w_{p1} (μm)	R_1 (Ω)	C_1 (pF)	w_{n2} (μm)	R_2 (Ω)	C_2 (pF)	w_{p3} (μm)	R_3 (Ω)	C_3 (pF)	C_{12} (pF)	C_{23} (pF)	τ_2 (ns)	τ_2 (ns)	δ_2 (%)	τ_2 (ns)	δ_2 (%)
0.2	3.6	80	0.1	3.6	100	0.2	3.6	90	0.1	0.1	0.1	437	422	3.4	443	1.4
0.2	3.6	100	0.1	5.4	100	0.2	3.6	100	0.1	0.1	0.1	225	269	19.6	208	7.6
0.2	3.6	100	0.1	3.6	0.05	100	3.6	100	0.1	0.05	0.05	153	191	24.8	139	9.2
0.2	3.6	100	0.1	3.6	100	0.05	3.6	100	0.1	0.1	0.1	246	323	31.3	226	8.1
0.2	3.6	100	0.1	5.4	100	0.1	3.6	100	0.1	0.1	0.1	165	229	38.8	146	11.5
0.2	7.2	150	0.2	5.4	100	0.1	3.6	100	0.1	0.1	0.1	185	229	23.8	167	9.7
0.2	7.2	150	0.2	5.4	100	0.1	7.2	100	0.2	0.1	0.1	212	229	8.0	196	7.6
0.2	7.2	150	0.2	5.4	100	0.1	7.2	100	0.2	0.15	0.15	307	325	5.9	295	3.9
0.2	7.2	150	0.2	7.2	100	0.1	7.2	100	0.2	0.15	0.15	176	221	25.6	161	8.5

Statistic analysis	No coupling	Analytic estimation
Maximum error (%)	38.8	11.5
Average error (%)	20.1	7.5

presented in Section 7.5.2. Analytical estimations are also compared to SPICE in Section 6.5.5.

7.5.1 Two-Line Coupled Structure

For either an in-phase or an out-of-phase transition, the coupling capacitance affects the waveform of the output voltage and the propagation delay of each inverter, changing (primarily decreasing) the speed of a CMOS integrated circuit [23, 92, 93]. Interconnect coupling capacitances typically degrade the performance of a CMOS integrated circuit. If one inverter is active and the other is quiet, the active transition can induce a voltage change at the output of a quiet inverter through the coupling capacitance. The coupled noise voltage may seriously affect the circuit behavior and related power dissipation characteristics [22, 27, 34, 37, 39].

In the following analysis, the output of Inv_1 is assumed to transition from high-to-low while the input of Inv_2 is fixed at V_{dd}. Therefore, the initial voltage of V_1 and V_2 are V_{dd} and ground, respectively. The input voltage of Inv_1 is assumed to be shaped as a rising ramp signal [defined in (5.1)]. When the input voltage exceeds V_{TN}, $NMOS_1$ is ON and starts operating in the saturation region. $NMOS_2$ operates in the linear region due to the small voltage change at the output. The differential equations, (7.1) and (7.2), become (7.114) and (7.115), respectively. There are no tractable solutions to these coupled differential equations, (7.114) and (7.115). In order to derive a tractable solution, it is necessary to make certain simplifying assumptions.

Table 7.19: One line is active and the other is quiet in a two-line coupled system

Differential equations $(\tau_n \leq t \leq \tau_r)$	
$(C_1+C_c)\frac{dV_1}{dt} - (1+R_2\gamma_{n2})C_c\frac{dV_2}{dt} = -B_{n1}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n} - R_1B_{n1}\frac{d(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}}{dt},$	(7.114)
$(1+R_2\gamma_{n2})(C_2+C_c)\frac{dV_2}{dt} - C_c\frac{dV_1}{dt} = -\gamma_{n2}V_2,$	(7.115)
Step input approximation $(t \leq \tau_{nsat}^1)$	
$V_1 = V_{dd} - \frac{B_{n1}}{C_1+C_c}(V_{dd}-V_{TN})^{n_n}t + \frac{C_c}{C_1+C_c}V_2$	(7.116)
$V_2 = -\frac{C_c}{(C_1+C_c)\gamma_{n2}}B_{n1}(V_{dd}-V_{TN})^{n_n}(1-e^{-\alpha_{n2}t})$	(7.117)
$\alpha_{n2} = \frac{(C_1+C_c)\gamma_{n2}}{(1+R_2\gamma_{n2})(C_1C_2+C_c(C_1+C_2))}$	(7.118)
	(7.119)

Table 7.20: One line is active and the other is quiet in a two-line coupled system (continued)

Current through $NMOS_2$ is negligible

$\tau_n \le t \le \tau_r$

$$V_1 = V_{dd} - R_1 B_{n1}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n} - \frac{C_2 + C_c}{C_1C_2 + C_c(C_1 + C_2)} \frac{B_{n1}\tau_r}{(n_n + 1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1} \quad (7.120)$$

$$V_2 = \frac{C_c}{C_1C_2 + C_c(C_1 + C_2)} \frac{B_{n1}\tau_r}{(1 + R_2\gamma_{n2})(n_n + 1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1} \quad (7.121)$$

$\tau_r \le t \le \tau^1_{nsat}$

$$V_1 = V_1(\tau_r) - \frac{B_{n1}}{C_1 + C_c}(V_{dd} - V_{TN})^{n_n}(t - \tau_r) - \frac{C_c(1 + R_2\gamma_{n2})}{C_1 + C_c}(V_2(\tau_r) + V_{2,a})(1 - e^{-\alpha_{n2}(t-\tau_r)}) \quad (7.122)$$

$$V_2 = -V_{2,a} + (V_2(\tau_r) + V_{2,a})e^{-\alpha_{n2}(t-\tau_r)} \quad (7.123)$$

$$V_{2,a} = \frac{C_cB_{n1}}{(C_1 + C_c)\gamma_{n2}}(V_{dd} - V_{TN})^{n_n} \quad (7.124)$$

$$\alpha_{n2} = \frac{(C_1 + C_c)\gamma_{n2}}{(1 + R_2\gamma_{n2})(C_1C_2 + C_c(C_1 + C_2))} \quad (7.125)$$

Approximation of the drain-to-source current

$\tau_n \le t \le \tau_r$

$$V_1 = V_{dd} - \frac{1}{C_1 + C_c}V_{1,a} - R_1B_{n1}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n} + \frac{C_c(1 + R_2\gamma_{n2})}{C_1 + C_c}V_2 \quad (7.126)$$

$$V_2 = B_1\xi + B_2\xi^2 + (1 - B_0)e^{-\alpha_{n2}(t-\tau_n)} \quad (7.127)$$

$$V_{1,a} = B_{n1}\frac{\tau_r}{(n_n + 1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1} \quad (7.128)$$

$$B_0 = -\frac{C_c}{(C_1 + C_c)\gamma_{n2}}A_0 + \frac{C_cC_t(1 + R_2\gamma_{n2})}{(C_1 + C_c)^2\gamma^2_{n2}\tau_r}A_1 - 2\frac{C_cC_t^2(1 + R_2\gamma_{n2})^2}{(C_1 + C_c)^3\gamma^3_{n2}\tau^2_r}A_2 \quad (7.129)$$

$$B_1 = 2\frac{C_cC_t(1 + R_2\gamma_{n2})}{(C_1 + C_c)^2\gamma^2_{n2}\tau_r}A_2 - \frac{C_c}{(C_1 + C_c)\gamma_{n2}}A_1 \quad (7.130)$$

$$B_2 = -\frac{C_c}{(C_1 + C_c)\gamma_{n2}}A_2 \quad (7.131)$$

$$C_t = C_1C_2 + C_c(C_1 + C_2) \quad (7.132)$$

Step Input Approximation

If the transition time of the input signal is small as compared to the propagation delay of a CMOS inverter and the output transition time, the input can be approximated as a step input. Analytical expressions characterizing the output voltage of Inv_1 and the coupling noise voltage at the output of Inv_2 before $NMOS_1$ starts to operate in the linear region are listed in Table 7.19. The time τ^1_{nsat} when $NMOS_1$ leaves the saturation region can be determined by applying a Newton-Raphson algorithm to (7.116).

The propagation delay of Inv_1 can be approximated from (7.116) by also applying a Newton-Raphson iteration technique. Since the current through $NMOS_2$ discharges the capacitor C_1, the propagation delay is less than the estimated delay based on a load of $C_1 + C_c$.

After τ^1_{nsat}, both of the NMOS transistors operate in the linear region. The solutions for the peak voltage can be obtained from the initial values of V_1 and V_2, as described in Appendix B. Note that V_2 decreases exponentially in the linear region. The peak noise occurs at τ^1_{nsat},

$$V_2(peak) = -\frac{C_c}{(C_1 + C_c)\gamma_{n2}} B_{n1}(V_{dd} - V_{TN})^{n_n}(1 - e^{-\alpha_{n2}\tau_{nsat1}}). \tag{7.133}$$

Current through $NMOS_2$ is Negligible

The analysis described in this section is based on the assumption that the current through $NMOS_2$ can be neglected, *i.e.*, $\gamma_{n2}V_2$ is small as compared to $C_c\frac{dV_1}{dt}$ in (7.115). Based on this assumption, the solutions of V_1 and V_2 are (7.120) and (7.121), respectively. The effective load capacitance of Inv_1 is

$$C_{1_{eff}} = (C_1 + \frac{C_2}{C_2 + C_c}C_c) \leq (C_1 + C_c). \tag{7.134}$$

When the input signal reaches V_{dd} at τ_r, $NMOS_1$ continues to operate in the saturation region. However, the coupling noise voltage V_2 at τ_r is

$$V_2(\tau_r) = \frac{C_c}{C_1C_2 + C_c(C_1 + C_2)} \frac{B_{n1}\tau_r}{(1 + R_2\gamma_{n2})(n_n + 1)V_{dd}}(V_{dd} - V_{TN})^{n_n+1}. \quad (7.135)$$

Note that $\gamma_2 V_2$ cannot be neglected after the input transition is completed since $\gamma_2 V_2$ may be comparable to $C_c\frac{dV_1}{dt}$. Therefore, the $\gamma_2 V_2$ term in (7.115) is considered in the derivation once the input transition is completed. After τ_r, the output voltages of V_1 and V_2 are described by (7.122) and (7.123), respectively. τ^1_{nsat} (the time when $NMOS_1$ leaves the saturation region) and $t_{0.5}$ (the time when V_1 reaches $0.5V_{dd}$) are determined from (7.122) by applying a Newton-Raphson iteration. The peak coupling noise voltage can be approximated at τ^1_{nsat} and is equal to $V_2(\tau^1_{nsat})$ which is determined from (7.123).

Approximation of the Drain-to-Source Current

A simplification in which the current through $NMOS_2$ is assumed to be negligible is appropriate when $\gamma_{n2}V_2$ is small as compared to $C_c\frac{dV_1}{dt}$ in (7.115). If $\gamma_{n2}V_2$ is comparable to $C_c\frac{dV_1}{dt}$, the current through $NMOS_2$ cannot be neglected.

In order to derive tractable solutions, the drain-to-source current of $NMOS_1$ can be approximated using a second order polynomial expansion,

$$B_{n1}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n} \approx A_0 + A_1\xi + A_2\xi^2, \quad (7.136)$$

where $\xi = \frac{t}{\tau_r} - \frac{V_{TN}}{V_{dd}}$ and A_0, A_1, and A_2 are determined from a polynomial expansion of the drain-to-source current of $NMOS_1$. Solutions of the differential equations represented by (7.114) and (7.115) are (7.126) and (7.127).

After the input transition is completed, $NMOS_1$ continues to operate in the saturation region. The analysis after τ_r is the same as the condition under which

the current through $NMOS_2$ is negligible, which is described in section 6.5.2. V_2 exhibits an exponential decay when both transistors operate in the linear region. Therefore, the peak coupling noise voltage can be approximated at τ^1_{nsat}.

Delay Uncertainty of An Active Logic Gate

In the previous analysis, the output of Inv_1 is assumed to transition from high-to-low and the input of Inv_2 is fixed at V_{dd}. Note that the current through $NMOS_2$ discharges C_1, and the estimated delay is smaller than the estimated delay based on $C_1 + C_c$. If the input of Inv_2 is at ground and $PMOS_2$ is ON, the coupling capacitance affects the propagation delay of Inv_1 differently.

The effect of the initial state can be demonstrated with a step input signal. If the initial value of both V_1 and V_2 is V_{dd}, and since $NMOS_1$ operates in the saturation region, the output voltages are

$$V_1 = V_{dd} - \frac{B_{n1}}{C_1 + C_c}(V_{dd} - V_{TN})^{n_n} t + \frac{C_c}{C_1 + C_c} V_{p2}, \tag{7.137}$$

$$V_2 = V_{dd} - \frac{C_c B_{n1}(V_{dd} - V_{TN})^{n_n}}{(C_1 + C_c)\gamma_{p2}}(1 - e^{-\alpha_{p2} t}), \tag{7.138}$$

where

$$V_{p2} = \frac{C_c}{C_1 + C_c} B_{n1}(V_{dd} - V_{TN})^{n_n}(1 - e^{-\alpha_{p2} t}), \tag{7.139}$$

$$\alpha_{p2} = \frac{\gamma_{p2}}{1 + R_2\gamma_{p2}} \frac{C_1 + C_c}{C_1 C_2 + C_c(C_1 + C_2)}. \tag{7.140}$$

The propagation delay of Inv_1 can be approximated by (6.73). Since the current through $PMOS_2$ slows down the discharge process, the propagation delay is greater than the delay calculated assuming $C_1 + C_c$ is the load capacitance. The peak coupling noise voltage also occurs at the time when $NMOS_1$ leaves the saturation region.

Undershoots are exhibited when the active inverter transitions from high-to-low and the quiet state is at a logic low (ground). Overshoots may occur when the active inverter transitions from low-to-high and the quiet state is at a logic high (V_{dd}). Overshoots or undershoots may cause carrier injection or collection in the substrate, possibly corrupting a data signal in dynamic logic circuits [18, 102].

7.5.2 Three-Line Coupled Structure

For a three-coupled system, the probability of two inverters being quiet and the other being active (condition 1) is 6/27 (see Table 7.3). If two inverters are quiet and the other inverter is active, the active inverter and the neighboring quiet inverter are equivalent to a system of two coupled interconnect lines. Therefore, the analysis made in section 7.5.1 for a two-line coupled structure can be applied to this condition.

The probability of one inverter being quiet and the other two being active (condition 2) is 12/27 (see Table 7.3) for a three-line coupled system. However, there are two different cases under condition 2: Inv_2 is quiet while both Inv_1 and Inv_3 are active; and Inv_1 is quiet while both Inv_2 and Inv_3 are active (or Inv_3 is quiet while both Inv_1 and Inv_2 are active). Based on the previous analysis of a two-line coupled system, a three-line coupled system can be simplified to an equivalent two-line coupled system.

Inv_2 is Quiet while both Inv_1 and Inv_3 are Active

The coupled noise voltage at the output of Inv_2, which is induced by the active transition at the outputs of Inv_1 and Inv_3, is very small as compared to the voltage change at the outputs of Inv_1 and Inv_3. Therefore, the coupling noise voltage can

be considered to have a negligible effect on the active transition at the outputs of both Inv_1 and Inv_3. The coupling noise voltage induced by the active transition at the output of Inv_1 is assumed to have no effect on the active transition at the output of Inv_3. The coupling noise voltage is proportional to $\frac{C_{12}}{C_1+C_{12}}\frac{C_{23}}{C_2+C_{23}}$ assuming a step input signal. Similarly, the coupling noise voltage induced by the active transition at the output of Inv_3 is assumed to have no effect on the active transition at the output of Inv_1. The coupling noise voltage is proportional to $\frac{C_{23}}{C_3+C_{23}}\frac{C_{12}}{C_2+C_{12}}$ assuming a step input signal. As shown in Figure 7.4, with this assumption, Inv_1 and Inv_2 (and Inv_2 and Inv_3) can be treated as a two-line coupled system. Therefore, a three-line coupled system can be decomposed into two two-line coupled systems. The coupling noise voltage at the output of Inv_2 is a linear superposition of these two individual noise voltages caused by the dynamic transition at the outputs of both Inv_1 and Inv_3. The propagation delay of Inv_1 and Inv_3 can be determined from the analysis of a two-line coupled system as discussed in section 7.5.1.

Note that if Inv_1 and Inv_3 have the same dynamic transitions, the coupling noise voltage at the output of Inv_2 is the summation of these two individual noise voltages caused by Inv_1 and Inv_3. This summation is the worst case in terms of producing a high peak noise voltage at the output of Inv_2 (assuming Inv_1 and Inv_3 are triggered close in time with approximately the same input slew rate). If Inv_1 and Inv_3 transition in the opposite directions, the coupling noise at the output of Inv_2 is the difference between the two individual noise voltages induced by Inv_1 and Inv_3. This condition is the best case in terms of minimizing the peak noise voltage at the output of Inv_2 (assuming Inv_1 and Inv_3 are triggered close in time with approximately the same input slew rate).

*Inv*1 is Quiet while both Inv_2 and Inv_3 are Active

For a three-line coupled system as shown in Figure 7.4, when Inv_1 is quiet while both Inv_2 and Inv_3 are active, this system can be simplified to an equivalent two-coupled system as shown in Figure 7.7. In this figure, the intrinsic load capacitance at the output of Inv_2 is $C_{2_{eff}}$ rather than C_2. The effective capacitive load $C_{2_{eff}}$ is determined based on the signal activity at the outputs of Inv_2 and Inv_3 [(7.42) or (7.43) for an in-phase transition and (7.96) or (7.97) for an out-of-phase transition], which has been discussed in sections 7.3.2 and 7.4.2, respectively. Therefore, the analysis of a two-line coupled system as described in section 7.5.1 can be applied to this simplified three-line coupled system (as illustrated in Figure 7.7).

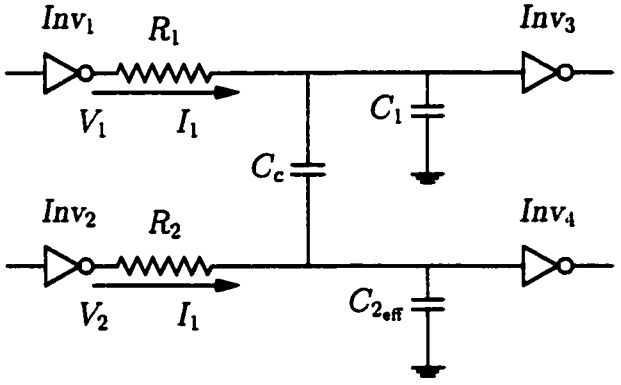


Figure 7.7: A simplified circuit diagram of a three-line coupled system when Inv_1 is quiet while Inv_2 and Inv_3 are dynamically transitioning.

7.5.3 Comparison with SPICE

For a two-line coupled system, the propagation delay of the active CMOS inverter and the peak coupling noise voltage at the output of the quiet inverter are compared to SPICE in Table 7.21. The propagation delay of the active CMOS

inverter is based on the intrinsic capacitance plus the coupling capacitance for the *no coupling* condition, *i.e.*, $C_1 + C_c$ for Inv_1 or $C_2 + C_c$ for Inv_2 [23, 78, 108]. The maximum error of the propagation delay based on the *no coupling* condition can exceed 15% as compared to SPICE while the maximum error of the proposed delay model is less than 5% as compared to SPICE. The maximum and average improvement of the proposed propagation delay model are 13% and 7% of SPICE, respectively. The peak coupling noise voltage based on these analytical expressions is within 10% as compared to SPICE. Note that as the size of the quiet inverter is increased, the peak noise voltage is reduced, as illustrated by comparing the third and fifth row listed in Table 7.21. However, this technique increases the propagation delay of the active CMOS inverter (Inv_1 for this case).

For a three-line coupled system, when Inv_2 is quiet and the other two lines are active, the peak coupling noise voltage at the output of Inv_2 is compared to SPICE in Table 7.22. The analytical prediction for this condition is within 13% of SPICE using a linear superposition method based on summing the effects of two two-line coupled systems, as described in section 7.5.2. Note that when Inv_1 and Inv_3 both transition in-phase, the coupling noise voltage at Inv_2 is greater than the peak noise voltage when Inv_1 and Inv_3 transition out-of-phase. Moreover, if Inv_1 and Inv_3 are similarly sized, these two individual noise voltages may compensate (or negatively resonate) in an out-of-phase transition, making the coupling noise voltage at Inv_2 almost negligible (assuming the two signal transitions occur close in time).

Table 7.21: Comparison of Inv_1 active and Inv_2 quiet with SPICE

	Circuit parameters							Initial	Delay of Inv_1					Peak voltage of Inv_2		
									SPICE	No Coupling		Analytic		SPICE	Analytic	
τ_r (ns)	W_{n1} (μm)	R_1 (Ω)	C_1 (pF)	W_{n1} (μm)	R_1 (Ω)	C_1 (pF)	C_c (pF)	State of Inv_2	τ_1 (ps)	τ_1 (ps)	δ_1 (%)	τ_1 (ps)	δ_1 (%)	V_2 (V)	V_2 (V)	δ_2 %
0.2	1.8	100	0.1	1.8	100	0.1	0.05	L	232	244	5.2	236	1.7	-0.364	-0.352	3.3
0.2	1.8	100	0.1	1.8	100	0.1	0.05	H	230	244	6.1	227	1.3	4.54	4.61	7.0
0.2	1.8	100	0.1	1.8	100	0.1	0.1	L	277	315	13.7	284	2.5	-0.565	-0.586	3.7
0.2	1.8	100	0.1	1.8	100	0.1	0.1	H	270	315	16.7	264	2.2	4.26	4.42	3.8
0.2	1.8	100	0.1	3.6	100	0.1	0.1	L	289	315	9.0	293	1.4	-0.313	-0.327	4.5
0.2	1.8	100	0.1	3.6	100	0.1	0.1	H	284	315	10.9	274	3.5	4.59	4.62	0.7
0.2	3.6	100	0.2	3.6	100	0.2	0.1	L	219	230	5.0	224	2.3	-0.35	-0.344	1.7
0.2	3.6	100	0.2	3.6	100	0.2	0.1	H	216	230	6.5	221	2.3	4.56	4.66	2.2

	Delay of *Invl*		
	No coupling	Analytic estimation	V_2
Maximum error (%)	16.7	3.5	7.0
Average error (%)	9.1	2.2	3.4

Table 7.22: Comparison of Inv_2 being quiet while both Inv_1 and Inv_3 being active

τ_r (ns)	Circuit parameters											Action		Noise at Inv_2		
	w_{p1} (μm)	R_1 (Ω)	C_1 (pF)	w_{n2} (μm)	R_2 (Ω)	C_2 (pF)	w_{p3} (μm)	R_3 (Ω)	C_3 (pF)	C_{12} (pF)	C_{23} (pF)	Inv_1	Inv_3	SPICE (V)	Analytic (V)	Analytic (%)
0.2	1.8	100	0.1	1.8	100	0.1	1.8	100	0.1	0.05	0.05	HL	HL	-0.63	-0.71	12.7
0.2	1.8	100	0.1	1.8	100	0.1	1.8	100	0.1	0.05	0.05	HL	LH	0.016	0.0	N/A
0.2	1.8	100	0.1	1.8	100	0.1	1.8	100	0.1	0.05	0.05	LH	LH	0.74	0.68	8.1
0.2	1.8	100	0.1	1.8	100	0.1	1.8	100	0.1	0.1	0.1	HL	HL	-1.05	-1.17	11.4
0.2	1.8	100	0.1	1.8	100	0.1	1.8	100	0.1	0.1	0.1	HL	LH	0.020	0.0	N/A
0.2	1.8	100	0.1	1.8	100	0.1	1.8	100	0.1	0.1	0.1	LH	LH	1.18	1.08	8.5
0.2	1.8	100	0.1	3.6	100	0.1	1.8	100	0.1	0.1	0.1	HL	HL	0.60	0.62	3.3
0.2	1.8	100	0.1	3.6	100	0.1	1.8	100	0.1	0.1	0.1	HL	LH	0.014	0.0	N/A
0.2	1.8	100	0.1	3.6	100	0.1	1.8	100	0.1	0.1	0.1	LH	LH	0.67	0.63	6.0
Statistic analysis												Noise voltage V_2				
Maximum error (%)												12.7				
Average error (%)												8.3				

7.6 Minimizing Coupling Effects

Delay uncertainty can be minimized or even eliminated when both inverters and load capacitances are approximately the same, *i.e.*, $B_{n1} \approx B_{n2}$ and $C_1 \approx C_2$. For example, the coupling capacitance can be eliminated from the effective load capacitance under the condition of an in-phase transition. To reduce the propagation delay of a CMOS logic gate in a coupled system, the probability of an out-of-phase transition should be minimized because of the increased effective load capacitance. In order to minimize any delay uncertainty, all of these circuit elements should therefore be designed to be as similar to each other as possible.

However, if an out-of-phase transition cannot be avoided, the size of each transistor within a coupled system can be adjusted to optimize the propagation delay within a critical path by "transferring" some signal delay (through the effective capacitance) from one circuit branch to another circuit branch, an "advantage" of coupling capacitances. A proper strategy for adjusting the coupled system depends upon the device parameters, the circuit structure, and the design target of the various data paths.

The coupling noise voltage is proportional to B_{n1}/γ_{n2} and C_c. If the effective output conductance of the quiet inverter is increased, the peak noise voltage can be reduced. This conclusion suggests that the size of the MOS transistors within the quiet inverter should be increased, contradicting the observation for the propagation delay. Therefore, a tradeoff exists when choosing the appropriate size of the transistors for capacitively coupled inverters. The optimal size of these transistors is also related to the signal activity and other circuit constraints.

7.7 Summary

An analysis of a CMOS inverter driving a coupled resistive-capacitive interconnect is presented in this chapter. The uncertainty of the effective load capacitance and the propagation delay is noted for both an in-phase and an out-of-phase transition if the circuit elements are not equally sized or evenly balanced. The coupling noise voltage at the interconnect line driven by a quiet inverter is also analyzed. An analytical propagation delay model and a technique of estimating the peak coupling noise voltage are also presented for a system level analysis. Finally, some design strategies are suggested to reduce the noise and propagation delay caused by interconnect coupling capacitance.

Chapter 8

Peak Noise Estimation for Lossy Transmission Lines

8.1 Introduction

A trend in modern high speed, high density CMOS VLSI circuits is decreasing feature sizes as well as increasing chip dimensions. The delay of these highly scaled integrated circuits is now dominated by the interconnect [1, 15, 17, 81]. An important advantage of CMOS digital circuits in a noisy environment is that static CMOS logic gates can reject noise, *i.e.*, CMOS has a relatively high immunity to noise. However, as power supply levels decrease (the NTRS predicts the supply voltage will drop from 1.8 to 2.5 volts in 1999 to 0.6 to 0.9 volts in 2009 [1]), this advantage will diminish. Therefore, in addition to interconnect delay and power consumption, coupling noise (or crosstalk) between adjacent interconnect lines is also a primary concern in present and future generations of CMOS VLSI circuits [63–65, 108].

Coupling noise between adjacent interconnect can cause disastrous effects on the logical functionality and long-term reliability of a VLSI circuit [23]. Coupling effects have become more significant as the feature size is decreased to deep sub-micrometer dimensions because the spacing between conductor lines is decreased

and the thickness of the high level conductor lines is increased in order to reduce the parasitic resistance of the conductors.

If the peak noise voltage at the receiver is greater than the threshold voltage, it may cause a circuit to malfunction. Furthermore, the induced noise voltage may cause extra power to be dissipated on the quiet line due to momentary glitches within the logic gates. Carrier injection or collection within the substrate may occur as the coupling noise voltage rises above the power supply voltage V_{dd} or falls below ground [18]. These deleterious effects caused by the coupling noise voltage become aggravated as the relaxation time, the time for the coupling noise to reach a steady state voltage, increases. The effect of the coupling noise is also important in dynamic CMOS circuits, which are more sensitive to noise than static CMOS circuits. In the design of high speed VLSI circuits, it is important to be able to predict coupling noise at the system (or chip) level [78]. This information permits circuit malfunctions or extra power consumption caused by the coupling noise to be avoided [33]. The design cycle and cost can therefore be reduced as well as the circuit reliability improved.

An analysis of coupling noise can be performed in both the frequency domain and the time domain, but most of these analyses result in numerical solutions [110, 111] or an equivalent circuit simulation [112]. A numerical solution is not convenient at the system (or chip) level to predict noise effects since this approach requires excessive simulation time and computer memory. The analytical analysis of coupled *lossless* transmission lines in the time domain has been addressed in [113]. A lossless model, however, is not appropriate for interconnect in CMOS VLSI circuits since the parasitic interconnect resistance typically cannot be neglected.

An analysis of coupled interconnect in CMOS VLSI circuits is presented in this chapter. For simplicity, the interconnect is modeled as a uniform transmission line [43] and the coupled interconnect lines are assumed to be in parallel. Although with interspersed contacts the interconnect lines are not uniform and coupled interconnect lines are not often parallel over long distances in many VLSI layouts, a uniform transmission line is used to model the distributed interconnect impedance. Also, coupling effects are typically more pronounced in parallel structures than in crossover structures [62].

Analytical equations are derived from time domain differential equations using Laplace transforms with the assumption that the effect of the coupling noise on the active line is neglected. The rationality of this assumption is discussed in greater detail within this chapter. The accuracy of the predicted peak noise voltage based on these closed form expressions is within 20% for the driver end coupling noise voltage and 15% for the receiver end coupling noise voltage. The dependence of the propagation delay of the CMOS driver stage on the driver impedance and the relationship between the relaxation time of the coupling noise voltage and the driver impedance are also investigated. Note that the shortest propagation delay and relaxation time occur when the driver output impedance matches the interconnect impedance.

An analytical model of a CMOS driver and receiver structure, as well as closed form expressions of the coupling noise voltage at both ends of the quiet interconnect line, are addressed in Section 8.2. The predicted peak coupling noise voltage based on the analytical equations is compared with dynamic circuit simulations in Section 8.3. A discussion of the coupling noise voltage of a lossy interconnect and the effect of the coupling noise on CMOS VLSI circuits, the driver output

impedance, and the relaxation time of the coupling noise voltage are discussed in Section 8.4 followed by some concluding remarks in Section 8.5.

8.2 Noise Coupling Equations

Consider a CMOS driver and receiver structure in a high speed VLSI circuit, an example of which is schematically shown in Figure 8.1(a). Inv_1 is the active driver and Inv_3 is the quiet driver, and Inv_2 and Inv_4 are the receivers. The interconnect between the CMOS driver and receiver is modeled as a lossy transmission line. In order to analyze the coupling noise, the CMOS drivers are modeled as a linear resistor (R_1 and R_2) and the receivers are modeled as a capacitive load (C_{l1} and C_{l2}). The interconnect between the active driver Inv_1 and the receiver Inv_2 is the active line, and the interconnect between the quiet driver Inv_3 and the receiver Inv_4 is the quiet line.

The equivalent circuit model is shown in Figure 8.1(b), where two coupled lossy transmission lines have similar impedance characteristics, *i.e.*, R, L, and C are the same for each line. Line 1 is the active (or aggressor) line and line 2 is the quiet (or victim) line.

Laplace transforms are used to solve the time domain differential equations characterizing this structure. The resulting formulation is

$$\frac{\partial^2}{\partial x^2}V_1(x,s) = A_1V_1(x,s) + B_1V_2(x,s), \tag{8.1}$$

$$\frac{\partial^2}{\partial x^2}V_2(x,s) = A_2V_1(x,s) + B_2V_2(x,s), \tag{8.2}$$

where

$$A_1 = B_2 = sRC + s^2LC - s^2L_mC_m, \tag{8.3}$$

$$B_1 = A_2 = s^2L_mC - s^2LC_m - sRC_m. \tag{8.4}$$

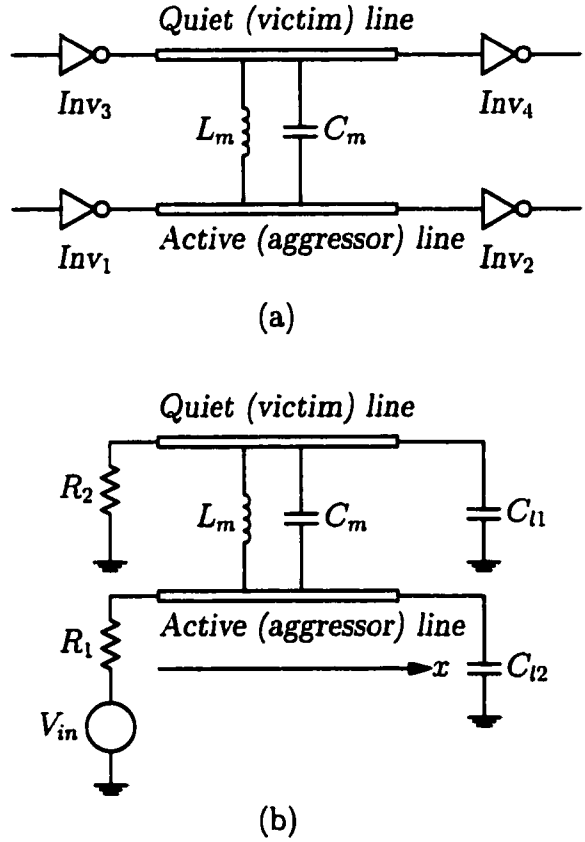


Figure 8.1: An example of a CMOS driver and receiver structure. a) Two adjacent CMOS drivers and receivers. b) A simplified circuit model of the structure.

R, L, and C are the line resistance, inductance, and capacitance per unit length, respectively. L_m and C_m are the coupling inductance and capacitance per unit length between line 1 and line 2. The minus sign in (8.3) and (8.4) occurs since C_m is a positive value [84, 111]. $V_1(x,s)$ and $V_2(x,s)$ are the Laplace transform of the voltages between line 1 and line 2, respectively, and ground.

In order to simplify this analysis, only first order effects are considered, where the voltage on line 1 affects the voltage on line 2 and $V_2(x,s)$ is sufficiently small to have a negligible effect on line 1. This situation is caused by the voltage on line 1 coupling onto line 2. Based on this assumption, (8.1) and (8.2) simplify to

$$\frac{\partial^2}{\partial x^2}V_1(x,s) = \gamma^2 V_1(x,s), \tag{8.5}$$

$$\frac{\partial^2}{\partial x^2}V_2(x,s) = \gamma^2 V_2(x,s) + \alpha V_1(x,s), \tag{8.6}$$

where

$$\gamma = \sqrt{sRC + s^2LC - s^2L_mC_m}, \tag{8.7}$$

$$\alpha = s^2L_mC - sRC_m - s^2LC_m. \tag{8.8}$$

The solution of (8.5) is

$$V_1(x,s) = V_+e^{-\gamma x} + V_-e^{+\gamma x}. \tag{8.9}$$

V_+ and V_- are solved based on the terminal condition of line 1. The general solution of (8.6) is

$$V_2(x,s) = (a_1x + c_1)e^{-\gamma x} + (a_2x + c_2)e^{+\gamma x}. \tag{8.10}$$

a_1 and a_2 are determined by solving the non-homogeneous differential equation,

(8.6). The general solution of a_1 and a_2 is

$$a_1 = -\frac{s^2 L_m C - sRC_m - s^2 LC_m}{2\gamma} V_+, \tag{8.11}$$

$$a_2 = \frac{s^2 L_m C - sRC_m - s^2 LC_m}{2\gamma} V_-. \tag{8.12}$$

c_1 and c_2 are calculated by using the boundary conditions of line 2. Therefore, all of these coefficients are determined based on boundary conditions, permitting the general closed form solutions of $V_1(x,s)$ and $V_2(x,s)$ to be determined.

The time domain solutions of $V_1(x,s)$ and $V_2(x,s)$ can be obtained by using an inverse Laplace transform. However, in many of these cases, a numerical solution results because the inverse Laplace transform of $\frac{1}{1+e^{-2\gamma x}}$ cannot be derived explicitly. In order to determine a closed form analytical expression for use in chip level noise analysis, some approximating assumptions are necessary.

The propagation factor γ, defined in (8.7), is

$$\begin{aligned}\gamma &= \sqrt{sRC + s^2 LC - s^2 L_m C_m} = s\sqrt{LC - L_m C_m}\left(1 + \frac{RC}{s(LC - L_m C_m)}\right)^{\frac{1}{2}} \\ &\approx s\sqrt{LC - L_m C_m}\left(1 + \frac{RC}{2(sLC - L_m C_m)}\right) \qquad \text{where } s(LC - L_m C_m) \geq RC.\end{aligned} \tag{8.13}$$

The assumption of $s(LC - L_m C_m) \geq RC$ is equivalent to $\omega(LC - L_m C_m) \geq RC$ in the frequency domain, *i.e.*, the inductive component exceeds its resistive component which is the condition for the on-chip inductance to be significant [43, 44]. If $s(LC - L_m C_m) = RC$, the error of the approximation made in (8.13) is about 6%. If the driver output impedances of line 1 and line 2 match the line impedance, no reflections will occur at each of the driver ends. V_+ and V_- in (8.9) can be quantified as

$$V_+ = V_{in}(s)/2, \tag{8.14}$$

$$V_- = e^{-2\gamma l} V_{in}(s)/2, \tag{8.15}$$

where l is the length of the transmission line. c_1 and c_2 can be calculated based on V_+ and V_- as well as a_1 and a_2,

$$c_1 = \frac{Z(a_1 + a_2) + sL_m(V_+ - V_-)}{2(R + sL)}, \tag{8.16}$$

$$c_2 = a_1 l e^{-2\gamma l} - a_2 l + c_1 e^{-2\gamma l}. \tag{8.17}$$

By inserting (8.11), (8.12), (8.16), and (8.17) into (8.10), the coupling noise voltage on the quiet line for the matched driver condition is determined.

8.2.1 Coupling noise voltage at the driver end

For the near end coupling noise voltage V_{NE} on the quiet line, *i.e.*, $x = 0$ in (8.10),

$$\frac{V_{NE}(s)}{V_{in}(s)} = -\frac{l}{2} e^{-2\gamma l} \frac{s^2 L_m C - s^2 L C_m - sRC_m}{\gamma} + \frac{1}{8}(1 - e^{-4\gamma l})\left(\frac{sL_m}{R + sL} + \frac{C_m}{C}\right). \tag{8.18}$$

The input is assumed to behave as a fast ramp,

$$V_{in}(t) = \frac{V_{dd}}{\tau_r}[tu(t) - (t - \tau_r)u(t - \tau_r)], \tag{8.19}$$

where τ_r is the rise time of the input signal. The first constraint for τ_r is $\tau_r \leq \tau_0$, where τ_0 is the time of flight delay of the signal through the transmission line, $\tau_0 = l\sqrt{LC}$. This constraint requires that the interconnect inductance not be neglected [44, 45]. The second constraint is from the assumption of $\omega(LC - L_m C_m) \geq RC$. The frequency corresponding to this rise time is $\omega = 2\pi * 0.33/\tau_r = 2.0/\tau_r$ [114]. This requirement becomes

$$\tau_r \leq \frac{2.0(LC - L_m C_m)}{RC}, \tag{8.20}$$

and

$$e^{-2\gamma l} = e^{-2s\tau' - Rl/Z'} \qquad \text{where } \tau' = l\sqrt{LC - L_m C_m} \text{ and } Z' = \sqrt{\frac{L}{C} - \frac{L_m C_m}{C}}. \tag{8.21}$$

Using the approximation of γ in (8.13) and an inverse Laplace transform, the driver end coupling noise voltage $V_{NE}(t)$ in the time domain is

$$\begin{aligned}
V_{NE}(t) &= -\frac{\tau' e^{-\frac{Rl}{Z'}} V_{dd}}{2\tau_r} V_{n1}(t) + \frac{V_{dd}}{8\tau_r} V_{n2}(t), \\
V_{n1}(t) &= \frac{L_m}{L} V_{n3}(t) - \frac{C_m}{C} V_{n4}(t) - \frac{C_m R}{2CL} V_{n5}(t), \\
V_{n3}(t) &= e^{-\frac{t-2\tau'}{2\tau_1}} u(t-2\tau') - e^{-\frac{t-2\tau'-\tau_r}{2\tau_1}} u(t-2\tau'-\tau_r), \\
V_{n4}(t) &= u(t-2\tau') - u(t-2\tau'-\tau_r), \\
V_{n5}(t) &= V_{n8}(t-2\tau'), \\
V_{n2}(t) &= V_{n6}(t) - e^{-\frac{2Rl}{Z'}} V_{n6}(t-4\tau'), \\
V_{n6}(t) &= \frac{L_m}{L}(V_{n7}(t) - V_{n7}(t-\tau_r)) + \frac{C_m}{C} V_{n8}(t), \\
V_{n7}(t) &= \tau_1(1 - e^{-\frac{t}{\tau_1}})u(t), \\
V_{n8}(t) &= tu(t) - (t-\tau_r)u(t-\tau_r),
\end{aligned} \tag{8.22}$$

where

$$\tau_1 = \frac{LC - L_m C_m}{RC}. \tag{8.23}$$

Each term in $V_{n1}(t)$ is due to the first reflection at the receiver end, where the reflection coefficient is one. $V_{n1}(t)$ is the difference between the inductive coupling noise voltage and the capacitive coupling noise voltage. There are two terms in $V_{n2}(t)$, one term occurs at the same time as when the active driver begins to transition and the other term lags by $4\tau'$ and is attenuated by $e^{-\frac{2Rl}{Z'}}$, which is due to the second reflection at the receiver end. $V_{n6}(t)$ is the summation of the

inductive coupling noise voltage and the capacitive coupling noise voltage. The steady state voltage of the driver end coupling noise signal is zero. The time for the driver end coupling noise voltage to reach a steady state voltage is approximately $4\tau' + \tau_r$.

8.2.2 Coupling noise voltage at the receiver end

For the far end noise voltage V_{FE} on the quiet line, where $x = l$ in (8.10),

$$\frac{V_{FE}(s)}{V_{in}(s)} = -\frac{l}{2}e^{-\gamma l}\frac{s^2L_mC - sRC_m - s^2LC_m}{\gamma} + \frac{1}{4}(e^{-\gamma l} - e^{-3\gamma l})(\frac{sL_m}{R+sL} + \frac{C_m}{C}). \tag{8.24}$$

For a fast ramp input signal, the approximation of γ in (8.13) and $V_{in}(s)$ are inserted into (8.24), permitting an inverse Laplace transform to be used to determine the receiver end coupling noise voltage $V_{FE}(t)$ in the time domain:

$$\begin{aligned}
V_{FE}(t) &= -\frac{\tau' e^{-\frac{Rl}{2Z'}}V_{dd}}{2\tau_r}V_{f1}(t) + \frac{V_{dd}}{4\tau_r}V_{f2}(t),\\
V_{f1}(t) &= \frac{L_m}{L}V_{f3}(t) - \frac{C_m}{C}V_{f4}(t) - \frac{C_mR}{2CL}V_{f5}(t),\\
V_{f3}(t) &= e^{-\frac{t-\tau'}{2\tau_1}}u(t-\tau') - e^{-\frac{t-\tau'-\tau_r}{2\tau_1}}u(t-\tau'-\tau_r),\\
V_{f4}(t) &= u(t-\tau') - u(t-\tau'-\tau_1),\\
V_{f5}(t) &= (t-\tau')u(t-\tau') - (t-\tau_1-\tau')u(t-\tau'-\tau_1),\\
V_{f2}(t) &= e^{-\frac{Rl}{2Z'}}V_{f6}(t-\tau') - e^{-\frac{3Rl}{2Z'}}V_{f6}(t-3\tau'),\\
V_{f6}(t) &= \frac{L_m}{L}(V_{f7}(t) - V_{f7}(t-\tau_r)) + \frac{C_m}{C}V_{n8}(t),
\end{aligned} \tag{8.25}$$

and $V_{f7}(t) = V_{n7}(t)$.

$V_{f1}(t)$ represents the difference between the inductive coupling noise voltage and the capacitive coupling noise voltage. The summation of the inductive coupling noise voltage and the capacitive coupling noise voltage is described by $V_{f6}(t)$.

The second term in $V_{f2}(t)$ lags the first term by $2\tau'$ and is also attenuated by $e^{-Rl/Z'}$. The steady state voltage of the receiver end coupling noise voltage is also zero. The time for the receiver end coupling noise voltage to reach a steady state voltage is approximately $3\tau' + \tau_r$.

8.3 Comparison with Simulation

To verify the accuracy of the analytical expressions, (8.22) and (8.25), that describe the coupling noise voltage at both ends of a quiet line, a criterion is defined to measure the error of these closed form approximations. This criterion quantifies the error between the predicted peak noise voltage and the simulated peak noise voltage, permitting the accuracy of these analytical equations to be determined. The criterion is defined as

$$\epsilon_{peak} = |V_p - V_s|/|V_s|, \tag{8.26}$$

where V_p is the value of the peak noise voltage predicted by the analytical expressions, and V_s is the peak noise voltage obtained by a circuit simulator (SPICE).

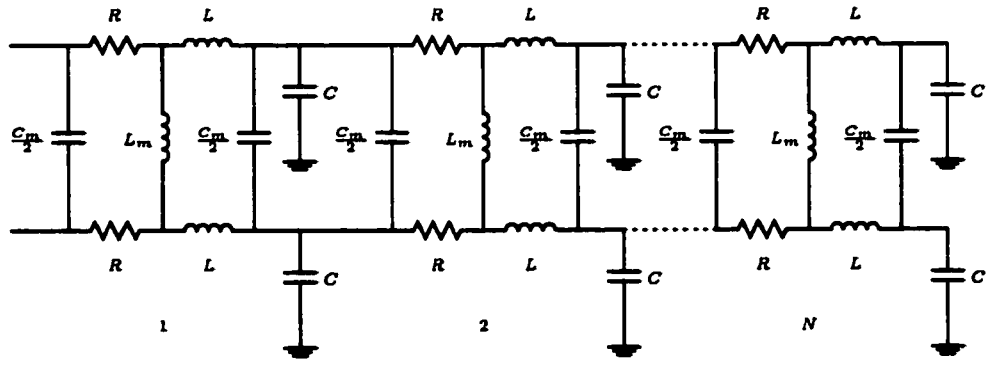


Figure 8.2: The SPICE equivalent circuit of a coupled interconnect

The equivalent circuit used in the SPICE simulation analysis is shown in Figure 8.2, where N sections of coupled RLC subcircuits are used to approximate two coupled lossy transmission lines. A mutual inductor is used to approximate the coupling inductance. A π model is used to model the coupling capacitance. The parameters used in the SPICE simulation are $R = 3\ \Omega/cm$, $C = 1\ pF/cm$, $L = 2\ nH/cm$, $L_m/L = 0.2$, $C_m/C = 0.1$, $l = 2\ cm$, $V_{dd} = 5.0\ V$, $\tau_r = 120\ ps$, and $N = 20$. The value of two linear resistors, which are used to approximate the driver output impedance, is $R_1 = R_2 = \sqrt{L/C} = 44.72\ \Omega$. Both the analytical and simulation results are depicted in Figures 8.3 and 8.4 for the driver end and the receiver end coupling noise voltage, respectively. The error of the peak noise voltage is within 6% at the driver end and less than 1% at the receiver end. The initial condition of the quiet line is assumed to be 0 volts, therefore the NMOS transistor is on and the quiet line is connected to ground. The coupling noise voltage at the driver end is momentarily below ground. If the initial condition of the quiet line is V_{dd} (the PMOS transistor is on and the interconnect is connected through the transistor to the power supply), the coupling noise voltage at the driver end may rise above the power supply voltage V_{dd}.

The analytically derived noise waveform deviates from the simulated waveform at both ends since the phase difference is neglected, but the predicted waveform follows the shape of the simulated coupling noise voltage. The phase difference due to the signal traveling along the interconnect line can be described in the frequency domain. In the time domain, only the numerical solution can predict the effect of the phase difference [111]. This approach, however, requires significant computation time and computer memory. It is typically prohibitive at the system (or chip) level to predict the effects of the phase difference on the coupling noise.

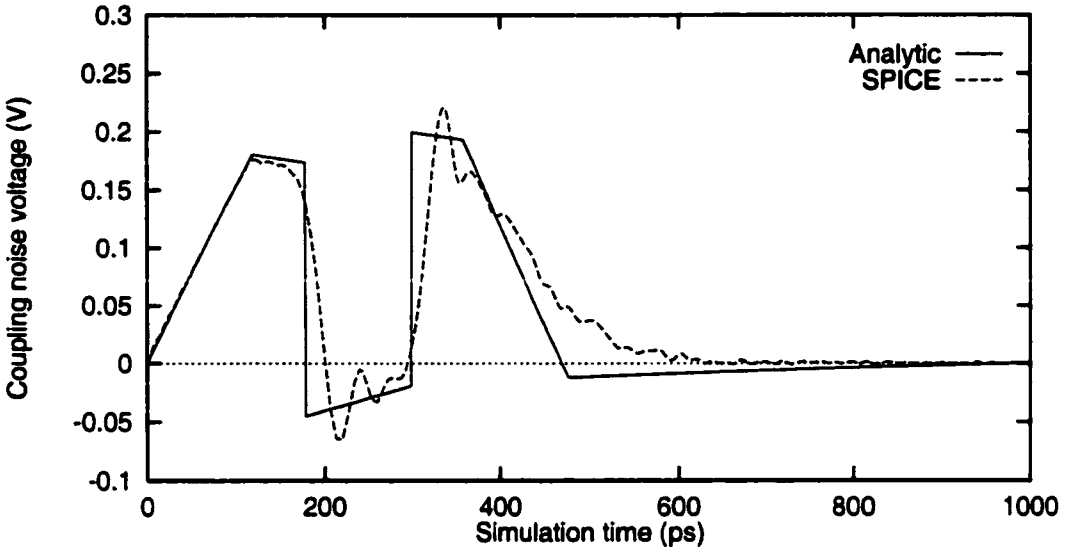


Figure 8.3: Coupling noise voltage at the driver end

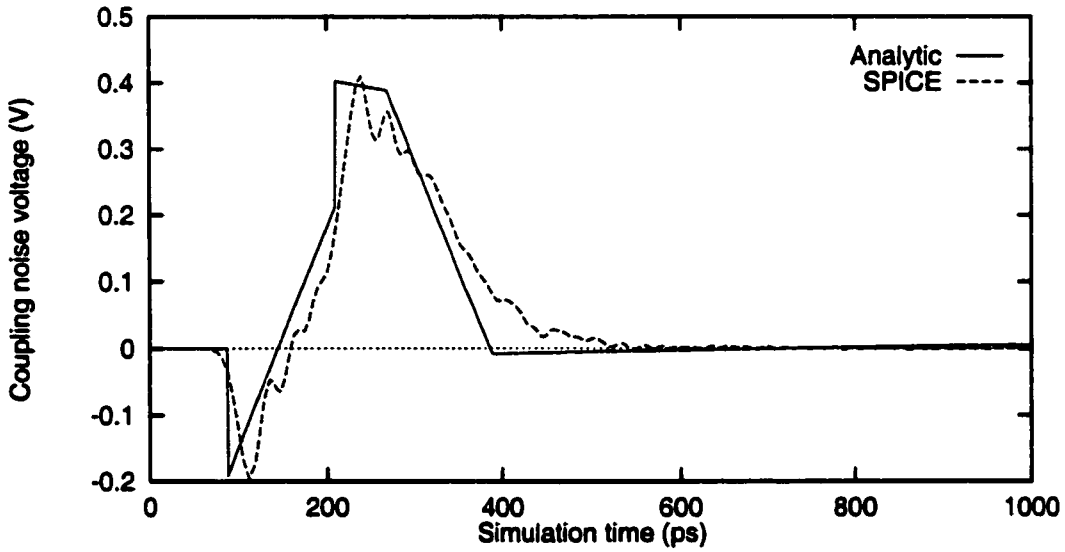


Figure 8.4: Coupling noise voltage at the receiver end

Table 8.1: Analytical expressions characterizing the peak noise voltage on a quiet interconnect line

Near end peak noise voltage

- Condition 1: $2\tau_0 \geq \tau_r$

$$V_1 = \frac{V_{dd}}{8}\left[\frac{L_m}{L}\left(1 - e^{-\frac{\tau_r}{\tau_1}}\right)\tau_1 + \frac{C_m}{C}\tau_r\right] \tag{8.27}$$

$$V_2 = -\frac{1}{2}\tau_0 e^{-\frac{R}{2}l}\frac{V_{dd}}{\tau_r}\left(\frac{L_m}{L} - \frac{C_m}{C}\right) + \frac{V_{dd}}{8}\left[\frac{L_m}{L}\left(e^{-\frac{2\tau_0-\tau_r}{\tau_1}} - e^{-\frac{2\tau_0}{\tau_1}}\right)\tau_1 + \frac{C_m}{C}\tau_r\right] \tag{8.28}$$

$$V_3 = -\frac{1}{2}\tau_0 e^{-\frac{R}{2}l}\frac{V_{dd}}{\tau_r}\left[\frac{L_m}{L}\left(e^{-\frac{\tau_r}{2\tau_1}} - 1\right) - \frac{C_m}{C}\frac{R}{2L}\tau_r\right] + \frac{V_{dd}}{8}\left[\frac{L_m}{L}\left(e^{-\frac{2\tau_0}{\tau_1}} - e^{-\frac{2\tau_0+\tau_r}{\tau_1}}\right)\tau_1 + \frac{C_m}{C}\tau_r\right] \tag{8.29}$$

$$V_{NE,Peak} = \max(|V_1|, |V_2|, |V_3|) \tag{8.30}$$

- Condition 2: $2\tau_0 \leq \tau_r$

$$V_4 = \frac{V_{dd}}{8}\left[\frac{L_m}{L}\left(e^{-\frac{2\tau_0-\tau_r}{\tau_1}} - e^{-\frac{2\tau_0}{\tau_1}}\right)\left(1 - e^{-\frac{\tau_r}{\tau_1}}\right)\tau_1 + \frac{C_m}{C}\tau_r\right] \tag{8.31}$$

$$V_5 = -\frac{1}{2}\tau_0 e^{-\frac{R}{2}l}\frac{V_{dd}}{\tau_r}\left(\frac{L_m}{L}e^{-\frac{\tau_r}{2\tau_1}} - \frac{C_m}{C}\left(1 + \frac{R}{2L}\tau_r\right)\right) + \frac{V_{dd}}{8}\left[\frac{L_m}{L}\left(e^{-\frac{2\tau_0}{\tau_1}} - e^{-\frac{2\tau_0+\tau_r}{\tau_1}}\right)\tau_1 + \frac{C_m}{C}\tau_r\right] \tag{8.32}$$

$$V_6 = -\frac{1}{2}\tau_0 e^{-\frac{R}{2}l}\frac{V_{dd}}{\tau_r}\left[\frac{L_m}{L}\left(e^{-\frac{2\tau_0}{2\tau_1}} - e^{-\frac{\tau_0-\tau_r}{2\tau_1}}\right) - \frac{C_m}{C}\frac{R}{2L}\tau_r\right] + \frac{V_{dd}}{8}\left[\frac{L_m}{L}\left(e^{-\frac{4\tau_0-\tau_r}{\tau_1}} - e^{-\frac{4\tau_0}{\tau_1}}\right)\tau_1 + \frac{C_m}{C}\tau_r\right] \tag{8.33}$$

$$V_{NE,Peak} = \max(|V_4|, |V_5|, |V_6|) \tag{8.34}$$

Far end peak noise voltage

$$V_7 = -\frac{1}{2}\tau_0 e^{-\frac{R}{2}l}\frac{V_{dd}}{\tau_r}\left(\frac{L_m}{L} - \frac{C_m}{C}\right) \tag{8.35}$$

$$V_8 = -\frac{1}{2}\tau_0 e^{-\frac{R}{2}l}\frac{V_{dd}}{\tau_r}\left(\frac{L_m}{L}e^{-\frac{\tau_r}{2\tau_1}} - \frac{C_m}{C} - \frac{C_m}{C}\frac{R}{2L}\tau_r\right) - \frac{C_m}{C}\right) + \frac{1}{4}\frac{V_{dd}}{\tau_r}e^{-\frac{R}{2}l}\left(\frac{L_m}{L}\tau_1\left(1 - e^{-\frac{\tau_r}{\tau_1}}\right) + \frac{C_m}{C}\tau_r\right) \tag{8.36}$$

$$V_{FE,Peak} = \max(|V_7|, |V_8|) \tag{8.37}$$

8.4 Discussion

Inductive coupling and the loosely coupled condition are discussed first in this section based on the compact model developed by Delorme [60]. The accuracy of the analytical equations is also evaluated in this section for different interconnect impedances, driver output impedances, and rise times of the input signal.

8.4.1 Coupled interconnect

Interconnects in CMOS VLSI circuits are multiconductor lines existing on different physical planes. The parasitic capacitance and resistance of the conductor lines can be extracted from the geometric layout [60, 62]. Due to the fast waveforms in high speed CMOS VLSI circuits, particularly if the transition times are comparable to or less than the time of flight delay of the signal through the line, the interconnect parasitic inductance should also be considered in the interconnect model [44, 45, 64] for long, low resistivity interconnect lines.

Adjacent interconnect lines are affected by electrostatic and electromagnetic field lines. Therefore, those lines are capacitively and inductively coupled. The current return path of the parasitic inductance includes both the silicon substrate and neighboring ground lines. The complicated current return path causes inductive coupling to extend across great distances, as illustrated in Figure 8.5.

Any transient signal on line 1 can cause a current change on the V_{ss} line, inducing a voltage change on line 3. Therefore, inductive coupling can occur between line 1 and line 3 despite line 2 being between line 1 and line 3.

The loosely coupled assumption permits the effect of the quiet line voltage on the signal waveform on the active line to be ignored. Both of the capacitive and inductive coupling factors, *i.e.*, C_m/C and L_m/L, are calculated based on different

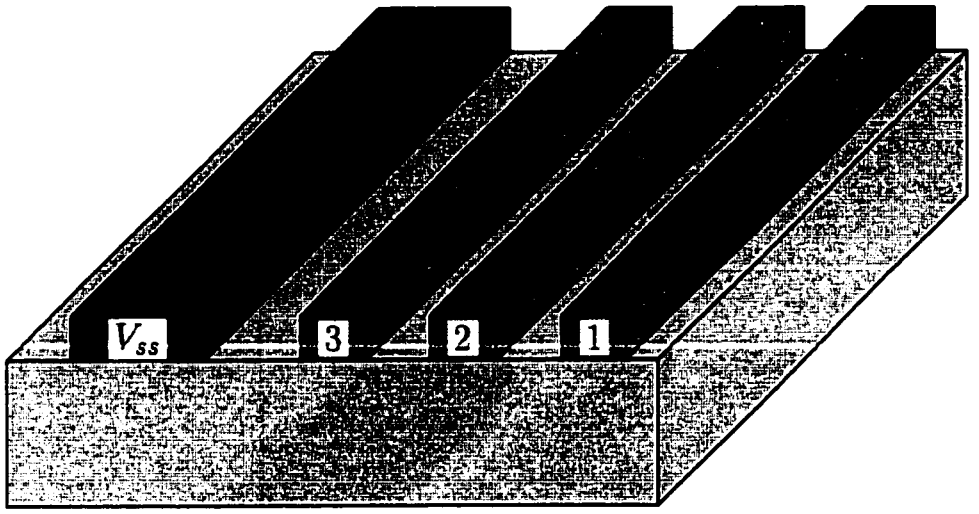


Figure 8.5: Coupled multiple conductor lines

geometric parameters [60]. These results are shown in Figure 8.6. The horizontal axis describes the ratio of the spacing between two interconnect lines over the line width. The coupling factors of a non-overlapping line structure are shown in the first two groups. The third group represents the capacitive coupling factor between two coplanar lines. Each group is composed of three different aspect ratios of the interconnect thickness-to-width, *i.e.*, 0.5 (lower line), 1.0 (middle line), and 1.5 (upper line). The line width of the interconnect is 1.6 μm. The loosely coupled assumption is satisfied for most conditions except for a coplanar line structure with a narrow space and a high thickness-to-width ratio. However, the distance between the high aspect ratio lines is typically greater than the line width in most practical VLSI circuits.

The validity of these analytical expressions are investigated in this section based on certain assumptions. The fast ramp input constraint, *i.e.*, the high frequency assumption, permits the interconnect to be modeled as a low loss transmission line, and the matched load condition at the driver end permits the use

of an inverse Laplace transform to obtain explicit solutions in the time domain. The driver impedance is typically comparable to the line impedance; therefore the on-chip inductance should be considered within the interconnect model [45].

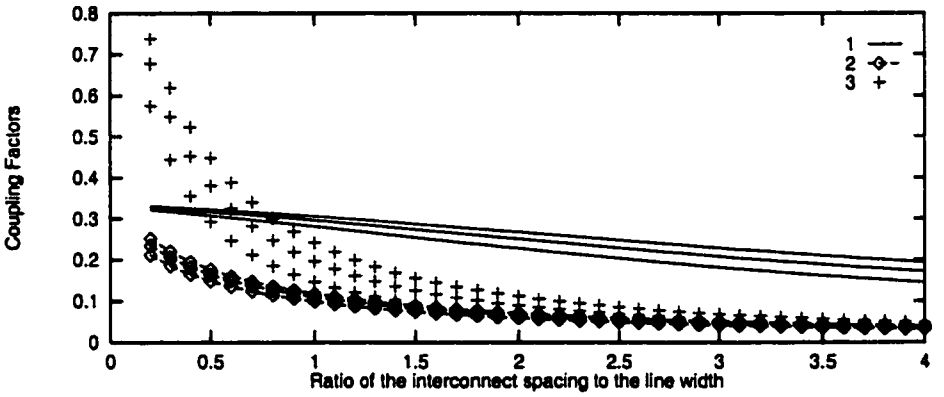


Figure 8.6: Coupling factors. Group 1 is the inductive coupling factor and Group 2 is the capacitive coupling factor for a non-overlapping line structure. Group 3 is the capacitive coupling factor between two coplanar lines.

8.4.2 Low loss or high frequency assumption

The rise time constraint, *i.e.*, $\tau_r < \tau_0$, is the condition that the interconnect inductance must be included in the interconnect model. If $2\tau_l/\tau_r \gg 1$, *i.e.*, $\omega L > R$ – the assumption made in (8.13), the interconnect should be modeled as a low loss transmission line under the high frequency condition. Two different regions of operation are defined for medium and high frequencies: condition 1 – medium frequency: $\tau_l/\tau_r \geq 2$, and condition 2 – high frequency: $\tau_l/\tau_r \geq 4$. The total line resistance (Rl) is varied from 0 to $1.0Z_0$ to test for the low and high loss conditions. The error of the peak noise voltage calculation as compared to SPICE is shown in Figures 8.7 and 8.8 at the driver end and the receiver end, respectively. The horizontal axis is the ratio of Rl/Z_0. The error is within 20% at the driver end and 15% at the receiver end for the worst case, *i.e.*, $Rl/Z_0 = 1.0$.

If the interconnect is modeled as a high loss transmission line ($Rl \approx 1.0Z_0$), these analytical equations accurately predict the peak noise voltage.

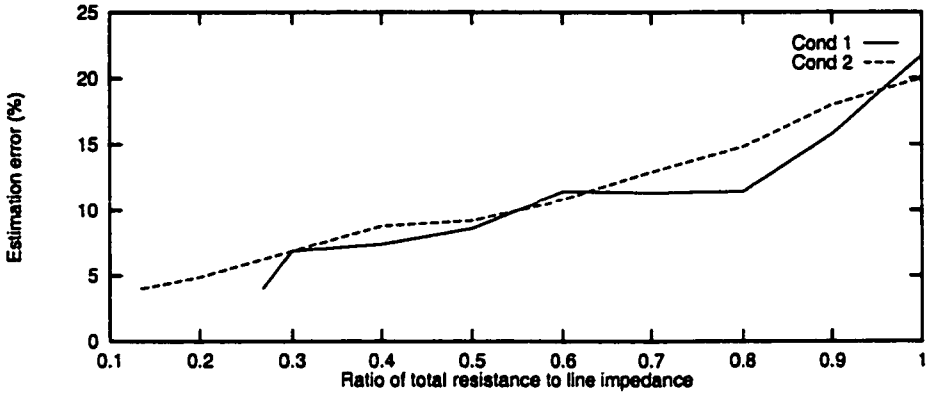


Figure 8.7: The peak noise voltage of different lossy interconnect lines at the driver end. The solid line (Cond 1) is the condition τ_l/τ_r=2, and the dashed line (Cond 2) is the condition τ_l/τ_r=4.

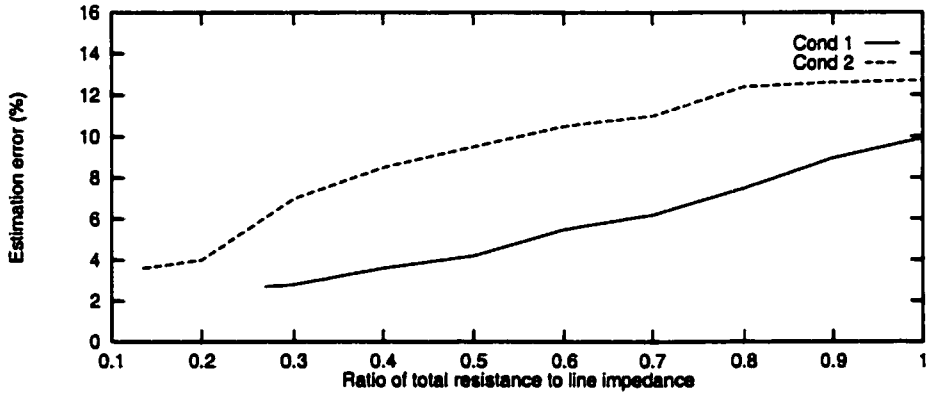


Figure 8.8: The peak noise voltage of different lossy interconnect lines at the receiver end. The solid line (Cond 1) is the condition τ_l/τ_r=2, and the dashed line (Cond 2) is the condition τ_l/τ_r=4.

8.4.3 Output impedance of a CMOS driver stage

A second assumption is that the driver impedance matches the line impedance. The following analysis investigates the coupling noise voltage under the condition

of a varying driver to load impedance ratio in terms of the propagation delay of the driver stage, the relaxation time of the coupling noise voltage, and the peak noise voltage.

Propagation delay versus driver impedance

Before discussing the relationship between the driver impedance and the coupling noise voltage, the propagation delay of the driver stage is investigated with respect to the active driver impedance. The driver impedance in terms of the propagation delay is shown in Figure 8.9. Note that the smaller the driver impedance, the shorter the propagation delay. However, if the driver impedance is less than the interconnect impedance, a negative reflection occurs at the active driver end, and overshoots (the signal rises above the power supply voltage V_{dd}) or undershoots (the signal falls below ground) occur. The overshoot (undershoot) may cause the PN junction of the drain of the PMOS (NMOS) transistor to be forward biased, collecting (injecting) electrons into the substrate, dissipating extra power [18], and delaying the time response. The output voltage of the active driver stage oscillates due to reflections at both ends of the active line before a final steady state voltage is reached.

Relaxation time versus driver impedance

Another effect of a small driver impedance as compared to the line impedance is that the relaxation time, the time required for a signal to reach the steady state voltage of the coupling noise voltage on the quiet line, increases. The relationship between the relaxation time of the coupling noise voltage and the active driver impedance is shown in Figure 8.10. The waveform of the coupling noise voltage

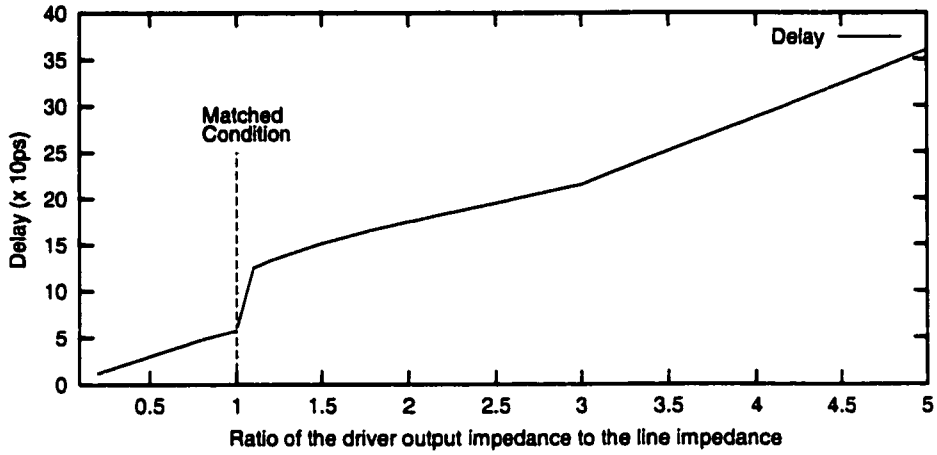


Figure 8.9: Propagation delay of the active CMOS driver stage versus the driver impedance

on the quiet line is strongly dependent on the signal transition occurring on the active line. The shortest relaxation time occurs when the active driver impedance matches the line impedance, where no reflections occur at the driver end on the active line. The relaxation time of the coupling noise voltage increases as the driver impedance deviates from the matched load condition.

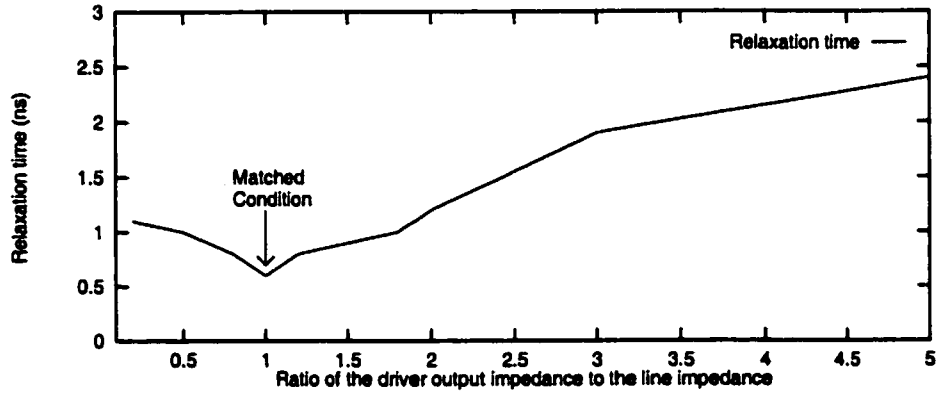


Figure 8.10: Relaxation time of the coupling noise on the quiet line versus the driver impedance. Note that when the ratio is equal to one, the relaxation time is at a minimum.

Power consumption due to the coupling noise voltage

The coupling noise voltage at the driver end of the quiet line causes the NMOS or PMOS transistor to begin operating in the linear region. In order to reduce the propagation delay of the driver stage in high speed CMOS VLSI circuits and decrease the relaxation time of the coupling noise voltage on the quiet line, the driver impedance should be similar in magnitude to the line impedance, permitting the negative reflection at the driver end to be minimized.

Non-matching driver impedance

The peak noise voltage for a variety of driver impedances is shown in Figure 8.11. The peak noise voltage decreases as the driver impedance increases. The maximum error of the peak noise voltage as compared to SPICE simulations is less than 15% at the driver end and within 20% at the receiver end of the quiet line where the driver impedance is in the range of $0.8Z_0$ to $2.0Z_0$. These analytical equations, (8.22) and (8.25), can therefore be used as a first order approximation to predict the coupling noise voltage in high speed CMOS VLSI circuits.

The analytical equations listed in Table 8.1 are used to predict the coupling noise voltage for the interconnect capacitances and inductances presented in [63]. The results are listed in Table 8.2 and the accuracy of these expressions is shown to be within 20% of SPICE. These analytical expressions are also applied to *RLC* impedance commonly used in MCM modules to estimate the peak coupling noise voltage. These results are listed in the last three rows in Table 8.2. The accuracy of these analytical expressions is within 10% as compared with SPICE.

Table 8.2: Comparison of analytic results to SPICE simulation

	Interconnect parameters							Near End Noise			Far End Noise		
$\tau\tau_r$ (ps)	l (cm)	R (Ω/cm)	L (nH/cm)	C (pF/cm)	L_m (nH/cm)	C_m (pF/cm)	Z_{drv} Ω	Sim. (mV)	Ana. (mV)	δ (%)	Sim. (mV)	Ana. (mV)	δ %
120	1.6	35.5	3.19	1.75	0.70	0.22	42.7	164.0	196.0	19.5	358.0	364.0	1.7
120	1.6	35.5	4.49	2.05	1.84	0.137	46.8	220.0	216.0	1.8	483.0	532.0	10.1
120	1.6	35.5	3.64	2.05	1.49	0.137	42.2	204.0	200.0	2.0	382.0	469.0	22.0
120	1.6	35.5	5.07	1.70	2.25	0.255	54.6	280.0	313.0	15.1	549.0	620.0	12.9
120	1.6	35.5	4.30	1.74	1.94	0.242	49.7	266.0	294.0	10.5	506.0	596.0	17.8
120	1.6	15.0	3.19	1.75	0.70	0.22	42.7	203.0	228.0	12.3	435.0	412.0	5.3
120	1.6	15.0	4.49	2.05	1.84	0.137	46.8	438.0	518.0	18.2	818.0	892.0	9.3
120	1.6	15.0	3.64	2.05	1.49	0.137	42.2	392.0	421.0	7.4	718.0	774.0	9.0
120	1.6	15.0	5.07	1.70	2.25	0.255	54.6	378.0	358.0	5.3	681.0	715.0	5.0
120	1.6	15.0	4.30	1.74	1.94	0.242	49.7	338.0	347.0	2.7	646.0	694.0	7.7
100	2.0	10.0	3.19	1.75	0.70	0.22	42.7	225.0	230.0	2.2	466.0	416.0	10.7
100	2.0	10.0	3.19	1.75	0.70	0.22	30.0	205.0	230.0	12.2	479.0	416.0	13.1
100	2.0	10.0	3.19	1.75	0.70	0.22	70.0	275.0	230.0	16.4	410.0	416.0	1.5
100	2.0	10.0	3.19	1.75	0.70	0.22	60.0	261.0	230.0	11.8	429.0	416.0	3.0
150	3.0	2.0	6.0	3.0	1.2	0.3	44.7	0.396	0.378	4.6	0.586	0.575	1.8
150	3.0	2.0	5.0	3.0	1.0	0.6	40.8	0.289	0.271	6.3	0.492	0.471	4.3
150	3.0	5.0	5.0	4.0	1.0	0.8	35.4	0.412	0.389	5.6	0.681	0.649	4.7

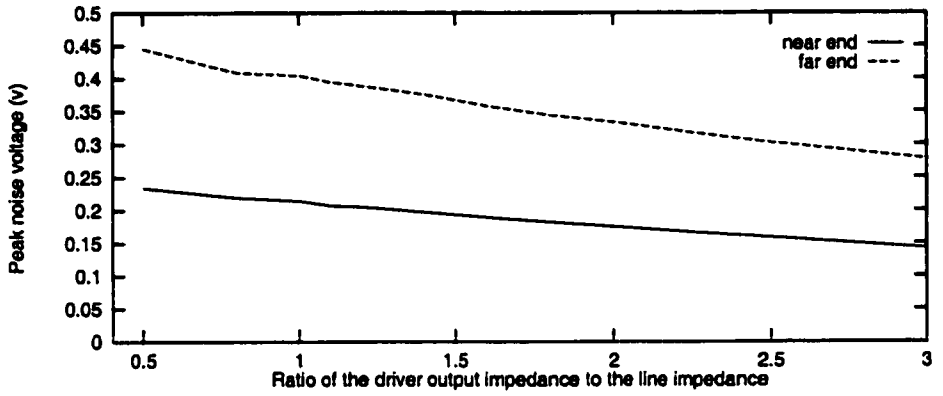


Figure 8.11: Peak noise voltage versus the ratio of the driver impedance to the line impedance

8.5 Summary

Closed from expressions for the peak coupling noise voltage between two neighboring interconnect lines in CMOS VLSI circuits have been presented for different load and waveform conditions. These equations provide an estimate of the coupling noise voltage with an error within 20% at both ends of the quiet line.

In the design of high speed CMOS VLSI circuits, the driver impedance should be comparable to the line impedance in order to reduce the propagation delay of the CMOS driver stage, minimize the reflections at the driver end, and decrease the relaxation time of the coupling noise voltage on the quiet line. The closed form expressions presented in this chapter can be used to estimate the peak value of the coupling noise voltage for lossy interconnect in CMOS VLSI circuits.

Chapter 9

Transient *IR* Voltage Drops in Power Distribution Networks

9.1 Introduction

As modern VLSI technology moves into the very deep submicrometer (VDSM) regime, millions of transistors will be integrated onto a single chip (a system-on-a-chip), operating at frequencies greater than a gigahertz. The die size is expected to increase from $400\,\mathrm{mm}^2$ in 1999 to $1120\,\mathrm{mm}^2$ by 2009 while average on-chip currents will increase from 50 amperes in 1999 to 190 amperes by 2009 [1]. Power distribution networks in high complexity CMOS integrated circuits must be able to provide sufficient current to support an average and peak power demand within all parts of an integrated circuit [17, 18, 20]. The large chip dimensions and on-chip average currents require special design strategies to maintain a constant voltage supply within a power distribution network [24, 25].

The voltage supply is expected to decrease from 1.8 volts in 1999 to 0.9 volts by 2009 [1], reducing the tolerance to voltage changes within a power distribution network. Because of the lossy characteristics of the metal interconnections in CMOS integrated circuits, *IR* voltage drops within a mesh power distribution

structure are no longer negligible [53, 115]. For example, metal 4 in the Alpha 21164 provides the power supply for each element within the entire integrated circuit [19]. The thickness of metal 4 is 1.53 μm and the pitch is 6.0 μm [18]. The average on-chip current is about 15 amperes. The current density is approximately 1.2 mA/μm^2 and the current is about 5.5 mA for a 3.0 μm wide line. For a 9.0 mm long aluminum power line with a resistivity of 4.0 $\mu\Omega$-cm, a parasitic line resistance of 59 Ω results in an average *IR* voltage drop of close to 0.33 volts, which is about 10% of the voltage supply (3.3 volts for the Alpha 21164). Transient *IR* voltage drops which occur during logic transitions in a synchronous CMOS integrated circuit are even greater than these average *IR* voltage drops.

Therefore, significant transient *IR* voltage drops can occur in a synchronous CMOS integrated circuit. These *IR* voltage drops can create delay uncertainty within data paths due to momentary changes in the power supply voltage, making the maximum and minimum propagation delays difficult to estimate, such as needed in clock skew scheduling in the design of high performance clock distribution networks [116]. Additional power planes are an effective design technique to reduce transient *IR* voltage drops, decreasing the parasitic resistance associated with a power distribution network.

An analysis of transient *IR* voltage drops is presented in this chapter. The MOS transistors are characterized by the nth power law I-V model [41]. Analytical expressions describing these transient *IR* voltage drops are developed based on an assumption of a fast ramp input signal. The peak *IR* voltage drops are shown to occur when the input signal completes a transition. The peak value of the transient *IR* voltage drops based on the analytical expression is within 6% as compared to SPICE. Circuit- and layout-level design constraints are also addressed to manage

the maximum *IR* voltage drops. Analytical expressions characterizing the output voltage and propagation delay of a CMOS logic gate are presented for both a capacitive and a resistive-capacitive load, respectively. A propagation delay model based on these analytical expressions is within 5% as compared to SPICE while an estimate without considering transient *IR* voltage drops can reach 20% of SPICE for a 20 Ω power line.

Analytical expressions characterizing transient *IR* voltage drops are developed in Section 9.2. A comparison of the analytical result with SPICE and discussions of circuit- and layout-level constraints are presented in Section 9.3. The effect of transient *IR* voltage drops on the output voltage and propagation delay of a CMOS logic gate is addressed for both a capacitive and a resistive-capacitive load in Section 9.4 followed by some concluding remarks in Section 9.5.

9.2 Modeling of Transient *IR* Voltage Drops

Transient *IR* voltage drops are caused by a large number of logic gates switching close to the same time in a synchronous integrated circuit. For a switching CMOS logic gate, the current through the power lines is assumed to be m times greater than the current through a single CMOS logic gate. This assumption is equivalent to m simultaneously triggered logic gates connected to the same power line.

A circuit schematic of m simultaneously triggered logic gates, each of which is connected to the same power rail, is depicted in Figure 9.1. An analytical expression characterizing the transient *IR* voltage drops on the ground rail is developed in this section for a high-to-low output transition. $R_{V_{ss}}$ is the parasitic resistance of the ground rail. In order to derive an analytical expression characterizing the

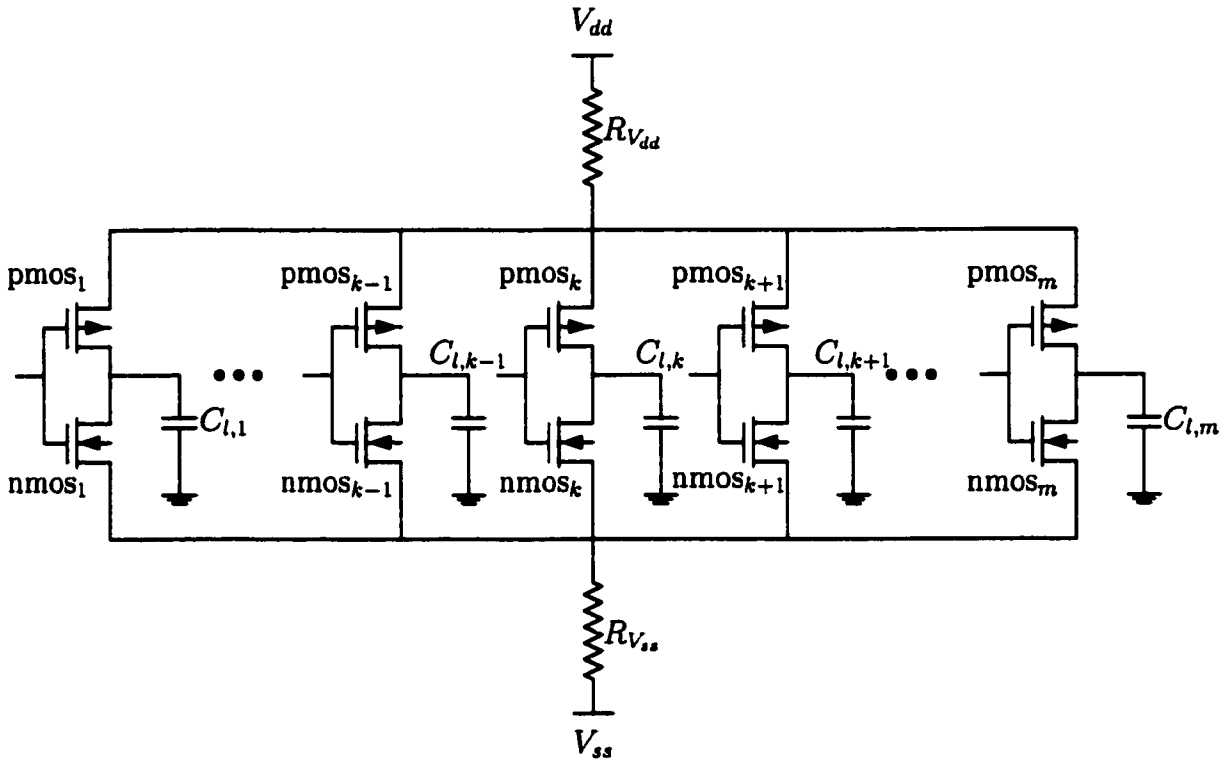


Figure 9.1: Equivalent circuit for analyzing transient *IR* voltage drops

transient *IR* voltage drops on the power rail, the short-circuit current is neglected based on an assumption of a fast ramp input signal [69],

$$V_{in}(t) = \frac{t}{\tau_r} V_{dd} \text{ for } 0 \leq t \leq \tau_r, \tag{9.1}$$

permitting the current through the PMOS transistor to be neglected. The regions of operation of a CMOS inverter during a high-to-low output transition are illustrated in Figure 9.2.

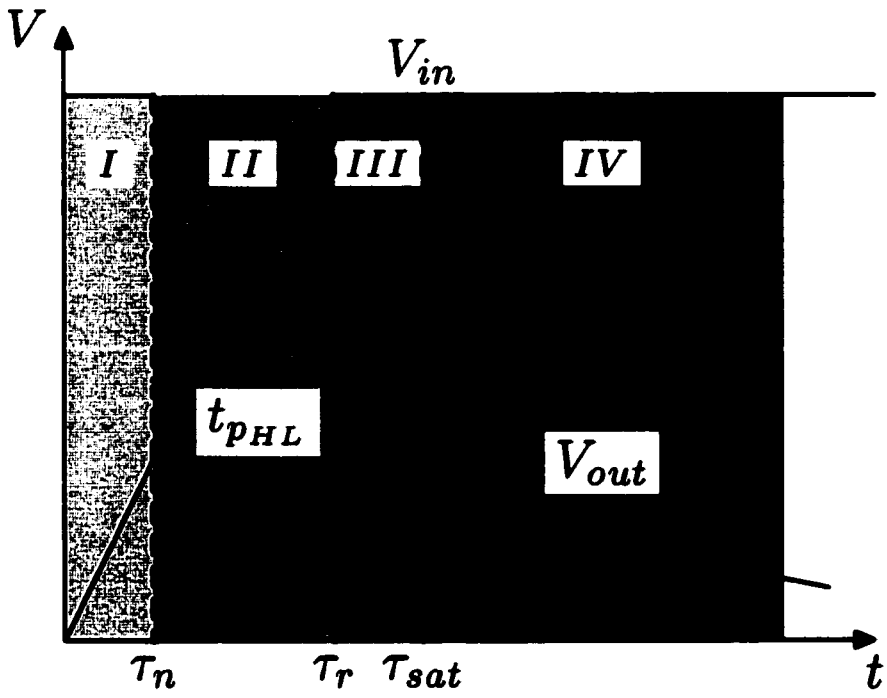


Figure 9.2: Operating regions of a CMOS inverter during the high-to-low output transition.

In region I, the input voltage is less than the threshold voltage of the NMOS transistor. The NMOS transistor is OFF and no current flows to the ground rail; therefore, the transient *IR* voltage drops in region I are zero.

Once the input voltage exceeds the threshold voltage of the NMOS transistor, the NMOS transistor turns ON and is assumed to operate solely in the saturation

region during the input transition. The drain-to-source current in this region is

$$I_{DS} = B_n(V_{in} - V_{TN} - mR_{V_{ss}}I_{DS})^{n_n}. \tag{9.2}$$

Assuming that $mR_{V_{ss}}I_{DS}$ is less than $V_{in} - V_{TN}$, the drain-to-source current can be approximated as

$$I_{DS} = \frac{B_n(V_{in} - V_{TN})^{n_n}}{1 + mR_{V_{ss}}n_nB_n(V_{in} - V_{TN})^{(n_n-1)}}. \tag{9.3}$$

Therefore, the transient IR voltage drops in region II are

$$V_{IR} = mR_{V_{ss}}\frac{B_n(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}}{1 + mR_{V_{ss}}n_nB_n(\frac{t}{\tau_r}V_{dd} - V_{TN})^{(n_n-1)}} \quad \text{for} \quad \tau_n \le t \le \tau_r, \tag{9.4}$$

where $\tau_n = \frac{V_{TN}}{V_{dd}}\tau_r$. Transient IR voltage drops reach the maximum value at $t = \tau_r$,

$$V_{IR,max} = mR_{V_{ss}}\frac{B_n(V_{dd} - V_{TN})^{n_n}}{1 + mR_{V_{ss}}B_n(V_{dd} - V_{TN})^{n_n-1}}. \tag{9.5}$$

The NMOS transistor is assumed to remain saturated when the input transition is completed, which is the behavior modeled by region III in Figure 9.2. The drain-to-source current is a constant, independent of the output voltage. The transient IR voltage drops in this region are the same as $V_{IR,max}$.

After τ_{sat}, the NMOS transistor operates in the linear region. In order to derive a tractable expression, the drain-to-source current is characterized by γ_nV_{DS}, where γ_n is the effective output conductance of the NMOS transistor. The transient IR voltage drops in region IV can be characterized as

$$V_{IR} = V_{IR,max}e^{-\alpha(t-\tau_{sat})}, \tag{9.6}$$

where $\alpha = \frac{\gamma_n}{C_L(1+mR_{V_{ss}}\gamma_n)}$ and C_L is the load capacitance. However, the effective output conductance of an MOS transistor also depends upon the output voltage in the linear region, changing from γ_{nsat} to $2\gamma_{nsat}$ [41]. In order to accurately characterize the transient IR voltage drops in the linear region, a value of γ_n is chosen between γ_{nsat} and $2\gamma_{nsat}$.

9.3 Characteristics of Transient *IR* Voltage Drops

The waveform and peak value of the transient *IR* voltage drops based on the analytical expression (9.5) are compared to SPICE in Section 9.3.1. Circuit- and layout-level design constraints to manage the peak value of the transient *IR* voltage drops are discussed in Sections 9.3.2 and 9.3.3, respectively.

9.3.1 Comparison with SPICE

A comparison of the analytical expression characterizing the waveform of the transient *IR* voltage drops with SPICE is shown in Figure 9.3 for both the V_{ss} and V_{dd} rails. The transient *IR* voltage drops at the V_{ss} rail increase the potential on the V_{ss} rail, while the transient *IR* voltage drops at the V_{dd} rail decrease the potential on the V_{dd} rail, as shown in Figure 9.3. Thus, the overall voltage swing is decreased, degrading system speed. Transient *IR* voltage drops on the power supply rails increase the effective gate voltage required to turn on the MOS transistors ($V_{GS} = V_{TN} + V_{IR}$ for the NMOS transistor). Note that the analytical prediction is quite close to SPICE. The difference is caused by the effective output conductance of the MOS transistors changing from γ_{sat} to $2\gamma_{sat}$ in the linear region [41].

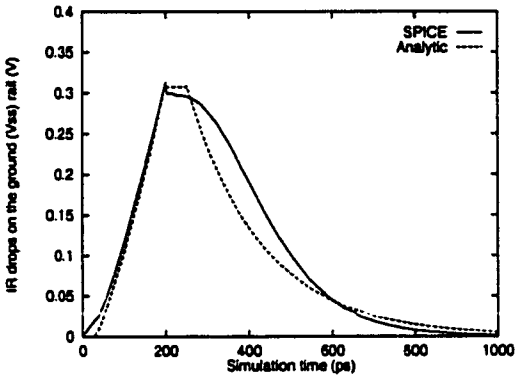
The results of comparing the peak value of the transient *IR* voltage drops with SPICE are listed in Tables 9.1 and 9.2 for both the high-to-low and low-to-high output transitions, respectively, with $w_n = 1.8\,\mu$m, $w_p = 3.6\,\mu$m, and $C_L = 0.1\,$pF. The peak value of the transient *IR* voltage drops based on the analytical expression (9.5) is within 6% as compared to SPICE.

Table 9.1: Comparison of peak IR voltage drops on the V_{ss} rail with SPICE

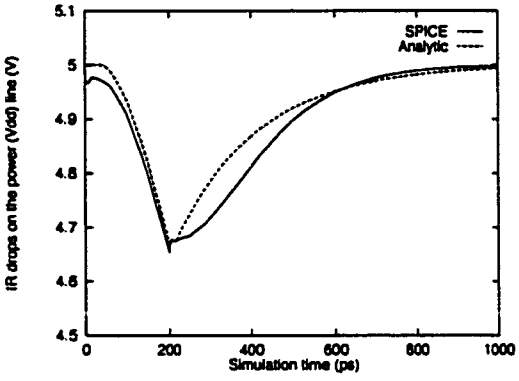
$R_{V_{ss}}$ (Ω)	τ_r (ps)	m	Analytic (V)	SPICE (V)	δ (%)
40.0	100	20	0.971	0.968	0.3
		15	0.786	0.800	1.8
		10	0.569	0.595	4.4
	150	20	0.971	0.945	2.8
		15	0.785	0.780	0.6
		10	0.568	0.578	1.7
	200	20	0.971	0.931	4.3
		15	0.785	0.767	1.0
		10	0.568	0.569	0.2
30.0	100	20	0.785	0.786	0.1
		15	0.626	0.641	2.3
		10	0.445	0.468	4.9
	150	20	0.785	0.766	2.5
		15	0.626	0.624	0.3
		10	0.445	0.455	2.2
	200	20	0.785	0.754	4.1
		15	0.626	0.614	2.0
		10	0.445	0.447	0.4
20.0	100	20	0.568	0.571	0.5
		15	0.445	0.458	2.8
		10	0.311	0.329	5.5
	150	20	0.568	0.556	2.2
		15	0.445	0.445	0.0
		10	0.311	0.319	2.5
	200	20	0.568	0.546	4.0
		15	0.445	0.439	1.4
		10	0.311	0.313	0.6
Maximum error					5.5
Average error					2.0

Table 9.2: Comparison of peak IR voltage drops on the V_{dd} rail with SPICE

$R_{V_{dd}}$ (Ω)	τ_f (ps)	m	Analytic (V)	SPICE (V)	δ (%)
40.0	100	20	4.07	3.95	3.0
		15	4.23	4.13	2.4
		10	4.43	4.35	1.8
	150	20	4.07	3.99	2.0
		15	4.23	4.16	1.7
		10	4.43	4.37	1.4
	200	20	4.07	4.00	1.8
		15	4.23	4.18	1.2
		10	4.43	4.39	0.9
30.0	100	20	4.23	4.13	2.4
		15	4.37	4.29	1.9
		10	4.54	4.48	1.3
	150	20	4.23	4.16	1.7
		15	4.37	4.32	1.2
		10	4.54	4.50	0.9
	200	20	4.23	4.18	1.2
		15	4.37	4.33	0.9
		10	4.54	4.52	0.4
20.0	100	20	4.43	4.35	1.8
		15	4.54	4.48	1.3
		10	4.67	4.63	0.8
	150	20	4.43	4.38	1.1
		15	4.54	4.50	0.9
		10	4.67	4.65	0.4
	200	20	4.43	4.39	0.9
		15	4.54	4.52	0.4
		10	4.67	4.66	0.2
Maximum error					3.0
Average error					1.3



(a) $R_{V_{ss}} = 20.0\,\Omega$, $C_L = 0.1\,\text{pF}$, and $\tau_r = 0.20\,\text{ns}$



(b) $R_{V_{dd}} = 20.0\,\Omega$, $C_L = 0.1\,\text{pF}$, and $\tau_f = 0.20\,\text{ns}$

Figure 9.3: Comparison of the analytical waveform of transient IR voltage drops with SPICE for $w_n = 1.8\,\mu\text{m}$, $w_p = 3.6\,\mu\text{m}$, and $m = 10$.

9.3.2 Circuit-Level Constraints

Assuming the maximum IR voltage drops should be less than a critical voltage V_c, the product of m and $R_{V_{ss}}$ must satisfy

$$mR_{V_{ss}} \leq \frac{V_c}{B_n(V_{dd} - V_{TN})^{n_n} - V_c B_n (V_{dd} - V_{TN})^{n_n - 1}}. \tag{9.7}$$

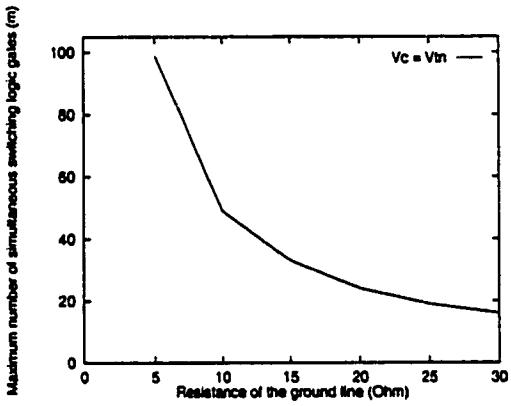
The constraint defined in (9.7) demonstrates that the product of m and $R_{V_{ss}}$ should be less than a constant determined by the right hand side of (9.7). Therefore, the maximum parasitic resistance of a power rail can be determined for a fixed m; the maximum number of simultaneously triggered logic gates can also be determined for a target power rail resistance of $R_{V_{ss}}$ as shown in Figure 9.4(a).

9.3.3 Layout-Level Constraints

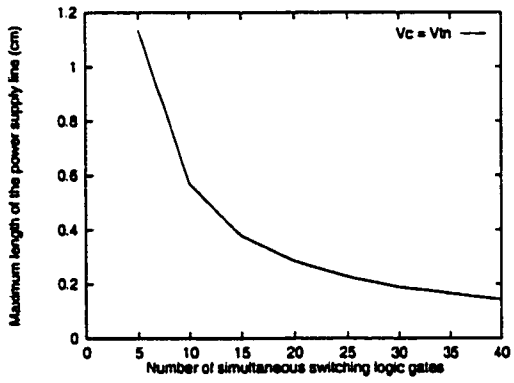
For a metal interconnection, the parasitic resistance can be expressed as

$$R = \rho \frac{l}{wt}, \tag{9.8}$$

where ρ is the resistivity of the material, and l, w, and t are the length, width, and thickness of the metal line, respectively. In practical CMOS integrated circuits, the current density must be less than a limit set by the electromigration constraint [53]. Therefore, for a metal interconnection with a fixed thickness, the minimum width and maximum length of the metal line can be determined by combining (9.7) and (9.8). The maximum length of the power supply rail with $w = 3.0\,\mu$m, $t = 1.53\,\mu$m, and $\rho = 4.0\,\mu\Omega$-cm is shown in Figure 9.4(b).



(a) Maximum number of simultaneously switching logic gates versus the ground line resistance.



(b) Maximum length of the power supply rail versus the number of simultaneously switching logic gates with $w = 3.0\,\mu$m, $t = 1.53\,\mu$m, and $\rho = 4.0\,\mu\Omega$-cm.

Figure 9.4: Maximum number of simultaneously switching logic gates and maximum length of the power supply rail for $V_c = V_{TN}$.

Both (9.7) and (9.8) provide design guidelines for managing the transient *IR* voltage drops within a power distribution network. The use of additional power planes is an effective design technique to reduce the peak value of the transient *IR* voltage drops, significantly reducing the parasitic resistance associated with a power distribution network.

9.4 Output voltage and Propagation Delay

The effect of transient *IR* voltage drops on the output voltage and propagation delay of a CMOS logic gate is discussed in this section. Analytical expressions characterizing the output voltage waveform of a CMOS logic gate are developed for both a capacitive and a resistive-capacitive load in Sections 9.4.1 and 9.4.2, respectively. The propagation delay of a CMOS logic gate based on these analytical expressions is also compared with SPICE.

9.4.1 Capacitive Load

Analytical expressions characterizing the output voltage of a CMOS logic gate driving a capacitive load are listed in Table 9.3 based on an assumption of a fast ramp input signal. τ_{sat} is the time when the NMOS transistor starts to operate in the linear region and is determined from (9.10). The analytical results are compared to both SPICE and the analytical prediction without considering *IR* voltage drops in Figure 9.5. Note that transient *IR* voltage drops affect the propagation delay of a CMOS logic gate. Therefore, the delay uncertainty caused by transient *IR* voltage drops should be included when analyzing the timing of critical data paths [116].

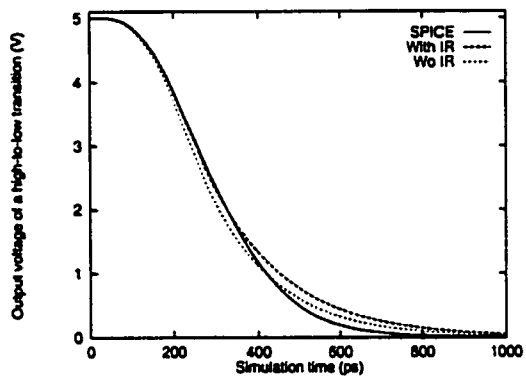
The drain-to-source saturation voltage is typically greater than $0.5V_{dd}$, therefore, the high-to-low propagation delay of a CMOS logic gate can be expressed as

$$t_{P_{HL}} = \frac{C_L(1+mR_{V_{ss}}\gamma_n)}{\gamma_n} ln \frac{2(V_{sat}+V_{IR,max})}{V_{dd}} + \tau_{sat} - \frac{\tau_r}{2}. \qquad (9.12)$$

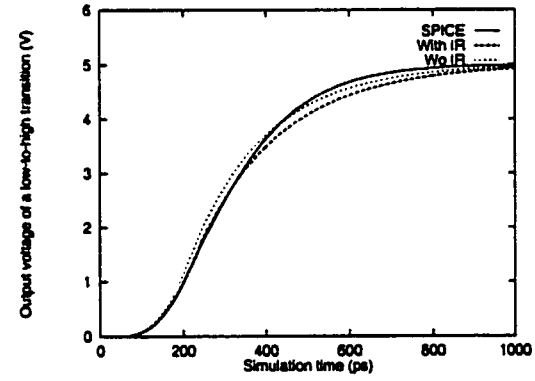
The error of the propagation delay model of a CMOS logic gate without considering transient *IR* voltage drops is illustrated in Figure 9.6. A comparison of

Table 9.3: Analytical expressions characterizing the output voltage with IR voltage drops for a capacitive load

Region	Analytical expressions
$[\tau_n, \tau_r]$	$V_o = V_{dd} - \frac{\tau_r B_n}{C_L(n_n+1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{(n_n+1)} + \frac{mR_{V_{ss}}B_n^2\tau_r}{2C_L V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{2n_n}$ (9.9)
$[\tau_r, \tau_{sat}]$	$V_o = V_o(\tau_r) - \frac{B_n(V_{dd} - V_{TN})^{n_n}(t-\tau_r)}{C_L(1 + mR_{V_{ss}}nB_n(V_{dd} - V_{TN})^{(n_n-1)})}$ (9.10)
$t \geq \tau_{sat}$	$V_o = (V_{sat} + V_{IR,max})e^{-\frac{\gamma_n}{C_L(1+mR_{V_{ss}}\gamma_n)}(t-\tau_{sat})}$ (9.11)



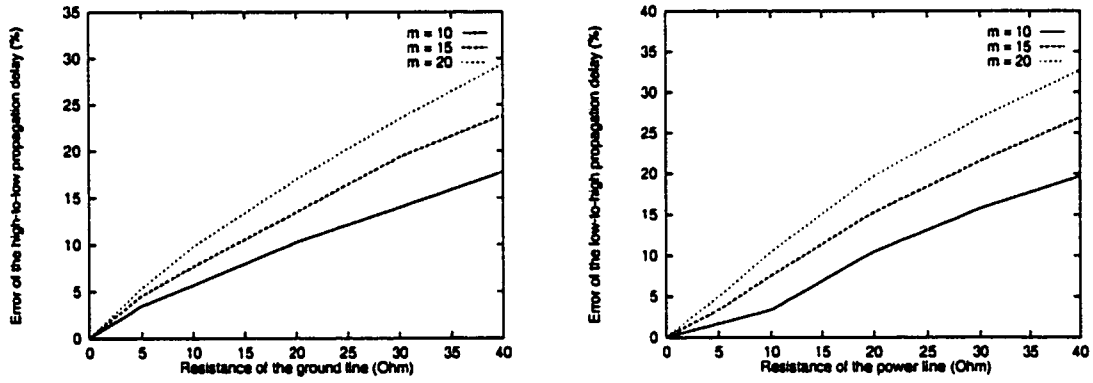
(a) $R_{V_{ss}} = 20.0\,\Omega$, $C_L = 0.1\,\text{pF}$, and $\tau_r = 0.20\,\text{ns}$



(b) $R_{V_{dd}} = 20.0\,\Omega$, $C_L = 0.1\,\text{pF}$, and $\tau_r = 0.20\,\text{ns}$

Figure 9.5: Comparison of the analytical output voltage with SPICE, $w_n = 1.8\,\mu\text{m}$, $w_p = 3.6\,\mu\text{m}$, and $m = 10$.

the propagation delay based on (9.12) with both SPICE and an estimate without considering transient *IR* voltage drops is listed in Tables 9.4 and 9.5 for the high-to-low and low-to-high output transitions, respectively. Note that the maximum error of the proposed delay model is within 3% of SPICE as compared to 20% when transient *IR* voltage drops are not considered (for a 20 Ω power line which is equivalent to a resistance of a 0.23 cm long power line with $w = 3.0\,\mu$m, $t = 1.53\,\mu$m, and $\rho = 4.0\,\mu\Omega$-cm).



(a) Error of high-to-low propagation delay

(b) Error of low-to-high propagation delay

Figure 9.6: Error of the propagation delay model of a CMOS logic gate without considering transient *IR* voltage drops with $\tau_r = 150$ ps, $w_n = 1.8\,\mu$m, and $w_p = 3.6\,\mu$m.

9.4.2 Resistive-Capacitive Load

In this discussion, the interconnect is characterized by a lumped resistive-capacitive model. R_L is the load resistance of the interconnect. Analytical expressions describing the output voltage waveform of a CMOS logic gate driving a resistive-capacitive load are depicted in Table 9.6 based on the same assumption

Table 9.4: High-to-low propagation delay with *IR* voltage drops for a capacitive load

Condition			SPICE	Analytic			
$R_{V_{ss}}$ (Ω)	τ_r (ps)	m	(ps)	Wo IR (ps)	δ (%)	Wi IR (ps)	δ (%)
40.0	100	20	228	160	29.8	231	1.3
		15	212	160	24.5	209	1.4
		10	196	160	18.4	191	2.6
	150	20	235	166	29.4	239	1.7
		15	218	166	23.9	216	0.9
		10	202	166	17.8	198	2.0
	200	20	240	172	28.3	248	3.3
		15	225	172	23.6	223	0.9
		10	208	172	17.3	203	2.4
30.0	100	20	212	160	24.5	209	1.4
		15	200	160	20.0	196	2.0
		10	187	160	14.4	182	2.7
	150	20	217	166	23.5	216	0.5
		15	206	166	19.4	202	2.0
		10	193	166	14.0	189	2.1
	200	20	223	172	22.9	223	0.0
		15	211	172	18.5	208	1.4
		10	199	172	13.6	196	1.5
20.0	100	20	194	160	17.5	190	2.1
		15	187	160	14.4	183	2.1
		10	178	160	10.1	175	1.7
	150	20	200	166	17.0	197	1.5
		15	192	166	13.5	189	1.6
		10	185	166	10.3	181	2.2
	200	20	206	172	16.5	203	1.5
		15	200	172	14.0	196	2.0
		10	190	172	10.5	187	1.6
Maximum error				29.8		3.3	
Average error				20.9		1.0	

Table 9.5: Low-to-high propagation delay with *IR* voltage drops for a capacitive load

Condition			SPICE	Analytic			
$R_{V_{dd}}$ (Ω)	τ_f (ps)	m	(ps)	Wo IR (ps)	δ (%)	Wi IR (ps)	δ (%)
40.0	100	20	246	162	34.1	245	0.4
		15	225	162	28.0	222	1.3
		10	204	162	20.6	201	1.5
	150	20	254	171	32.7	257	1.2
		15	234	171	26.9	233	0.4
		10	213	171	19.7	211	0.9
	200	20	263	181	31.2	269	2.3
		15	243	181	25.5	244	0.4
		10	222	181	18.5	221	0.5
30.0	100	20	225	162	28.0	222	1.3
		15	209	162	22.5	206	1.4
		10	193	162	16.1	191	1.0
	150	20	234	171	26.9	233	0.4
		15	218	171	21.6	216	0.9
		10	203	171	15.8	200	1.5
	200	20	242	181	25.2	244	0.8
		15	227	181	20.3	226	0.4
		10	211	181	14.2	210	0.5
20.0	100	20	203	162	20.2	201	1.0
		15	193	162	16.1	191	1.0
		10	182	162	11.0	181	0.5
	150	20	213	171	19.7	211	0.9
		15	202	171	15.3	200	1.0
		10	191	171	10.5	190	0.5
	200	20	221	181	18.1	221	0.0
		15	211	181	14.2	210	0.5
		10	200	181	9.5	200	0.0
Maximum error				34.1		2.3	
Average error				23.4		1.2	

made in section 9.4.1 while τ_{sat} is determined by (9.15) in Table 9.6. If the drain-to-source saturation voltage is greater than $0.5V_{dd}$, the high-to-low propagation delay of a CMOS logic gate is

$$t_{P_{HL}} = \frac{C_L(1 + mR_{V_{ss}}\gamma_n + R_L\gamma_n)}{\gamma_n} ln \frac{2(V_{sat} + V_{IR,max})}{V_{dd}} + \tau_{sat} - \frac{\tau_r}{2}. \qquad (9.13)$$

A comparison of the propagation delay based on (9.13) with both SPICE and an estimate without considering transient IR voltage drops is listed in Tables 9.7 and 9.8 for the high-to-low and low-to-high output transitions, respectively. Note that the maximum error of the proposed delay model is within 3% of SPICE as compared to about 23% for $\tau_f = 100$ ps and $m = 20$ when transient IR voltage drops are not considered (assuming a 20 Ω power line which is equivalent to a resistance of a 0.23 cm long power line with $w = 3.0\,\mu$m, $t = 1.53\,\mu$m, and $\rho = 4.0\,\mu\Omega$-cm).

Table 9.6: Analytical expressions characterizing the output voltage with IR voltage drops for a resistive-capacitive load

Region	Analytical expressions
$[\tau_n, \tau_r]$	$V_o = V_{dd} - \frac{\tau_r B_n (\frac{t}{\tau_r} V_{dd} - V_{TN})^{(n_n+1)}}{C_L(n_n+1)V_{dd}} + \frac{mR_{V_{ss}} B_n^2 \tau_r}{2C_L V_{dd}} (\frac{t}{\tau_r} V_{dd} - V_{TN})^{2n_n}$ $-R_L \left[B_n (\frac{t}{\tau_r} V_{dd} - V_{TN})^{n_n} - mR_{V_{ss}} n_n B_n^2 (\frac{t}{\tau_r} V_{dd} - V_{TN})^{(2n_n-1)} \right]$ (9.14)
$[\tau_r, \tau_{sat}]$	$V_o = V_o(\tau_r) - \frac{B_n(V_{dd} - V_{TN})^{n_n}}{C_L(1 + mR_{V_{ss}} n B_n (V_{dd} - V_{TN})^{(n_n-1)})} (t - \tau_r)$ (9.15)
$t \geq \tau_{sat}$	$V_o = (V_{sat} + V_{IR,max}) e^{-\frac{\gamma_n}{C_L(1+mR_{V_{ss}}\gamma_n + R_L\gamma_n)}(t-\tau_{sat})}$ (9.16)

Table 9.7: High-to-low propagation delay with *IR* voltage drops for a resistive-capacitive load

Condition			SPICE	Analytic			
$R_{V_{ss}}$ (Ω)	τ_r (ps)	m	(ps)	Wo IR (ps)	δ (%)	Wi IR (ps)	δ (%)
40.0	100	20	212	141	33.5	211	0.4
		15	196	141	28.1	192	2.0
		10	179	141	21.2	175	2.2
	150	20	217	148	31.8	219	0.9
		15	201	148	26.4	200	0.5
		10	184	148	19.6	182	1.1
	200	20	223	154	30.9	227	1.8
		15	207	154	25.6	207	0.0
		10	191	154	19.4	188	1.6
30.0	100	20	194	141	27.3	192	1.0
		15	182	141	22.5	179	1.6
		10	170	141	17.1	167	1.8
	150	20	200	148	26.0	200	0.0
		15	188	148	21.3	186	1.1
		10	175	148	15.4	173	1.1
	200	20	207	154	25.6	207	0.0
		15	194	154	20.6	193	0.5
		10	181	154	14.9	179	1.1
20.0	100	20	178	141	20.8	175	1.7
		15	169	141	16.6	167	1.3
		10	160	141	11.8	158	1.3
	150	20	183	148	19.1	182	0.5
		15	175	148	15.4	173	1.1
		10	166	148	10.8	165	0.6
	200	20	188	154	18.1	188	0.0
		15	180	154	14.4	179	0.6
		10	172	154	10.5	171	0.6
Maximum error				33.5		2.2	
Average error				17.8		1.8	

Table 9.8: Low-to-high propagation delay with *IR* voltage drops for a resistive-capacitive load

Condition			SPICE	Analytic			
$R_{V_{dd}}$ (Ω)	τ_f (ps)	m	(ps)	Wo IR (ps)	δ (%)	Wi IR (ps)	δ (%)
40.0	100	20	232	144	37.9	231	0.4
		15	210	144	31.4	206	1.9
		10	188	144	23.4	184	2.1
	150	20	240	154	35.8	243	1.3
		15	219	154	29.6	217	0.9
		10	197	154	21.8	194	1.5
	200	20	250	163	34.8	256	2.4
		15	227	163	28.2	228	0.4
		10	206	163	20.9	204	1.0
30.0	100	20	210	144	31.4	206	1.9
		15	194	144	25.8	189	2.6
		10	177	144	18.6	174	1.7
	150	20	219	154	29.7	217	0.9
		15	203	154	24.1	200	1.5
		10	186	154	17.2	184	1.1
	200	20	227	163	28.2	228	0.4
		15	211	163	22.7	210	0.5
		10	195	163	16.4	193	1.0
20.0	100	20	188	144	23.4	184	2.1
		15	177	144	18.6	174	1.7
		10	166	144	13.3	164	1.2
	150	20	197	154	21.8	194	1.5
		15	186	154	17.2	184	1.1
		10	175	154	12.0	174	0.6
	200	20	206	163	20.9	204	1.0
		15	195	163	16.4	193	1.0
		10	184	163	11.4	183	0.5
Maximum error				37.9		2.4	
Average error				17.8		1.3	

9.5 Summary

Analytical delay and design constraint expressions characterizing transient *IR* voltage drops are presented in this chapter. The peak *IR* voltage drops occur when the input signal completes a transition (for a fast ramp input signal). The peak value of the transient *IR* voltage drops based on the analytical expression is within 6% as compared to SPICE. Analytical expressions characterizing the output voltage and propagation delay of a CMOS logic gate are also presented for a capacitive and a resistive-capacitive load, respectively. The propagation delay model based on these analytical expressions is within 5% of SPICE while the delay model without considering *IR* voltage drops can reach 20% of SPICE for a 20 Ω power line. Circuit- and layout-level design constraints are also addressed to manage the maximum value of the transient *IR* voltage drops, providing guidelines for the design of power distribution networks. Additional power planes are one effective design technique to reduce transient *IR* voltage drops, significantly reducing the parasitic resistance associated with a power distribution network.

Chapter 10

On-Chip Simultaneous Switching Noise in Power Distribution Networks

10.1 Introduction

The trend of next generation integrated circuit (IC) technology is towards higher speeds and densities. The total capacitive load associated with the internal circuitry is therefore increasing in both current and next generation VLSI circuits [17–19]. As the operating frequency increases, the average on-chip current required to charge (and discharge) these capacitances also increases, while the time during which the current being switched decreases. Therefore, a large change in the total on-chip current occurs within a short period of time.

The primary sources of the current surges are the I/O drivers and the internal logic circuitry, particularly those gates that switch close in time to the clock edges. Because of the self-inductance of the off-chip bonding wires and the on-chip parasitic inductance inherent to the power supply rails, the fast current surges result in voltage fluctuations in the power distribution network [117], which is called simultaneous switching noise or delta-I noise.

Most existing research on simultaneous switching noise has concentrated on the transient power noise caused by the current through the inductive bonding wires at the I/O drivers [118–122]. However, simultaneous switching noise originating from the internal circuitry is becoming an important issue in the design of very deep submicrometer (VDSM) high performance microprocessors [19, 25]. This increased importance can be attributed to fast clock rates, large on-chip switching activities, and large on-chip current, all of which are increasingly common characteristics of a VDSM synchronous integrated circuit.

For example, at gigahertz operating frequencies and high integration densities, power dissipation densities are expected to approach $20\,\mathrm{W/cm^2}$ [1, 7], a power density limit for an air-cooled packaged device. Such a power density is equivalent to 16.67 amperes of current for a 1.2 V power supply in a 0.1 μm CMOS technology. Assuming that the current is uniformly distributed along a 1 cm wide and 1 μm thick Al-Cu interconnect plane, the average current density is approximately $1.67\,\mathrm{mA}/\mu\mathrm{m}^2$. For a standard mesh structured power distribution network, the current density is even greater than $1.67\,\mathrm{mA}/\mu\mathrm{m}^2$. For a 1 mm long power buss line with a parasitic inductance of 2 nH/cm [123], if the edge rate of the current signal is on the order of an overly conservative estimate of nanosecond, the amplitude of the simultaneous switching (or $L\,di/dt$) noise is approximately 0.35 volts. This peak noise is not insignificant in VDSM CMOS integrated circuits.

Therefore, on-chip simultaneous switching noise has become an important issue in VDSM integrated circuits. On-chip simultaneous switching noise affects the signal delay, creating delay uncertainty since the power supply level temporally changes the local drive current [124]. Furthermore, logic malfunctions may be created and excess power may be dissipated due to faulty switching if the power

supply fluctuations are sufficiently large [67, 116]. On-chip simultaneous switching noise must therefore be controlled or minimized in high performance integrated circuits.

An analytical expression characterizing the on-chip SSN voltage is presented here based on a lumped *RLC* model characterizing the on-chip power supply rails rather other a single inductor to model a bonding wire. The MOS transistors are characterized by the nth power law model [41], which is a more accurate device model than the Shichman-Hodges model for short-channel devices [46]. The SSN voltage predicted by the analytical expression is compared to SPICE. The waveform describing the SSN voltage is quite close to the waveform obtained from SPICE simulation. The peak value of the SSN is within 10% of SPICE.

Circuit-level design constraints, such as the number of simultaneously switching logic gates connected to the same power supply rail, the drive current of the logic gates, the input transition time, and the magnitude of the power supply are discussed to manage the peak value of the SSN. For a specific parasitic *RLC* impedance of the power supply rails, the analytical expressions presented here provide guidelines for designing the on-chip power distribution network.

Analytical expressions describing the output voltage waveform of a CMOS logic gate considering the effect of on-chip simultaneous switching noise are also developed. The output voltage waveform based on the analytical expressions is quite close to SPICE. For a capacitive load, the maximum error of the propagation delay model based on the analytical expressions is within 5% of SPICE, as compared to close to 16% of the estimate if on-chip simultaneous switching noise is not considered. The average improvement in accuracy is about 8% as compared to SPICE. For a resistive-capacitive load, the estimated propagation delay based

on the analytical expressions is within 5% of SPICE, while the error of the model which does not consider on-chip simultaneous switching noise can reach 18% of SPICE with an average improvement in accuracy of 10% as compared to SPICE.

An analytical expression of the on-chip simultaneous switching noise voltage is described in Section 10.2. A discussion of the dependence of the on-chip simultaneous switching noise voltage on the load capacitance, and related circuit- and layout-level constraints are presented in Section 10.3. Analytical expressions characterizing the output voltage of a CMOS logic gate for both a capacitive and a resistive-capacitive load are derived in Section 10.4 considering the effect of on-chip simultaneous switching noise, while the output voltage and propagation delay based on these analytical expressions are also compared to SPICE. Some concluding remarks are addressed in Section 10.5.

10.2 Simultaneous Switching Noise Voltage

The power supply in high complexity CMOS circuits should provide sufficient current to support the average and peak power demand within all parts of an integrated circuit. An inductive, capacitive, and resistive model is used in this section to characterize the power supply rails when a transient current is generated by simultaneous switching of the on-chip registers and logic gates within a synchronous CMOS integrated circuit. The short-channel MOS transistors are modeled as nonlinear devices and characterized by the nth power law model, which is more accurate than the alpha power law model in both the linear region and the saturation region [124].

A CMOS logic gate in this discussion is modeled as a CMOS inverter. The power supply rail is characterized by a lumped *RLC* model. The input signal is

assumed to be a fast ramp. The equivalent circuit depicted in Figure 10.1 is used to characterize the simultaneous switching noise voltage on the power supply rails.

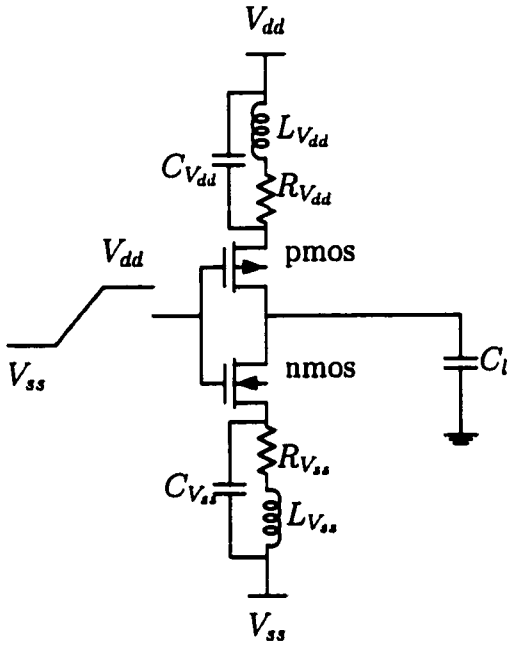


Figure 10.1: An equivalent circuit for analyzing the simultaneous switching noise of an on-chip CMOS inverter.

The current through the PMOS transistor with a rising input signal, *i.e.*, the short-circuit current, is neglected in this discussion when determining the simultaneous switching noise voltage on a ground rail based on the assumption of a fast ramp input signal [69]. The equivalent circuit therefore simplifies to the circuit shown in Figure 10.2. $L_{V_{ss}}$, $C_{V_{ss}}$, and $R_{V_{ss}}$ are the parasitic inductance, capacitance, and resistance of the ground rail, respectively. The input signal is

$$V_{in} = \frac{t}{\tau_r} V_{dd} \text{ for } 0 \leq t \leq \tau_r. \tag{10.1}$$

After the input voltage reaches V_{TN}, the NMOS transistor turns ON and begins to operate in the saturation region. It is assumed that the NMOS transistor remains in the saturation region before the input signal transition is completed.

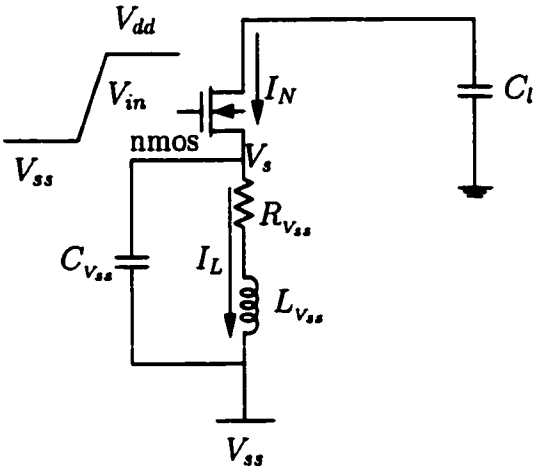


Figure 10.2: Simultaneous switching noise within a ground rail.

The current through the NMOS transistor (I_N), the parasitic inductance (I_L), and the simultaneous switching noise voltage (V_s) are given, respectively, as

$$I_N = B_n(V_{in} - V_{TN} - V_s)^n, \tag{10.2}$$

$$V_s = R_{V_{ss}} I_L + L_{V_{ss}} \frac{dI_L}{dt}, \tag{10.3}$$

$$I_L = I_N - C_{V_{ss}} \frac{dV_s}{dt}. \tag{10.4}$$

Assuming that the magnitude of V_s is small as compared to $V_{in} - V_{TN}$, I_N can be approximated as

$$I_N \approx B_n(V_{in} - V_{TN})^n - \frac{dI_N}{dV_{GS}} V_s. \tag{10.5}$$

Rewriting (10.5),

$$f_1 = \frac{dI_N}{dV_{GS}} = nB_n(V_{in} - V_{TN} - V_s)^{n-1}. \tag{10.6}$$

f_1 is a function of V_{GS}, *i.e.*, V_{in} for the case of an inverter. In order to simplify the derivation, f_1 is approximated using V_{in} equal to 0.5 V_{dd}.

Combining (10.4), (10.5), and (10.6),

$$L_{V_{ss}}C_{V_{ss}}\frac{d^2V_s}{dt^2}+(R_{V_{ss}}C_{V_{ss}}+L_{V_{ss}}f_1)\frac{dV_s}{dt}+(R_{V_{ss}}f_1+1)V_s=$$
$$R_{V_{ss}}B_n(V_{in}-V_{TN})^n+L_{V_{ss}}\frac{d}{dt}[B_n(V_{in}-V_{TN})^n]. \tag{10.7}$$

The first term on the left hand side of (10.7) is neglected since the remaining two terms on the left hand side of (10.7) dominate the expression.

$$(R_{V_{ss}}C_{V_{ss}}+L_{V_{ss}}f_1)\frac{dV_s}{dt}+(R_{V_{ss}}f_1+1)V_s\cong$$
$$R_{V_{ss}}B_nV_{dd}^n(\frac{t}{\tau_r}-\nu_n)^n+\frac{L_{V_{ss}}B_nV_{dd}^n}{\tau_r}(\frac{t}{\tau_r}-\nu_n)^{n-1}, \tag{10.8}$$

where $\nu_n=\frac{V_{TN}}{V_{dd}}$. No close form solution of this differential equation exists due to the non-integer value of n and $n-1$. In order to derive an analytical expression for the differential equation, $(\frac{t}{\tau_r}-\nu_n)^n$ and $(\frac{t}{\tau_r}-\nu_n)^{n-1}$ are approximated by a polynomial expansion to the fifth order, where the average error is less than 3%,

$$\xi^n\approx a_0+a_1\xi+a_2\xi^2+a_3\xi^3+a_4\xi^4+a_5\xi^5,$$
$$\xi^{n-1}\approx b_0+b_1\xi+b_2\xi^2+b_3\xi^3+b_4\xi^4+b_5\xi^5, \tag{10.9}$$

where $\xi=\frac{t}{\tau_r}-\nu_n$. Note that a_i and b_i for $i=0\ldots5$ are independent of the input transition time τ_r. The solution of the simultaneous switching noise voltage is

$$V_s=c_0(1-e^{-\frac{t-\tau_n}{\gamma\tau_r}})+c_1\xi+c_2\xi^2+c_3\xi^3+c_4\xi^4+c_5\xi^5 \quad \text{for} \quad \tau_n\le t\le\tau_r, \tag{10.10}$$

where

$$\gamma=\frac{R_{V_{ss}}C_{V_{ss}}+L_{V_{ss}}f_1}{(R_{V_{ss}}f_1+1)\tau_r}, \tag{10.11}$$

$$\tau_n=\frac{V_{TN}}{V_{dd}}\tau_r=\nu_n\tau_r. \tag{10.12}$$

These coefficients are

$$\begin{aligned}
c_0 =& A_0\gamma - A_1\gamma^2 + 2A_2\gamma^3 - 6A_3\gamma^4 + 24A_4\gamma^5 - 120A_5\gamma^6,\\
c_1 =& A_1\gamma - 2A_2\gamma^2 + 6A_3\gamma^3 - 24A_4\gamma^4 + 120A_5\gamma^5,\\
c_2 =& A_2\gamma - 3A_3\gamma^2 + 12A_4\gamma^3 - 60A_5\gamma^4,\\
c_3 =& A_3\gamma - 4A_4\gamma^2 + 20A_5\gamma^3,\\
c_4 =& A_4\gamma - 5A_5\gamma^2,\\
c_5 =& A_5\gamma. \qquad (10.13)
\end{aligned}$$

The A_i for $i = 0 \ldots 5$ are

$$A_i = \frac{R_{V_{ss}} B_n V_{dd}^n \tau_r}{R_{V_{ss}} C_{V_{ss}} + L_{V_{ss}} f_1} a_i + \frac{L_{V_{ss}} B_n V_{dd}^n}{R_{V_{ss}} C_{V_{ss}} + L_{V_{ss}} f_1} b_i, \qquad (10.14)$$

where a_i and b_i are defined in (10.9). The simultaneous switching noise voltage reaches a maximum when the input voltage completes the transition, *i.e.*, $t = \tau_r$.

$$V_{s,max} = c_0(1 - e^{-\frac{\tau_r - \tau_n}{\gamma\tau_r}}) + c_1\xi_r + c_2\xi_r^2 + c_3\xi_r^3 + c_4\xi_r^4 + c_5\xi_r^5, \qquad (10.15)$$

where $\xi_r = 1 - \nu_n$.

The simultaneous switching noise voltage on a ground rail as predicted by (10.10) is compared to SPICE in Figure 10.3 for a single CMOS inverter with $W_n = 3.6\,\mu$m, $W_p = 7.2\,\mu$m, and $C_l = 1$ pF based on a $0.5\,\mu$m CMOS technology. The solid line represents the analytical prediction and the dashed line represents the results from SPICE simulations. During the time period from τ_n to τ_r, the analytical result agrees quite closely with SPICE (the error is less than 10%).

This analysis is based on a single inverter. If m simultaneously switching logic gates are connected to the same ground rail, the total simultaneous switching noise voltage can be obtained by substituting mB_n for B_n in (10.11) and (10.14).

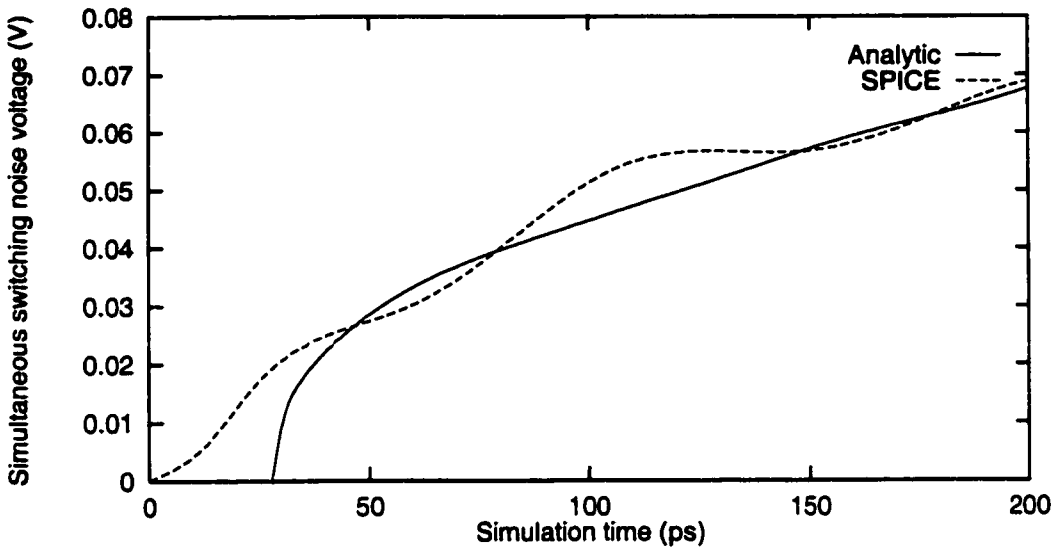


Figure 10.3: Simultaneous switching noise voltage on the ground rail for a single switching logic gate with $L_{V_{ss}} = 2\,\text{nH}$, $R_{V_{ss}} = 5\,\Omega$, $C_{V_{ss}} = 0.1\,\text{pF}$, $\tau_n = 29\,\text{ps}$, and $\tau_r = 200\,\text{ps}$.

Note that all c_i for $i = 0 \ldots 5$ are proportional to m, $\frac{1}{\tau_r}$, and B_n. Therefore, the simultaneous switching noise voltage increases with the number of simultaneous switching logic gates m, the input slew rate $\frac{1}{\tau_r}$, and the drive current of the logic gates B_n.

The analytical prediction of the simultaneous switching noise voltage for five simultaneously switching CMOS inverters with $W_n = 3.6\,\mu\text{m}$, $W_p = 7.2\,\mu\text{m}$, and $C_l = 1\,\text{pF}$ is compared to SPICE in Figure 10.4, exhibiting less than 7% error. During the time interval from τ_n to τ_r, the analytical evaluation accurately models the results from SPICE simulations.

Similarly, the analytical expression for the simultaneous switching noise voltage on the power rail can be derived based on this same procedure. An estimate of the simultaneous switching noise voltage on the power rail based on the model presented in [121] is less accurate because an assumption that n is close to one

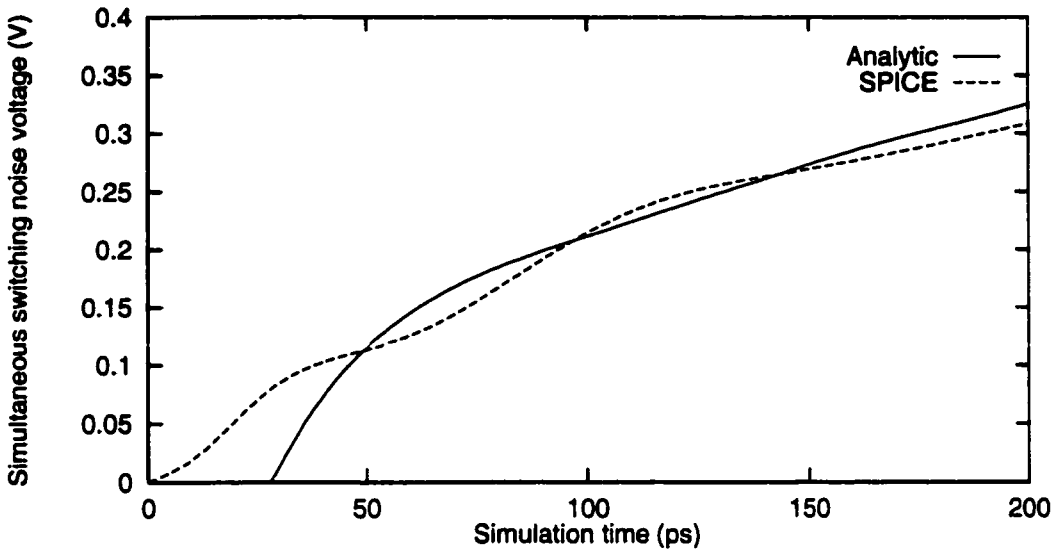


Figure 10.4: Simultaneous switching noise voltage on a ground rail for five simultaneously switching logic gates with $L_{V_{ss}} = 2\,\text{nH}$, $R_{V_{ss}} = 5\,\Omega$, $C_{V_{ss}} = 0.1\,\text{pF}$, $\tau_n = 29\,\text{ps}$, and $\tau_r = 200\,\text{ps}$.

$(1 \leq n \leq 1.2)$ is made. This assumption is appropriate for short-channel NMOS transistors, but the value of n in a short-channel PMOS transistor is higher, typically in the range of 1.5 to 1.8 (it is 1.68 in the target $0.5\,\mu\text{m}$ CMOS technology).

A comparison of the simultaneous switching noise voltage on the power rail is shown in Figure 10.5. The effect of the carrier velocity saturation on a PMOS transistor is small as compared to an NMOS transistor. Therefore, the prediction based on the model presented in [121] cannot approximate the simultaneous switching noise voltage on the power rail as shown in Figure 10.5. Note that the analytical expression presented here accurately predicts the SSN on the power rails. The coefficients for the polynomial expansion in (10.9) are listed in Table 10.1 with $n_n = 1.29$ and $n_p = 1.68$.

The peak value of the SSN as compared to SPICE is shown in Figure 10.6 with $W_n = 1.8\,\mu\text{m}$, $W_p = 3.6\,\mu\text{m}$, and $C_l = 1.0\,\text{pF}$. The dashed line represents the peak

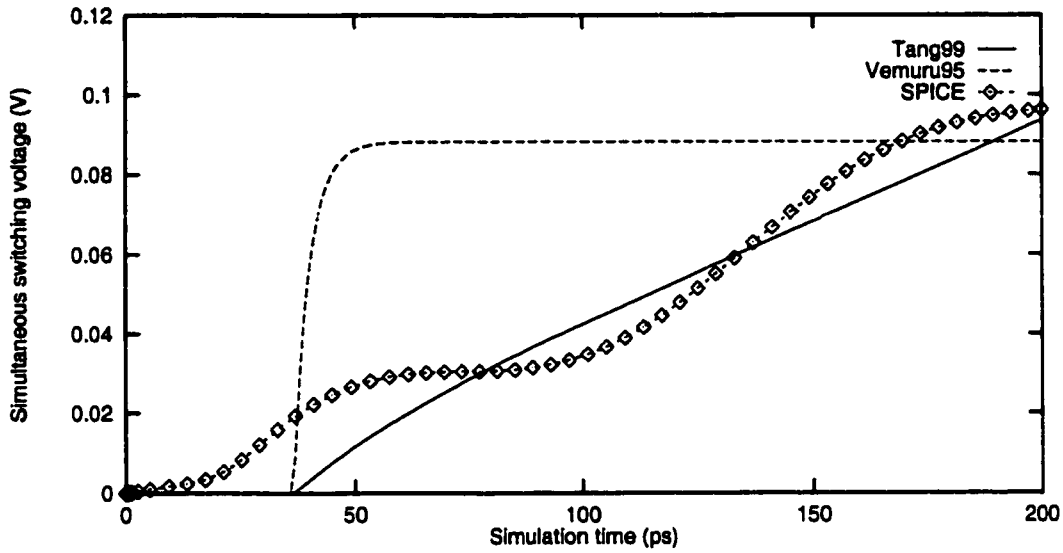


Figure 10.5: The simultaneous switching voltage on a power rail with $L_{V_{dd}} = 2\,\text{nH}$, $R_{V_{dd}} = 5\,\Omega$, $C_{V_{dd}} = 0.2\,\text{pF}$, $\tau_p = 39\,\text{ps}$, and $\tau_r = 200\,\text{ps}$.

Table 10.1: Polynomial expansion coefficients of a 0.5 μm CMOS technology

Coef.	NMOS		PMOS	
	ξ^{n_n}	ξ^{n_n-1}	ξ^{n_p}	ξ^{n_p-1}
0th	-0.0023	0.2391	-0.0008	0.0255
1st	0.4132	3.9601	0.0777	2.2010
2nd	1.4836	-14.9465	1.4986	-4.7503
3rd	-2.0667	31.7737	-1.2056	9.0439
4th	1.8168	-32.4443	0.9537	-8.8016
5th	-0.6502	12.5497	-0.3262	3.3138

value of the predicted SSN based on the analytical expression described by (10.15). The dotted line describes the results derived from the SPICE simulations. The accuracy of the analytical prediction is within 10% as compared to SPICE. The peak SSN voltage based on (10.15) is compared to SPICE for different conditions, as illustrated in Tables 10.2 and 10.3 for both the ground and V_{dd} rails, respectively, with $W_n = 1.8\,\mu$m, $W_p = 3.6\,\mu$m, and the input transition time $\tau_r = 200$ ps. Note that the maximum error of the analytical expression is within 10% of SPICE.

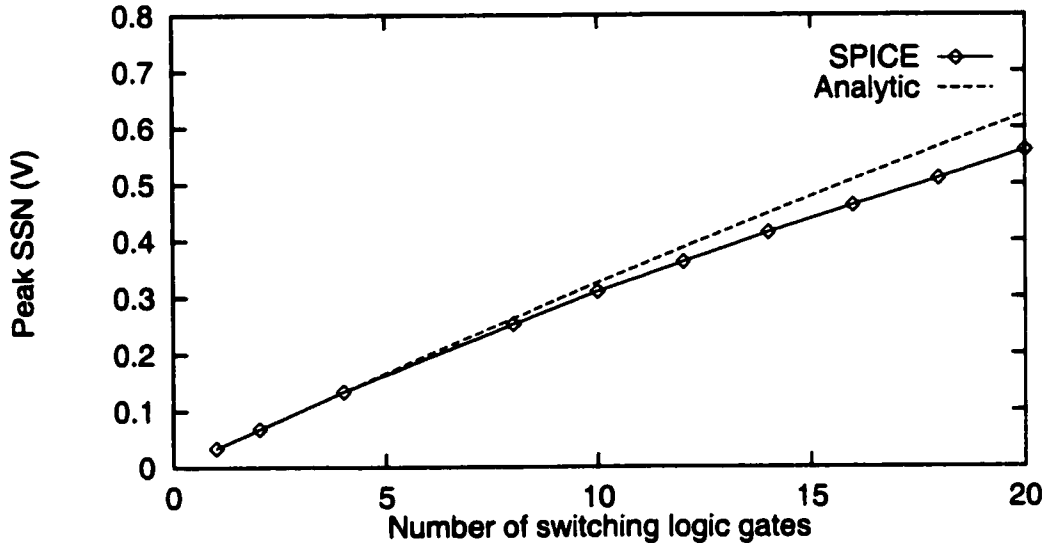


Figure 10.6: The peak value of the simultaneous switching noise voltage with $L_{V_{ss}} = 2$ nH, $R_{V_{ss}} = 5\,\Omega$, $C_{V_{ss}} = 0.1$ pF, and $\tau_r = 200$ ps.

The NMOS transistor is assumed to remain saturated when the input transition is completed. The on-chip simultaneous switching noise voltage in this region can be expressed as

$$V_s(t) = V_{s,1} + [V_s(\tau_r) - V_{s,1}]e^{-\tau_2(t-\tau_r)} \qquad \text{for } \tau_r \le t \le \tau_{sat}, \tag{10.16}$$

Table 10.2: Comparison of peak simultaneous switching noise voltage on the ground rails, Num is the number of simultaneously switching logic gates

Power Rail			Number of switching logic gates								
R	L	C	Peak SSN (V) (Num=5)			Peak SSN (V) (Num=10)			Peak SSN (V) (Num=15)		
(Ω)	(nH)	(pF)	Analytic	SPICE	δ (%)	Analytic	SPICE	δ (%)	Analytic	SPICE	δ (%)
2.0	1.0	0.1	0.0802	0.0762	5.2	0.159	0.150	6.0	0.236	0.218	8.2
		0.2	0.0802	0.0806	0.5	0.159	0.152	4.6	0.236	0.219	7.7
		0.3	0.0801	0.0790	0.3	0.159	0.151	5.3	0.235	0.217	8.2
	2.0	0.1	0.143	0.141	1.4	0.282	0.265	6.4	0.417	0.381	9.4
		0.2	0.143	0.137	4.3	0.282	0.263	7.2	0.417	0.380	9.7
		0.3	0.142	0.138	2.9	0.281	0.260	8.0	0.415	0.378	9.8
	4.0	0.1	0.267	0.256	4.3	0.522	0.490	6.5	0.760	0.697	9.0
		0.2	0.267	0.252	5.9	0.522	0.500	4.4	0.766	0.710	3.6
		0.3	0.267	0.286	6.6	0.521	0.530	1.7	0.765	0.742	3.5
5.0	1.0	0.1	0.104	0.102	1.9	0.206	0.197	4.6	0.300	0.284	5.6
		0.2	0.104	0.106	1.8	0.206	0.199	3.5	0.300	0.283	6.0
		0.3	0.104	0.104	0.0	0.206	0.198	4.0	0.300	0.282	6.3
	2.0	0.1	0.167	0.165	1.2	0.320	0.310	3.2	0.470	0.438	7.3
		0.2	0.167	0.162	3.1	0.320	0.308	3.9	0.470	0.436	7.7
		0.3	0.166	0.153	8.5	0.319	0.302	5.6	0.469	0.434	8.0
	4.0	0.1	0.288	0.278	3.6	0.560	0.526	6.4	0.810	0.750	8.0
		0.2	0.288	0.281	2.5	0.560	0.534	4.8	0.810	0.752	7.7
		0.3	0.287	0.308	6.5	0.559	0.567	0.1	0.810	0.790	2.5
Maximum error (%)			8.5			8.0			9.8		
Average error (%)			3.4			4.7			7.1		

Table 10.3: Comparison of peak simultaneous switching noise voltage on the V_{dd} rails, Num is the number of simultaneously switching logic gates

Power Rail			Number of switching logic gates								
R	L	C	Peak SSN (V) (Num=5)			Peak SSN (V) (Num=10)			Peak SSN (V) (Num=15)		
(Ω)	(nH)	(pF)	Analytic	SPICE	δ (%)	Analytic	SPICE	δ (%)	Analytic	SPICE	δ (%)
2.0	1.0	0.1	4.890	4.89	0.0	4.778	4.78	0.0	4.672	4.68	0.1
		0.2	4.890	4.89	0.0	4.778	4.79	0.1	4.670	4.68	0.1
		0.3	4.890	4.89	0.0	4.776	4.79	0.1	4.670	4.67	0.0
	2.0	0.1	4.794	4.81	0.3	4.599	4.63	0.6	4.412	4.47	1.3
		0.2	4.793	4.79	0.1	4.598	4.61	0.4	4.412	4.47	1.3
		0.3	4.794	4.79	0.1	4.600	4.61	0.1	4.410	4.46	1.3
	4.0	0.1	4.604	4.62	0.3	4.261	4.35	2.0	3.995	4.14	3.6
		0.2	4.604	4.63	0.4	4.260	4.36	2.0	3.994	4.13	3.6
		0.3	4.603	4.62	0.3	4.262	4.34	2.1	3.990	4.13	3.5
5.0	1.0	0.1	4.861	4.86	0.0	4.728	4.73	0.2	4.601	4.62	0.4
		0.2	4.860	4.86	0.0	4.726	4.73	0.2	4.600	4.62	0.4
		0.3	4.860	4.87	0.0	4.726	4.74	0.3	4.600	4.61	0.4
	2.0	0.1	4.770	4.78	0.2	4.554	4.59	0.8	4.351	4.42	1.6
		0.2	4.771	4.78	0.2	4.552	4.59	0.8	4.350	4.41	1.5
		0.3	4.770	4.76	0.2	4.552	4.58	0.8	4.350	4.42	1.6
	4.0	0.1	4.692	4.61	1.8	4.224	4.32	2.3	3.900	4.10	9.2
		0.2	4.690	4.61	1.7	4.220	4.32	2.3	3.905	4.11	9.3
		0.3	4.690	4.60	1.7	4.220	4.31	2.1	3.905	4.12	9.3
Maximum error (%)			1.8			2.3			9.3		
Average error (%)			0.4			1.0			2.8		

where

$$V_{s,1} = \frac{mB_n R_{Vss}(V_{dd} - V_{TN})^n}{R_{V_{ss}} f_{2,m} + 1}, \tag{10.17}$$

$$\tau_2 = \frac{R_{V_{ss}} f_{2,m} + 1}{R_{V_{ss}} C_{V_{ss}} + L_{V_{ss}} f_{2,m}}, \tag{10.18}$$

$$f_{2,m} = mnB_n(V_{dd} - V_{TN} - V_s(\tau_r))^{(n-1)}. \tag{10.19}$$

τ_{sat} the time duration when the NMOS transistor remains in the saturation region.

After τ_{sat}, the NMOS transistor operates in the linear region. In order to derive a tractable expression, the drain-to-source current is approximated by $\gamma_n V_{DS}$, where γ_n is the effective output conductance of the NMOS transistor. The on-chip simultaneous switching noise voltage in this region is

$$V_s(t) = K_1 e^{-\frac{\beta_1 t}{2}} + K_2 e^{-\frac{\beta_2 t}{2}} \qquad \text{for } t \geq \tau_{sat}, \tag{10.20}$$

where

$$\begin{aligned} B_1 &= \frac{mR_{V_{ss}} C_L + R_{V_{ss}} C_{V_{ss}} + \frac{C_L}{\gamma_n}}{R_{V_{ss}} C_{V_{ss}} \frac{C_L}{\gamma_n} + mL_{V_{ss}} C_L + L_{Vss} C_{V_{ss}}}, \\ B_2 &= \frac{1}{R_{V_{ss}} C_{V_{ss}} \frac{C_L}{\gamma_n} + mL_{V_{ss}} C_L + L_{Vss} C_{V_{ss}}}, \\ \beta_1 &= B_1 + \sqrt{B_1^2 - 4B_2}, \\ \beta_2 &= B_1 - \sqrt{B_1^2 - 4B_2}. \end{aligned} \tag{10.21}$$

C_L is the load capacitance. K_1 and K_2 are integration constants and can be determined from $V_s(\tau_{sat})$ and $V_s'(\tau_{sat})$. However, the effective output conductance of an MOS transistor also depends upon the output voltage in the linear region, changing from γ_{nsat} to $2\gamma_{nsat}$ [41]. In order to accurately characterize the on-chip simultaneous switching noise voltage, γ_n is chosen between γ_{nsat} and $2\gamma_{nsat}$.

$B_1^2 - 4B_2$ can be expressed as

$$B_1^2 - 4B_2 = (mR_{V_{ss}}C_L + R_{V_{ss}}C_{V_{ss}} + \frac{C_L}{\gamma_n})^2 - 4(R_{V_{ss}}C_{V_{ss}}\frac{C_L}{\gamma_n} + mL_{V_{ss}}C_L + L_{Vss}C_{V_{ss}}). \tag{10.22}$$

If $B_1^2 - 4B_2$ is less than zero,

$$L_{V_{ss}} > \frac{(mR_{V_{ss}}C_L + R_{V_{ss}}C_{V_{ss}} + \frac{C_L}{\gamma_n})^2 - 4R_{V_{ss}}C_{V_{ss}}\frac{C_L}{\gamma_n}}{4(mC_L + C_{V_{ss}})}, \tag{10.23}$$

resulting in a complex solution, which means the on-chip simultaneous switching noise oscillates sinusoidally until exponentially reaching a steady state voltage in the linear region. The critical value defined in (10.23) depends upon the resistance and capacitance of the power supply rail ($R_{V_{ss}}$ and $C_{V_{ss}}$), the load condition (C_L), the effective output conductance of the NMOS transistor (γ_n), and the number of switching gates (m). In practical integrated circuits, the load condition, the size of the MOS transistors, and the number of switching gates should be optimized in order to satisfy the condition described by (10.23). The on-chip simultaneous switching noise voltage can be approximated by forcing the imaginary part to zero,

$$V_s(t) = V_s\tau_{sat}e^{-\frac{\beta_3(t-\tau_{sat})}{2}}\frac{cos(\beta_4 t)}{cos(\beta_4\tau_{sat})} \qquad \text{for } t \geq \tau_{sat}, \tag{10.24}$$

where $\beta_3 = B_1$ and $\beta_4 = \sqrt{4B_2 - B_1^2}$. If $R_{V_{ss}}$ and $C_{V_{ss}}$ are assumed to be zero, the solution represented by (10.24) and the condition defined by (10.23) are similar to the results presented in [124], which characterizes the simultaneous switching noise voltage caused by the off-chip bonding wires. The parasitic inductance within the on-chip power distribution network is typically less than the critical value defined in (10.23) [123]. However, for off-chip bonding wires, the condition defined in (10.23) may occur, where the simultaneous switching noise oscillates sinusoidally

before exponentially reaching a steady state voltage [124]. Therefore, the model of the power supply rails presented here is a unified approach which can characterize both on-chip and off-chip simultaneous switching noise.

10.3 Discussion

The dependence of the peak SSN voltage on the capacitive load is described in Section 10.3.1. Circuit- and layout-level constraints related to the peak SSN voltage are discussed in sections 10.3.2 and 10.3.3, respectively.

10.3.1 Capacitive Load

The NMOS transistor is assumed here to operate in the saturation region before the input transition is completed. This assumption depends upon the input transition time, the capacitive load, and the device transconductance. Vemuru notes in [121] that the peak value of the simultaneous switching noise voltage depends on the capacitive load.

The time when the NMOS transistor leaves the saturation region τ_{sat} is

$$\tau_{sat} = \frac{C_l}{B_n V_{dd}^n}(V_{dd} - V_{DSAT}) + \frac{\nu_n + n}{1+n}\tau_r, \tag{10.25}$$

where $V_{DSAT} = K(V_{dd} - V_{TN})^m$ is the drain-to-source saturation voltage. If $\tau_{sat} \geq \tau_r$, the assumption that the NMOS transistor operates solely within the saturation region before the input transition is completed is appropriate. This constraint can be expressed as

$$C_l \geq \frac{(1-\nu_n)B_n V_{dd}^n}{(1+n)(V_{dd} - V_{DSAT})}\tau_r. \tag{10.26}$$

The dependence of the peak simultaneous switching noise voltage on the load capacitance is shown in Figure 10.7 with $W_n = 3.6\,\mu$m and $W_p = 7.2\,\mu$m. The right

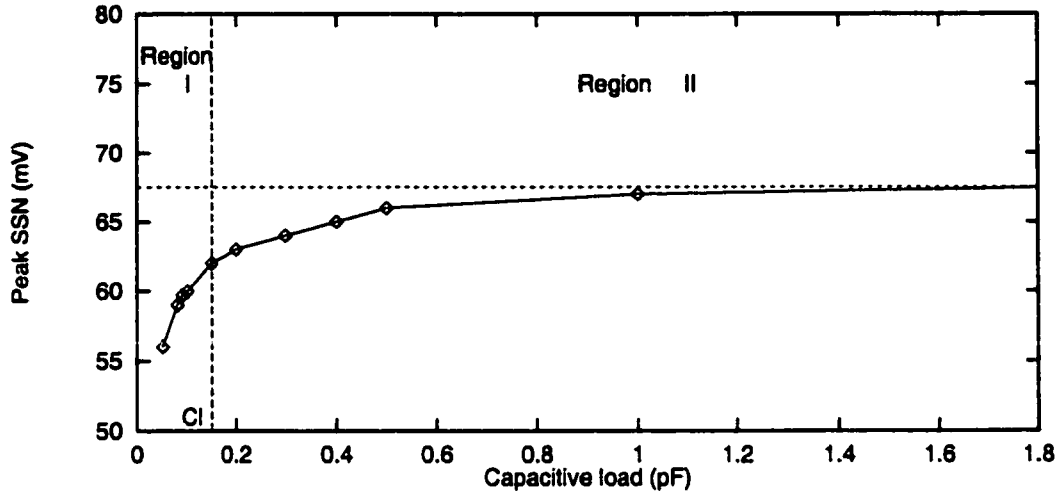


Figure 10.7: Dependence of the peak simultaneous switching noise voltage on the load capacitance with $\tau_r = 200$ ps.

side of the vertical dashed line C_l, *i.e.*, Region II, satisfies the constraint defined by (10.26). The horizontal dashed line represents the analytically predicted peak simultaneous switching voltage. The accuracy of the analytical expression in Region II is within 10% of SPICE. Therefore, if the load capacitance and the input transition time satisfy the constraint defined by (10.26), the analytical prediction accurately estimates the peak simultaneous switching noise voltage.

10.3.2 Circuit-Level Constraints

The simultaneous switching noise voltage should be less than a target V_c for a circuit to operate properly. Circuit design parameters, such as the input transition time τ_r, the drive current of each logic gate B_n, and the number of simultaneously switching logic gates connected to the same power supply rail m, can be determined based on

$$V_{s,max}(m, B_n, \tau_r) \leq V_c, \tag{10.27}$$

where $V_{s,max}$ is defined in (10.15).

For example, the maximum number of simultaneously switching logic gates connected to the same power supply rail can be determined based on this constraint. Assume that $V_c = V_{TN} = 0.75V$. The maximum number of switching logic gates for different conditions is shown in Figure 10.8. $C1$ is the condition of $\tau_r = 200\,\text{ps}$ and $W_n = 3.6\,\mu\text{m}$, $C2$ is the condition of $\tau_r = 400\,\text{ps}$ and $W_n = 3.6\,\mu\text{m}$, and $C3$ is the condition of $\tau_r = 200\,\text{ps}$ and $W_n = 1.8\,\mu\text{m}$. $N1 = 12$, $N2 = 20$, and $N3 = 23$ are the maximum number of switching logic gates for each case, respectively.

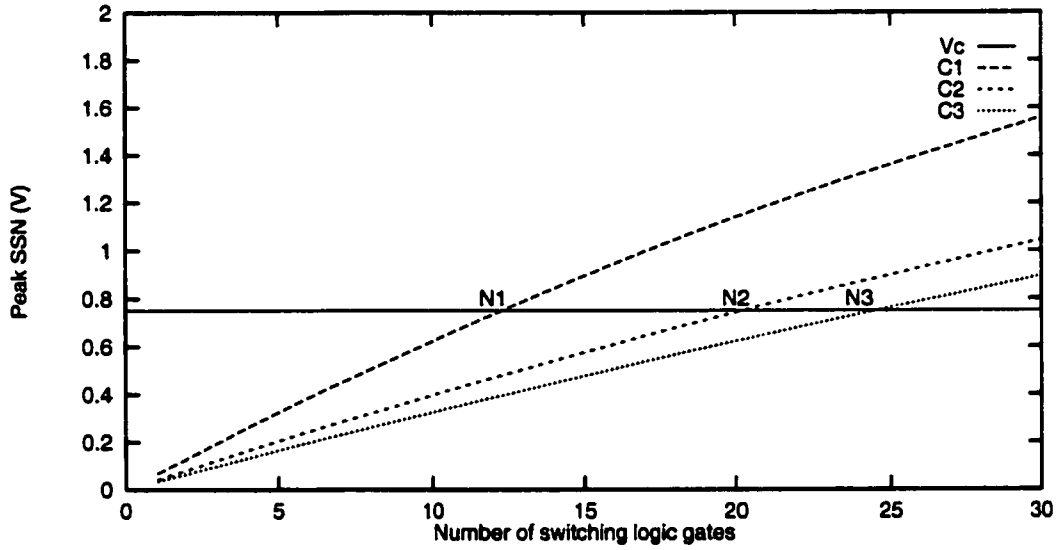


Figure 10.8: The maximum number of simultaneously switching logic gates with $L_{V_{ss}} = 2\,\text{nH}$, $R_{V_{ss}} = 5\,\Omega$, and $C_{V_{ss}} = 0.1\,\text{pF}$. V_c is the voltage target, $C1$: $\tau_r = 200\,\text{ps}$, $W_n = 3.6\,\mu\text{m}$, $C2$: $\tau_r = 400\,\text{ps}$, $W_n = 3.6\,\mu\text{m}$, and $C3$: $\tau_r = 200\,\text{ps}$, $W_n = 1.8\,\mu\text{m}$.

The on-chip simultaneous switching noise voltage results from the parasitic inductance of the power rails and the large current surges within a short period of time. Therefore, the peak simultaneous switching noise voltage increases as the input transition time decreases. The constraint of the input transition time is shown in Figure 10.9 for different number of simultaneously switching gates,

e.g., 10, 15, and 20 with $L_{V_{ss}} = 2\,\text{nH}$, $R_{V_{ss}} = 5\,\Omega$, $C_{V_{ss}} = 0.1\,\text{pF}$, and $W_n = 1.8\,\mu\text{m}$. $t1 = 85\,\text{ps}$, $t2 = 115\,\text{ps}$, and $t3 = 180\,\text{ps}$ are the limits of the input transition times for each condition, respectively. If the number of simultaneously switching logic gates increases, the input slew rate ($\frac{1}{\tau_r}$) should be decreased in order to decrease the maximum simultaneous switching noise voltage. The peak noise values for different input transition times with $L_{V_{ss}} = 1\,\text{nH}$, $R_{V_{ss}} = 5\,\Omega$, and $C_{V_{ss}} = 0.1\,\text{pF}$ are listed in Table 10.4, note that for a very short input transition time, *i.e.*, 20 ps, the analytical model still provides an accurate estimation of the peak noise. The analytical error is within 8% of SPICE as listed in Table 10.4.

Table 10.4: Peak SSN for short input transition times

Transition time	$m = 5$			$m = 10$		
τ (ps)	SPICE (V)	Analytic (V)	Error (%)	SPICE (V)	Analytic (V)	Error (%)
150	0.123	0.125	1.6	0.230	0.246	7.0
100	0.166	0.166	<1.0	0.3155	0.325	3.2
80	0.194	0.917	1.5	0.371	0.384	3.5
50	0.312	0.288	7.7	0.570	0.559	1.9
20	0.715	0.658	8.0	1.17	1.18	0.8
Maximum error (%)					8.0	
Average error (%)					3.5	

Also note that the simultaneous switching noise voltage is proportional to the nth power of the supply voltage (V_{dd}^n). Therefore the normalized simultaneous switching voltage V_s/V_{dd} is proportional to the $(n-1)$th power of the supply voltage (V_{dd}^{n-1}), permitting the supply voltage to be reduced in order to decrease the SSN voltage. The dashed line shown in Figure 10.10 represents the normalized peak value of the simultaneous switching noise voltage $V_{s,max}/V_{dd}$ and the solid line represents the absolute value of the peak SSN.

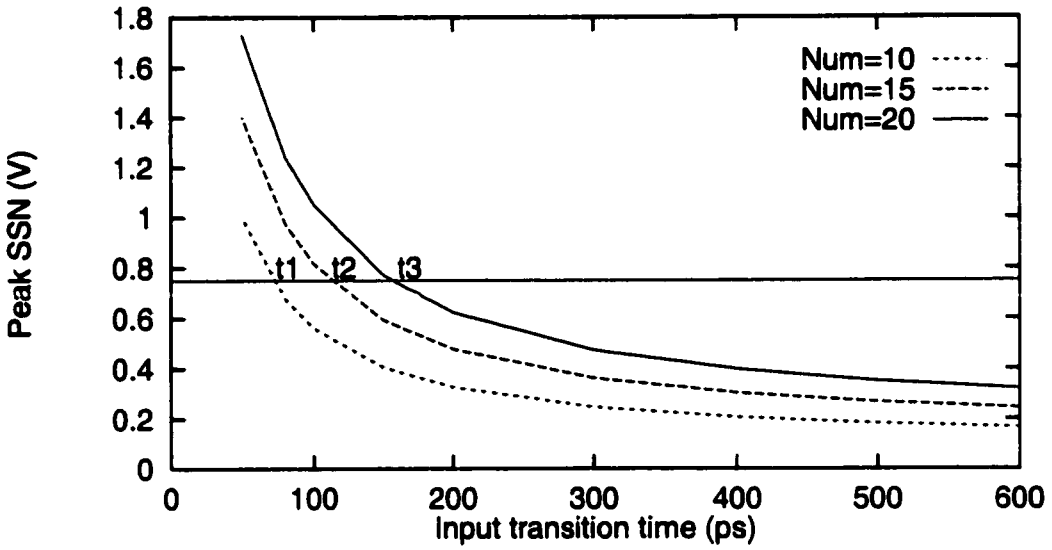


Figure 10.9: Peak SSN as a function of the input transition time. Note the limiting constraints on the input transition time for different number of simultaneously switching gates, Num = 10, 15, and 20.

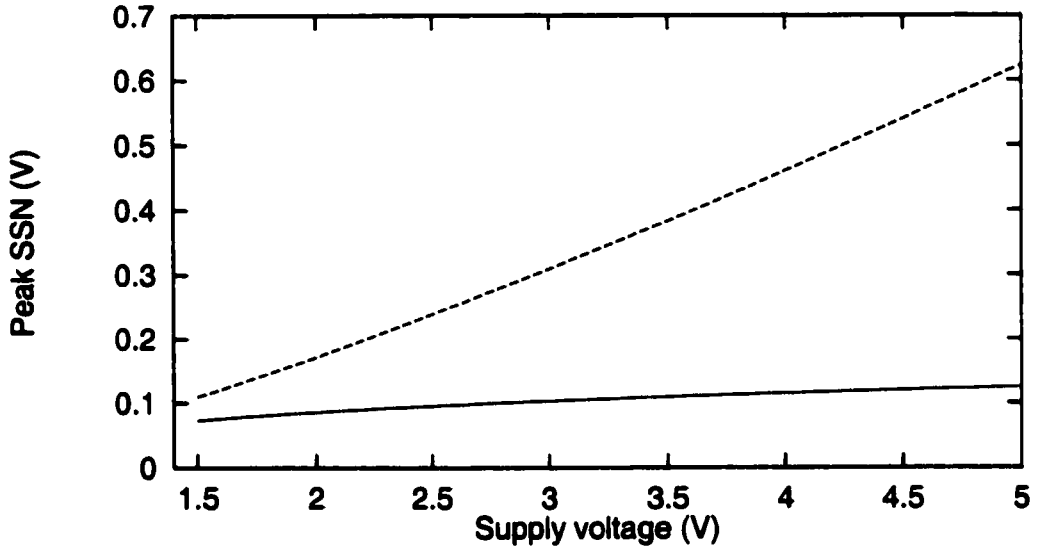


Figure 10.10: Dependence of the peak value of the SSN on the power supply with $m = 10$, $L_{V_{ss}} = 2\,\text{nH}$, $R_{V_{ss}} = 5\,\Omega$, $C_{V_{ss}} = 0.1\,\text{pF}$, and $\tau_r = 200\,\text{ps}$.

10.3.3 Layout-Level Constraints

The peak SSN can be controlled by reducing the parasitic inductance of the power supply rails. The parasitic inductance L, resistance R, and capacitance C of the power supply rails can be determined from the physical geometries of the layout, *i.e.*, the width (w), thickness (h), length (l), and spacing (s) of the power supply rails.

$$V_{s,max}(R, L, C) = V_{s,max}(w, h, l, s) \leq V_c. \tag{10.28}$$

Extraction of the parasitic RLC impedance of the on-chip interconnect is currently an important research topic [44, 60, 62]. However, if compact models characterizing the parasitic impedance of the power supply rails are available, guidelines such as presented in (10.28) for designing the on-chip power distribution network can be developed. By combining both of the constraints represented by (10.27) and (10.28), the peak SSN voltage for a circuit to operate properly can be determined.

The parasitic inductance of the power rails is proportional to the length of the power rails. Even though the dependence of the parasitic inductance on w, h, and s are not available, the length of the power rail can be determined based on the parasitic impedance per unit length. The constraint of the power rail length is shown in Figure 10.11 for different conditions assuming 15 simultaneously switching logic gates. $l1 = 0.98\,\text{cm}$, $l2 = 1.85\,\text{cm}$, and $l3 = 1.70\,\text{cm}$ are the length limits for each condition in this case, respectively.

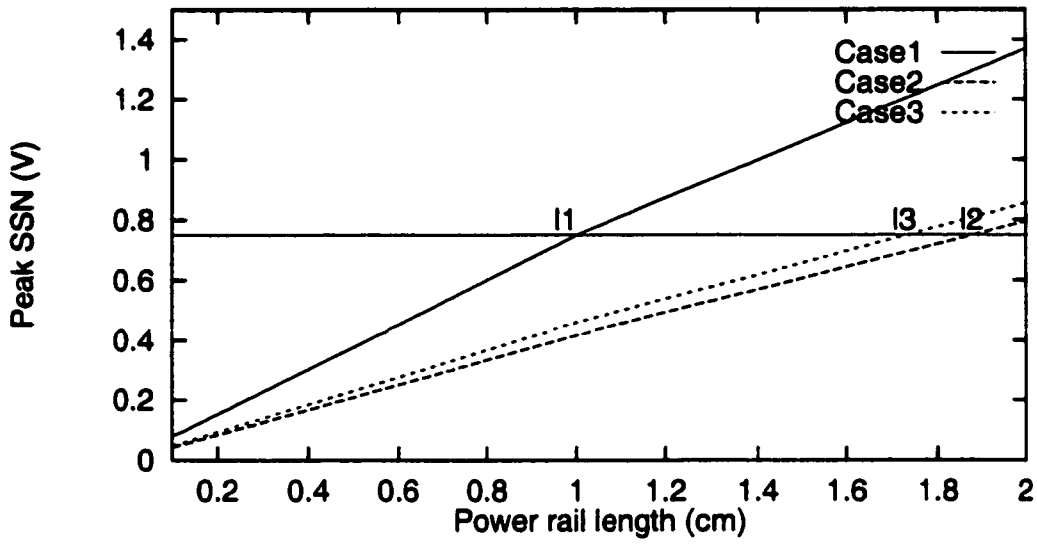


Figure 10.11: Peak SSN as a function of the length of the power rails. Note the limiting constraints on the length of the power rails with 15 simultaneously switching logic gates. Case 1: $L_{V_{ss}} = 2\,\text{nH/cm}$, $R_{V_{ss}} = 1\,\Omega/\text{cm}$, and $C_{V_{ss}} = 0.1\,\text{pF/cm}$, Case 2: $L_{V_{ss}} = 1\,\text{nH/cm}$, $R_{V_{ss}} = 2\,\Omega/\text{cm}$, and $C_{V_{ss}} = 0.1\,\text{pF/cm}$, and Case 3: $L_{V_{ss}} = 1\,\text{nH/cm}$, $R_{V_{ss}} = 4\,\Omega/\text{cm}$, and $C_{V_{ss}} = 0.1\,\text{pF/cm}$.

10.4 Output Voltage Waveform and Propagation Delay Models

Analytical expressions characterizing the output voltage and propagation delay of a CMOS logic gate, which include the effect of on-chip simultaneous switching noise, are presented for both a capacitive and a resistive-capacitive load in Sections 10.4.1 and 10.4.2, respectively. The analytical results are also compared to both an analytical model which does not consider on-chip simultaneous switching noise and SPICE.

10.4.1 Capacitive load

Analytical expressions characterizing the output voltage of a CMOS logic gate driving a capacitive load based on an assumption of a fast ramp input signal are listed in Table 10.5, where $f_{1,s} = \frac{f_{1,m}}{m}$ and $f_{2,s} = \frac{f_{2,m}}{m}$. K_1 and K_2 are determined from $V_o(\tau_{sat})$ and $V_o'(\tau_{sat})$. Note that both $\frac{f_{1,s}\tau_r}{C_L}V_{s,2}(t)$ in (10.29) and $\frac{f_{2,s}}{C_L}V_{s,3}(t)$ in (10.31) cause the output voltage to drop slowly during a high-to-low output transition. Therefore, the on-chip simultaneous switching noise affects the waveform shape of the output voltage and causes a change in the propagation delay of a CMOS logic gate driving a capacitive load.

Table 10.5: Analytical expressions characterizing the output voltage of a CMOS inverter driving a capacitive load

Region	Analytical expressions
$[\tau_n, \tau_r]$	$V_o(t) = V_{dd} - \frac{B_n\tau_r V_{dd}^n}{(n+1)C_L}\xi^{(n+1)} + \frac{f_{1,s}\tau_r}{C_L}V_{s,2}(t)$ (10.29) $V_{s,2}(t) = (\xi + \frac{e^{-\tau_1\xi}}{\tau_1})c_0 + \frac{c_1}{2}\xi^2 + \frac{c_2}{3}\xi^3 + \frac{c_3}{4}\xi^4 + \frac{c_4}{5}\xi^5 + \frac{c_5}{6}\xi$ (10.30)
$[\tau_r, \tau_{sat}]$	$V_o(t) = V_o(\tau_r) - \frac{B_n}{C_L}(V_{dd} - V_{TN})^n(t-\tau_r) + \frac{f_{2,s}}{C_L}V_{s,3}(t)$ (10.31) $V_{s,3}(t) = V_{s,1}(t-\tau_r) + \frac{V_s(\tau_r) - V_{s,1}}{\tau_2}(1 - e^{-\tau_2(t-\tau_r)})$ (10.32)
$t \geq \tau_{sat}$	$V_o(t) = K_1 e^{-\frac{\beta_1 t}{2}} + K_2 e^{-\frac{\beta_2 t}{2}}$ (10.33)

The time when the NMOS transistor leaves the saturation region τ_{sat} can be determined as

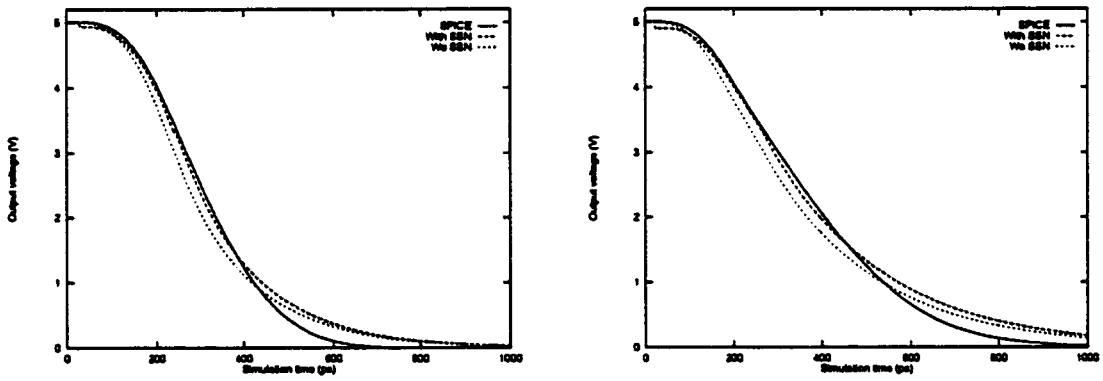
$$V_o(\tau_{sat}) - V_s(\tau_{sat}) = V_{sat}. \tag{10.34}$$

There is no explicit solution of τ_{sat}, but τ_{sat} can be determined by applying the Newton-Raphson technique. The technique typically requires two to four iterations.

If $B_1^2 - 4B_2$ is less than zero, a complex solution of the output voltage results. The output voltage can therefore be approximated as

$$V_s(t) = V_o(\tau_{sat}) e^{-\frac{\beta_3(t-\tau_{sat})}{2}} \frac{cos(\beta_4 t)}{cos(\beta_4 \tau_{sat})} \qquad \text{for } t \geq \tau_{sat}, \tag{10.35}$$

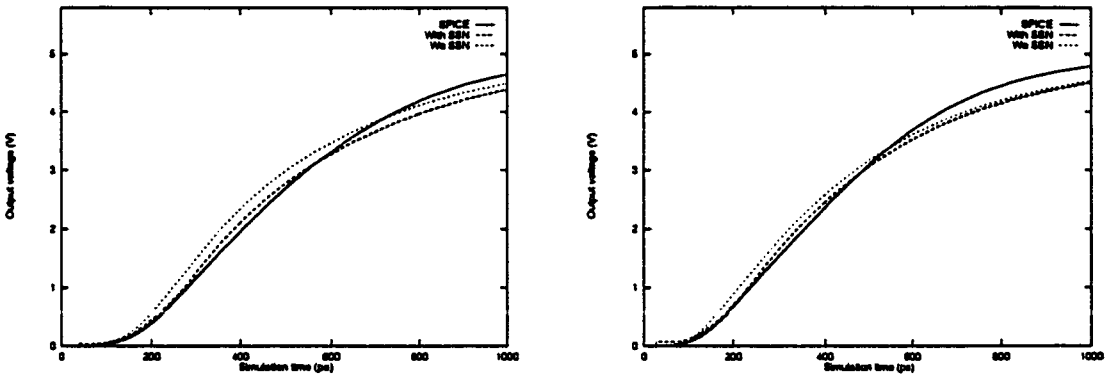
where β_3 and β_4 are defined in (10.24).



(a) $C_L = 0.1\,\text{pF}$ and $\tau_r = 0.20\,\text{ns}$ (b) $C_L = 0.15\,\text{pF}$ and $\tau_r = 0.15\,\text{ns}$

Figure 10.12: Comparison of the analytical output voltage with SPICE during a high-to-low output transition, $L_{V_{ss}} = 3.0\,\text{nH}$, $R_{V_{ss}} = 20.0\,\Omega$, $C_{V_{ss}} = 0.1\,\text{pF}$, $w_n = 1.8\,\mu\text{m}$, $w_p = 3.6\,\mu\text{m}$, and $m = 10$.

The output voltage based on these analytical expressions is compared to SPICE in Figures 10.12 and 10.13 for high-to-low and low-to-high output transitions,



(a) $C_L = 0.1\,\text{pF}$ and $\tau_r = 0.20\,\text{ns}$ (b) $C_L = 0.2\,\text{pF}$ and $\tau_r = 0.15\,\text{ns}$

Figure 10.13: Comparison of the analytical output voltage with SPICE during a low-to-high output transition, $L_{V_{dd}} = 3.0\,\text{nH}$, $R_{V_{dd}} = 20.0\,\Omega$, $C_{V_{dd}} = 0.1\,\text{pF}$, $w_n = 1.8\,\mu\text{m}$, $w_p = 3.6\,\mu\text{m}$, and $m = 10$.

respectively. Note that the analytical waveform which considers on-chip simultaneous switching noise voltage is quite close to SPICE. The difference in the linear region between the analytically derived waveform and SPICE is due to an assumption of a constant effective output conductance γ_{sat} of the MOS transistor in the analysis. However, the effective output conductance of the MOS transistor changes from γ_{nsat} to $2\gamma_{nsat}$ in the linear region [41], causing the analytical prediction which does not consider on-chip simultaneous switching noise to be more accurate than the analytical result based on the expressions listed in Table 10.5 for a portion of the linear region. The effect of the on-chip simultaneous switching noise on the propagation delay of a CMOS logic gate is depicted in Figures 10.12 and 10.13.

The propagation delay of a CMOS logic gates t_P is typically defined as the time from the 50% V_{dd} point of the input to the 50% V_{dd} point of the output. The high-to-low propagation delay of a CMOS logic gate can be determined by

(10.31) or (10.33) using a Newton-Raphson iteration. Since β_1 is greater than β_2 in (10.20), the output voltage in this region can be approximated as

$$V_o(t) = V_o(\tau_{sat})e^{-\frac{\beta_2}{2}(t-\tau_{sat})} \qquad \text{for} \qquad t \geq \tau_{sat}. \tag{10.36}$$

The drain-to-source saturation voltage is typically greater than $0.5V_{dd}$; therefore, the high-to-low propagation delay can be expressed as

$$t_{PHL} = \frac{2}{\beta_2} ln \frac{2V_o(\tau_{sat})}{V_{dd}} + \tau_{sat} - \frac{\tau_r}{2}. \tag{10.37}$$

Similarly, the low-to-high propagation delay of a CMOS logic gate can also be determined based on the time required to charge the load capacitor, which considers the simultaneous switching noise at the V_{dd} rail.

A comparison of the analytical propagation delay expressions with SPICE is listed in Tables 10.6 and 10.7 for both high-to-low and low-to-high output transitions. It is demonstrated in both Tables 10.6 and 10.7 that the delay uncertainty caused by on-chip simultaneous switching noise increases with increasing input slew rate, parasitic inductance, and resistance of the power supply rails. The maximum error of the propagation delay based on the analytical expressions is within 5%, as compared to nearly 16% of SPICE when not considering on-chip simultaneous switching noise. The average improvement in accuracy is about 8%.

10.4.2 Resistive-capacitive load

In this discussion, the interconnect is modeled as a resistive-capacitive impedance. R_L is the load resistance driven by a CMOS logic gate. Analytical expressions characterizing the output voltage of a CMOS logic gate driving a resistive-capacitive load impedance are listed in Table 10.8. Similar to the capacitive load condition, τ_{sat} can be determined by applying the Newton-Raphson technique.

Table 10.6: Comparison of high-to-low propagation delay with SPICE of a CMOS inverter driving a capacitive load including the effect of on-chip simultaneous switching noise

Input Rise Time	Impedance of Ground Rail			Comparison of Propagation Delay				
				Simulation	Analytic Estimation			
τ_r	L	R	C	SPICE	Without SSN		With SSN	
(ps)	(nH)	(Ω)	(pF)	(ps)	(ps)	δ (%)	(ps)	δ (%)
200	1.0	5.0	0.1	182	172	5.5	183	1.1
		10.0	0.1	186	172	7.5	183	1.6
		15.0	0.1	190	172	9.5	186	2.1
		20.0	0.1	194	172	11.3	189	2.6
	2.0	5.0	0.1	186	172	7.5	183	1.6
		10.0	0.1	190	172	9.5	186	2.1
		15.0	0.1	194	172	11.3	189	2.6
		20.0	0.1	198	172	13.1	192	3.0
	3.0	5.0	0.1	191	172	10.0	187	2.1
		10.0	0.1	195	172	11.8	190	2.6
		15.0	0.1	199	172	13.6	192	3.5
		20.0	0.1	203	172	15.3	195	3.9
150	1.0	5.0	0.1	175	166	5.1	174	0.6
		10.0	0.1	180	166	7.7	177	1.7
		15.0	0.1	184	166	9.8	180	2.2
		20.0	0.1	189	166	12.2	183	3.2
	2.0	5.0	0.1	179	166	7.3	177	1.1
		10.0	0.1	184	166	9.7	180	2.2
		15.0	0.1	188	166	11.7	183	2.7
		20.0	0.1	193	166	14.0	185	4.1
	3.0	5.0	0.1	185	166	10.3	180	2.7
		10.0	0.1	188	166	11.7	182	3.2
		15.0	0.1	193	166	14.0	185	4.1
		20.0	0.1	197	166	15.7	188	4.6
Maximum error (%)					15.7		4.6	
Average error (%)					10.6		2.3	

Table 10.7: Comparison of low-to-high propagation delay with SPICE of a CMOS inverter driving a capacitive load including the effect of on-chip simultaneous switching noise

Input Fall Time	Impedance of V_{dd} Rail			Comparison of Propagation Delay				
				Simulation	Analytic Estimation			
τ_f	L	R	C	SPICE	Without SSN		With SSN	
(ps)	(nH)	(Ω)	(pF)	(ps)	(ps)	δ (%)	(ps)	δ (%)
150	1.0	5.0	0.1	321	313	2.5	323	0.6
		10.0	0.1	332	313	5.7	332	0.0
		15.0	0.1	343	313	8.7	339	1.2
		20.0	0.1	355	313	11.8	346	2.5
	2.0	5.0	0.1	325	313	3.7	325	0.0
		10.0	0.1	343	313	7.3	331	3.5
		15.0	0.1	348	313	10.1	338	2.9
		20.0	0.1	359	313	12.8	344	4.2
	3.0	5.0	0.1	331	313	5.4	326	1.5
		10.0	0.1	342	313	8.5	332	2.9
		15.0	0.1	353	313	11.3	339	3.9
		20.0	0.1	363	313	13.8	345	4.9
200	1.0	5.0	0.1	331	323	2.4	333	0.6
		10.0	0.1	341	323	5.3	340	0.3
		15.0	0.1	353	323	8.5	349	1.1
		20.0	0.1	364	323	11.3	355	2.5
	2.0	5.0	0.1	335	323	3.6	335	0.0
		10.0	0.1	346	323	6.6	343	0.9
		15.0	0.1	357	323	9.5	349	2.2
		20.0	0.1	368	323	12.2	356	3.3
	3.0	5.0	0.1	340	323	5.0	338	0.6
		10.0	0.1	351	323	8.0	344	2.0
		15.0	0.1	362	323	10.8	351	3.0
		20.0	0.1	373	323	13.4	357	4.3
Maximum error (%)					13.8		4.9	
Average error (%)					8.3		2.0	

K_1 and K_2 are also determined from $V_o(\tau_{sat})$ and $V_o'(\tau_{sat})$. Both $\frac{f_{1,s}\tau_r}{C_L}V_{s,2}(t)$ in (10.38) and $\frac{f_{2,s}}{C_L}V_{s,3}(t)$ in (10.39) cause the output voltage to drop slowly during a high-to-low output transition for a resistive-capacitive load impedance. Therefore, the on-chip simultaneous switching noise affects the waveform shape of the output voltage, increasing the propagation delay of a CMOS logic gate driving a resistive-capacitive load impedance.

Table 10.8: Analytical expressions characterizing the output voltage of a CMOS inverter driving a resistive-capacitive load

Region	Analytical expressions
$[\tau_n, \tau_r]$	$V_o(t) = V_{dd} - \frac{B_n\tau_r V_{dd}^n}{(n+1)C_L}\xi^{(n+1)} - R_L B_n V_{dd}^n \xi^n + \frac{f_{1,s}\tau_r}{C_L}V_{s,2}(t)$ (10.38)
$[\tau_r, \tau_{sat}]$	$V_o(t) = V_o(\tau_r) - \frac{B_n}{C_L}(V_{dd} - V_{TN})^n(t-\tau_r) + \frac{f_{2,s}}{C_L}V_{s,3}(t)$ (10.39)
$t \geq \tau_{sat}$	$V_o(t) = K_1 e^{-\frac{\beta_5 t}{2}} + K_2 e^{-\frac{\beta_6 t}{2}}$ (10.40) $B_3 = \frac{mR_{V_{ss}}C_L + R_{V_{ss}}C_{V_{ss}} + \frac{C_L(1+R_L\gamma_n)}{\gamma_n}}{R_{V_{ss}}C_{V_{ss}}\frac{C_L(1+R_L\gamma_n)}{\gamma_n} + mL_{V_{ss}}C_L + L_{VSS}C_{V_{ss}}}$ (10.41) $B_4 = \frac{1}{R_{V_{ss}}C_{V_{ss}}\frac{C_L(1+R_L\gamma_n)}{\gamma_n} + mL_{V_{ss}}C_L + L_{VSS}C_{V_{ss}}}$ (10.42) $\beta_5 = B_3 + \sqrt{B_3^2 - 4B_4}$ (10.43) $\beta_6 = B_3 - \sqrt{B_3^2 - 4B_4}$ (10.44)

For a resistive-capacitive load, $B_3^2 - 4B_4$ can be expressed as

$$B_3^2 - 4B_4 = (mR_{V_{ss}}C_L + R_{V_{ss}}C_{V_{ss}} + \frac{C_L(1+R_L\gamma_n)}{\gamma_n})^2 - 4(R_{V_{ss}}C_{V_{ss}}\frac{C_L(1+R_L\gamma_n)}{\gamma_n} + mL_{V_{ss}}C_L + L_{Vss}C_{V_{ss}}). \quad (10.45)$$

If $B_3^2 - 4B_4$ is less than zero, the critical value of the parasitic inductance defined in (10.23) becomes

$$L_{V_{ss}} > \frac{(mR_{V_{ss}}C_L + R_{V_{ss}}C_{V_{ss}} + \frac{C_L(1+R_L\gamma_n)}{\gamma_n})^2 - 4R_{V_{ss}}C_{V_{ss}}\frac{C_L(1+R_L\gamma_n)}{\gamma_n}}{4(mC_L + C_{V_{ss}})}. \quad (10.46)$$

The output voltage in this region can be approximated as

$$V_s(t) = V_o(\tau_{sat})e^{-\frac{\beta_3(t-\tau_{sat})}{2}}\frac{cos(\beta_4 t)}{cos(\beta_4\tau_{sat})} \qquad \text{for } t \geq \tau_{sat}, \quad (10.47)$$

where $\beta_3 = B_3$ and $\beta_4 = \sqrt{4B_4 - B_3^2}$.

Based on the same assumption as for a capacitive load, the output voltage in this region can be approximated as

$$V_o(t) = V_o(\tau_{sat})e^{-\frac{\beta_6}{2}(t-\tau_{sat})} \qquad \text{for } t \geq \tau_{sat}. \quad (10.48)$$

If the drain-to-source saturation voltage is greater than $0.5V_{dd}$, the high-to-low propagation delay can be expressed as

$$t_{P_{HL}} = \frac{2}{\beta_6}ln\frac{2V_o(\tau_{sat})}{V_{dd}} + \tau_{sat} - \frac{\tau_r}{2}. \quad (10.49)$$

A comparison of the propagation delay based on these analytical expressions with SPICE is listed in Tables 10.9 and 10.10 for both high-to-low and low-to-high output transitions, respectively. The estimated propagation delay based on these analytical expressions is within 5% of SPICE, while the error of the estimate which does not consider on-chip simultaneous switching noise can reach 18% of SPICE. The average improvement in accuracy is about 10% as compared to SPICE.

Table 10.9: Comparison of high-to-low propagation delay with SPICE of a CMOS inverter driving a resistive-capacitive load including the effect of on-chip simultaneous switching noise

Input Rise Time	Impedance of Ground Rail			Comparison of Propagation Delay				
				Simulation	Analytic Estimation			
τ_r	L	R	C	SPICE	Without SSN		With SSN	
(ps)	(nH)	(Ω)	(pF)	(ps)	(ps)	δ (%)	(ps)	δ (%)
200	1.0	5.0	0.1	163	152	6.7	162	0.6
		10.0	0.1	167	152	9.0	165	1.2
		15.0	0.1	172	152	11.6	168	2.3
		20.0	0.1	176	152	13.6	171	2.8
	2.0	5.0	0.1	167	152	9.0	165	1.2
		10.0	0.1	171	152	11.1	168	1.8
		15.0	0.1	176	152	13.6	171	2.8
		20.0	0.1	180	152	15.6	174	3.3
	3.0	5.0	0.1	172	152	11.6	169	1.7
		10.0	0.1	176	152	13.6	172	2.3
		15.0	0.1	180	152	15.6	175	2.8
		20.0	0.1	184	152	17.4	177	3.8
150	1.0	5.0	0.1	157	146	7.0	156	0.6
		10.0	0.1	162	146	9.9	159	1.9
		15.0	0.1	166	146	12.0	162	2.4
		20.0	0.1	170	146	14.1	165	2.9
	2.0	5.0	0.1	161	146	9.3	159	1.2
		10.0	0.1	165	146	11.5	162	1.8
		15.0	0.1	170	146	14.1	165	2.9
		20.0	0.1	174	146	16.1	168	3.4
	3.0	5.0	0.1	166	146	12.0	162	2.4
		10.0	0.1	170	146	14.1	165	2.9
		15.0	0.1	174	146	16.1	168	3.4
		20.0	0.1	170	146	18.0	170	4.5
Maximum error (%)					18.0		4.5	
Average error (%)					12.6		2.4	

Table 10.10: Comparison of low-to-high propagation delay with SPICE of a CMOS inverter driving a resistive-capacitive load including the effect of on-chip simultaneous switching noise

Input Rise Time	Impedance of V_{dd} Rail			Comparison of Propagation Delay				
				Simulation	Analytic Estimation			
τ_r	L	R	C	SPICE	Without SSN		With SSN	
(ps)	(nH)	(Ω)	(pF)	(ps)	(ps)	δ (%)	(ps)	δ (%)
200	1.0	5.0	0.1	310	304	2.0	311	0.3
		10.0	0.1	319	304	4.7	318	0.3
		15.0	0.1	329	304	7.6	322	2.1
		20.0	0.1	338	304	10.0	328	3.0
	2.0	5.0	0.1	314	304	3.2	314	0.0
		10.0	0.1	323	304	5.9	319	1.2
		15.0	0.1	332	304	8.4	324	2.4
		20.0	0.1	341	304	10.9	329	3.5
	3.0	5.0	0.1	318	304	4.4	316	0.6
		10.0	0.1	327	304	7.0	321	1.8
		15.0	0.1	336	304	9.5	326	3.0
		20.0	0.1	345	304	11.9	330	4.3
150	1.0	5.0	0.1	300	294	2.0	302	0.6
		10.0	0.1	310	294	5.2	307	1.0
		15.0	0.1	319	294	7.8	313	1.9
		20.0	0.1	328	294	10.4	318	3.0
	2.0	5.0	0.1	304	294	3.3	303	0.3
		10.0	0.1	313	294	6.1	309	1.3
		15.0	0.1	323	294	9.0	314	2.8
		20.0	0.1	332	294	11.4	319	3.9
	3.0	5.0	0.1	308	294	4.5	305	1.0
		10.0	0.1	317	294	7.3	310	2.2
		15.0	0.1	326	294	9.8	315	3.4
		20.0	0.1	336	294	12.5	310	4.9
Maximum error (%)					12.5		4.9	
Average error (%)					7.3		2.0	

If on-chip simultaneous switching noise cannot be neglected in VDSM synchronous CMOS integrated circuits, these analytical equations, (10.37) and (10.49), provide system level timing characteristics of a CMOS logic gate driving both a capacitive and a resistive-capacitive load. This timing information can be used to develop guidelines and methodologies for designing tapered buffers and inserting repeaters in order to improve interconnect-based circuit performance.

10.5 Summary

An analytical expression characterizing the simultaneous switching noise voltage in VDSM CMOS circuits is presented in this chapter. This expression provides a method for evaluating simultaneous switching noise voltage at the system level. The analytically derived waveform characterizing the on-chip simultaneous switching noise voltage is quite close to SPICE. The predicted peak on-chip simultaneous switching noise voltage based on the analytical expression is within 10% as compared to SPICE. Circuit- and layout-level design constraints for the power distribution network have also been briefly discussed.

It is necessary to consider on-chip simultaneous switching noise when determining the propagation delay of a CMOS logic gate in a high speed synchronous CMOS integrated circuit. The effect of on-chip simultaneous switching noise on the waveform of the output voltage and the propagation delay of a CMOS logic gate is also discussed. The estimated propagation delay based on these analytical expressions is within 5% as compared to SPICE; the average improvement can reach 10% of SPICE as compared to delay estimates which do not consider on-chip simultaneous switching noise. The analytical expressions presented in this chapter provide an accurate timing model for repeater insertion, tapered buffer

design, and related high performance design techniques for those high speed synchronous CMOS integrated circuits where on-chip simultaneous switching noise cannot be neglected.

Chapter 11

Conclusions

On-chip interconnect noise has been the primary topic addressed in this dissertation and is becoming one of the dominant issues in the design of high speed CMOS integrated circuits. The integration density of CMOS integrated circuits will continue to increase in the next decade. The speed (or operating frequency) of high performance CMOS integrated circuits is now dominated by the on-chip global interconnections. It has become necessary to incorporate on-chip interconnect noise into the overall IC design flow in order to improve circuit design efficiency and reliability. It is, therefore, necessary to consider interconnect impedances when predicting the performance of CMOS integrated circuits.

A variety of interconnect models exist to characterize interconnect impedances. If the interconnect resistance is comparable to the effective output resistance of a CMOS logic gate, the interconnect should be modeled as a resistive load. For short signal transition times and wide interconnect lines, the interconnect should be characterized as an inductive load. A guideline for choosing an appropriate interconnect model has been described in Section 2.3. A single capacitor is no longer sufficiently accurate to model medium and long interconnect.

The process in which interconnect impedances (capacitance, resistance, and inductance) affect the waveform shape of on-chip signals, as well as the timing and power characteristics of a CMOS logic gate driving a resistive and inductive interconnect, has been discussed throughout this dissertation. An efficient lumped (or effective load) impedance model has been presented to characterize distributed interconnect based on a Fourier analysis of an on-chip signal. This analysis includes the frequency dependence of the interconnect impedances.

- On-chip signals can be approximated by a Fourier series up to the 15th harmonic component. The voltage waveform based on an effective load impedance model is similar to distributed interconnect approximated by sections of lumped circuit elements. Analytical expressions characterizing the output voltage and propagation delay of a CMOS logic gate driving an $R(L)C$ load have also been developed based on an effective load impedance model, simplifying the analysis of the circuit behavior of a CMOS logic gate while providing timing guidelines at the system level. The analytical waveforms are quite close to the waveforms derived from SPICE for a fast ramp input signal. The estimated propagation delay is within 7% and 11% as compared to SPICE for a resistive and an inductive load, respectively.

- For a resistive interconnect, the interconnect resistance reduces the time during which the active MOS transistors remain in the saturation region. This effect is called resistive shielding, where a portion of the load capacitance is shielded when the MOS transistors operate in the saturation region. Moreover, the interconnect resistance degrades the waveform shape of the output voltage signal. If the interconnect resistance is similar to the effective output resistance of a CMOS logic gate, the time during which an MOS transistor

operates in the linear region increases by almost 50% as compared to the time of linear operation if the load is primarily capacitive. Therefore, the MOS transistors of the following stage cannot turn off quickly. Additional short-circuit and subthreshold current within the following logic stage can also occur. Therefore, it is important to consider short-circuit power in the analysis of the total transient power consumption when the interconnect is modeled as a resistive-capacitive load.

- Large inductive loads and fast input transition times can result in significant short-circuit currents within the driver stage. The effect of the short-circuit current has been included in the analytical expressions that characterize the output voltage of a CMOS logic gate driving an inductive load. Analytical equations characterizing the short-circuit power have also been developed based on the load conditions and the shape of the input waveform. The waveform of the output voltage based on the analytical equations are quite close to SPICE for fast ramp input signals. The error of the estimated peak short-circuit current is less than 7% as compared to SPICE.

Interconnections in CMOS integrated circuits are conductors deposited on dielectric insulation layers. The fringing electric field and mutual magnetic flux between neighboring interconnect lines result in a coupling capacitance and mutual inductance. Therefore, there are two coupling mechanisms, *i.e.*, capacitive coupling and inductive coupling. Both the coupling capacitance and mutual inductance increase if the spacing between the adjacent interconnect lines is reduced and/or the aspect ratio of the interconnect thickness-to-width is increased.

- The coupling capacitance may become comparable to the line-to-ground interconnect capacitance. Therefore, capacitive coupling has emerged as one

of the primary issues in evaluating the signal integrity of CMOS integrated circuits.

- The importance of interconnect coupling capacitance depends upon the behavior of the CMOS logic gates. If the logic gates driving the coupled interconnections are in transition, the coupling capacitance can affect the propagation delay and the waveform shape of the output voltage signal. If one of these logic gates is in transition and the other logic gate is quiet, the coupling capacitance can not only change the propagation delay of the active logic gate, but can also induce a voltage change at the output of the quiet logic gate. The voltage change may cause extra current to flow through the CMOS logic gate driving the quiet interconnect line, resulting in additional power dissipation. Furthermore, the change in voltage may cause overshoots or undershoots. The overshoots and undershoots may cause carrier injection or collection within the substrate. Also, if the voltage change is greater than the threshold voltage of the following logic gates, circuit malfunctions and excess power dissipation may occur.

- Analytical expressions characterizing the output voltage of each CMOS logic gate driving a coupled capacitive load have been developed. Delay estimates based on the analytical expressions are within 3% as compared to SPICE, while the estimate neglecting the difference between load capacitances for an in-phase, an out-of-phase, and one active transition can reach 48%, 16%, and 12% of SPICE, respectively. The peak noise voltage based on the analytical prediction is within 4% of SPICE.

- A transient analysis of CMOS logic gates driving coupled resistive-capacitive interconnect has been presented for a two-line and three-line coupled system, respectively. Delay estimates based on the analytical expressions are within 10% as compared to SPICE, while the estimates neglecting the nonlinear behavior of a CMOS logic gate for an in-phase, an out-of-phase, and one active transition can reach 50%, 18%, and 16%, respectively, for a two-line coupled system. The peak noise voltage based on the analytical prediction is within 7% and 13% of SPICE for a two-line and three-line coupled system, respectively.

- Delay uncertainty can be minimized or even eliminated when both CMOS logic gates and load capacitances are similar within a coupled system. For example, the coupling capacitance can be eliminated from the effective load capacitance for an in-phase transition. To reduce the propagation delay of a CMOS logic gate in a coupled system, the probability of an out-of-phase transition should be minimized because of the increased effective load capacitance. However, if an out-of-phase transition cannot be avoided, the size of each transistor within a coupled system can be adjusted to optimize the propagation delay within a critical path by "transferring" some signal delay (through the effective capacitance) from one circuit branch to another circuit branch, an "advantage" of coupling capacitances. A proper strategy for adjusting the coupled system depends upon the device parameters, the interconnect structure, and the design target of the various data paths.

- For a two-line coupled system, the coupling noise voltage is proportional to B_{n1}/γ_{n2} (the ratio of the transconductance of the active transistor to the effective output conductance of the quiet transistor) and C_c (the cou-

pling capacitance) as described in Chapters 6 and 7. If the effective output conductance of the quiet transistor is increased, the peak noise voltage can be reduced. This conclusion suggests that the size of the MOS transistors within the quiet logic gate should be increased, contradicting the observation for the propagation delay. Therefore, a tradeoff exists when choosing the appropriate size of the transistors for a capacitively coupled system. The optimal size of these transistors is also related to the signal activity and other circuit constraints.

- Both capacitive coupling and inductive coupling mechanisms can be combined into a general coupled *RLC* transmission line model. Analytical expressions have been derived from time domain differential equations to estimate the coupling noise voltage at both ends of a quiet interconnect line. The accuracy of the predicted peak noise voltage based on the closed form expressions is within 20% of SPICE for the driver end and 15% of SPICE for the receiver end.

- The dependence of the propagation delay of the CMOS driver stage on the driver impedance and the relationship between the relaxation time of the coupling noise voltage and the driver impedance have also been presented. The propagation delay of the driver stage decreases as the driver impedance is reduced. The relaxation time of the coupling noise voltage is minimized when the driver output impedance matches the interconnect impedance. The peak noise at both ends of the quiet interconnect decreases when the driver impedance is increased. Therefore, the driver impedance should be determined from the specific design target in terms of the speed and noise constraints.

Power distribution networks in high complexity CMOS integrated circuits must be able to provide sufficient current to support an average and peak power demand within all parts of an integrated circuit. The large dimensions and average currents require special design strategies to maintain a constant voltage supply within the power distribution networks. Moreover, decreased power supply levels reduce the tolerance to voltage changes within the CMOS-based power distribution networks.

- Due to the lossy characteristics of the metal interconnections in CMOS integrated circuits, transient *IR* voltage drops within a power distribution network are no longer negligible. Analytical expressions characterizing these transient *IR* voltage drops have been developed. The peak *IR* voltage drops occur when the input signal completes a transition (for a fast ramp input signal). The peak value of the transient *IR* voltage drops based on the analytical expression is within 6% as compared to SPICE.

- Analytical expressions characterizing the output voltage and propagation delay of a CMOS logic gate have also been presented for a capacitive and a resistive-capacitive load, respectively, including the effects of transient *IR* voltage drops. The propagation delay model based on the analytical expressions is within 5% of SPICE while the delay model without considering transient *IR* voltage drops can reach 20% as compared to SPICE for a 20 Ω power line. Circuit- and layout-level design constraints have also been addressed to manage the maximum value of the transient *IR* voltage drops, providing guidelines for the design of on-chip power distribution networks.

- Due to the on-chip parasitic inductance inherent to the power distribution network, fast current surges result in voltage fluctuations in the power distribution network. Simultaneous switching noise originating from the internal

circuitry is becoming an important issue in the design of very deep submicrometer (VDSM) high performance integrated circuits. This increased importance can be attributed to faster clock rates, large on-chip switching activities, and large on-chip currents, all of which are increasingly common characteristics of a VDSM synchronous integrated circuit.

- An analytical expression characterizing on-chip simultaneous switching noise voltage in VDSM CMOS integrated circuits has been developed. This expression provides a method for evaluating simultaneous switching noise voltages at the system level. The analytically derived waveform characterizing the on-chip simultaneous switching noise voltage is quite close to SPICE. The predicted peak on-chip simultaneous switching noise voltage based on the analytical expression is within 10% as compared to SPICE. Circuit- and layout-level design constraints to manage the peak on-chip simultaneous switching noise have also been developed.

- The effects of on-chip simultaneous switching noise on the waveform shape of the output voltage signal and the propagation delay of a CMOS logic gate have been discussed. The estimated propagation delay based on the proposed delay model is within 5% as compared to SPICE; the average improvement can reach 10% as compared to delay estimates which do not consider on-chip simultaneous switching noise. The proposed delay model provides an accurate timing framework for repeater insertion, tapered buffer design, and related high performance design techniques for those high speed synchronous CMOS integrated circuits where on-chip simultaneous switching noise cannot be neglected.

Summarizing, the research presented in this dissertation provides a capability for estimating on-chip interconnect noise at the system (or chip) level, permitting interconnect-based design strategies and related design methodologies to be developed that reduce on-chip interconnect noise in CMOS integrated circuits. Multiple electrical and physical issues, inherent to high speed VDSM technologies, have also been considered in this dissertation. The primary overall goal of this dissertation is to develop the specific methodologies, techniques, and strategies for designing modern CMOS integrated circuits in order to both reduce and compensate for on-chip interconnect noise, thereby providing a high performance design capability with improved signal integrity.

Chapter 12

Future Work

Signal integrity has become a dominant concern in the design of high performance integrated circuits. As operating frequencies exceed a gigahertz, noise originating from the on-chip interconnect has begun to limit circuit performance. The challenge of managing signal integrity strongly affects the integrated circuit design process. Furthermore, currently on-chip interconnect noise is detected only after the physical layout has been completed, expending significant manpower, money, and time.

The effects of interconnect resistance and inductance on the waveform shape of on-chip signals, electromagnetically coupled interconnect, and voltage fluctuations in power distribution networks have been discussed in this dissertation. Design guidelines have also been developed to manage the peak noise caused by on-chip interconnect. The primary objective of this dissertation is to enhance signal integrity in high speed VDSM CMOS integrated circuits and incorporate noise estimation techniques into existing optimization algorithms to estimate circuit performance at the system level. In order to provide an overall capability for estimating noise at the system (or chip) level, interconnect design strategies need to be developed that reduce noise in integrated circuits. Multiple electrical and

physical issues, inherent to modern high speed VDSM technologies, will need to be considered in the future.

12.1 Modeling of Interconnect Impedances Based on Geometric Layout Parameters

The waveform shape of on-chip signals is a function of the interconnect impedances (capacitance, resistance, and inductance) [125, 126],

$$V = V(R, L, C), \tag{12.1}$$

where R, L, and C are the interconnect resistance, inductance, and capacitance, respectively. Interconnections in CMOS integrated circuits, however, are multi-conductor lines existing on different physical planes. The parasitic capacitance, resistance, and inductance of the conductor lines can be determined from the geometric parameters of the on-chip interconnections, as shown in Figure 12.1 [127, 128].

The interconnect impedances can be characterized as

$$R = R(l_{int}, W_{int}, H_{int}) = \rho \frac{l_{int}}{W_{int} H_{int}}, \tag{12.2}$$

$$C = C(l_{int}, W_{int}, H_{int}, S_{int}, t_{ox}), \tag{12.3}$$

$$C_c = C(l_{int}, W_{int}, H_{int}, S_{int}, t_{ox}), \tag{12.4}$$

$$L = L(l_{int}, W_{int}, H_{int}, S_{int}, t_{ox}), \tag{12.5}$$

$$L_m = L(l_{int}, W_{int}, H_{int}, S_{int}, t_{ox}), \tag{12.6}$$

where C_c and L_m are the coupling capacitance and mutual inductance between adjacent lines, respectively. W_{int} is the width, H_{int} is the thickness, and l_{int} is the length of the interconnect line. S_{int} is the spacing between adjacent interconnect

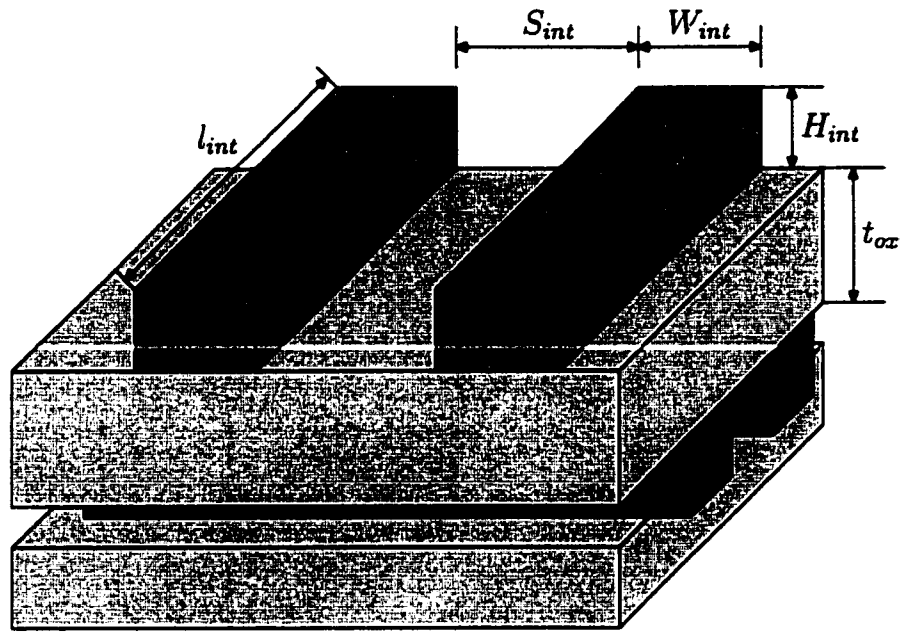


Figure 12.1: Geometric parameters of interconnect lines

lines. t_{ox} is the thickness of the insulation field layer. ρ is the resistivity of the interconnect. In terms of extracting on-chip interconnect impedances [127, 128], interconnect resistance is relatively simple to determine based on the structure of the on-chip interconnections [59]. However, significant research is required to extract and model on-chip capacitances and, particularly, inductances based on physical geometric information [129–134].

12.1.1 Compact Model of On-chip Inductance Including Current Return Path

Inductance extraction is notoriously difficult because the inductive current path depends upon characteristics of the silicon substrate, the layout of the power distribution network, the structure of adjacent interconnect lines, and other "non-local" factors [135, 136]. It is extremely difficult to develop a general solution by

considering all of these factors [137, 138]. However, if the physical structure of the on-chip interconnections is completely specified, the interconnect inductance can be determined by solving three-dimensional field equations using a full wave analysis or other numerical analyses, such as Monte Carlo techniques [139–141]. Based on these numerical results, a curve fitting technique can be applied to develop a reasonably accurate compact model of on-chip inductive interconnect impedances.

An alternative method is to consider the silicon substrate to behave as an ideal ground plane. The signal propagation along an interconnect line can be approximated as a TEM or quasi-TEM wave as shown in Figure 12.2. The parasitic inductance of the interconnect line per unit length can be determined from (12.7),

$$L = \frac{\mu \int_s \vec{H} d\hat{s}}{\oint_c \vec{H} d\hat{l}}, \tag{12.7}$$

where μ is the permeability of the dielectric. The inductance derived from (12.7) can be modified by considering the effect of the silicon substrate [142].

12.1.2 Design Guidelines to Optimize Physical Layout

If a compact model of interconnect inductance is available, the signal waveform described by (12.1) will become

$$V = V(R, L, C) = V(l_{int}, W_{int}, H_{int}, S_{int}, t_{ox}). \tag{12.8}$$

Therefore, the waveform shape of on-chip signals can be described as a function of geometric layout parameters of the on-chip interconnections [143–145]. Based on (12.8), the peak interconnect noise can be determined based on the geometric structure of the on-chip interconnections. Layout constraints and design guidelines can be developed to maintain specific circuit functions [146, 147]. These

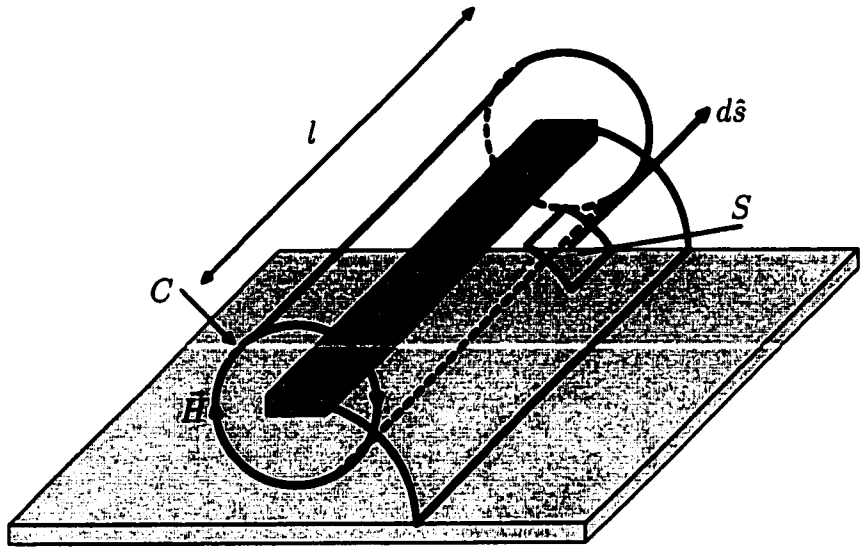


Figure 12.2: Parasitic inductance of an on-chip interconnect line

constraints and guidelines can be incorporated into an electrical rule checking capability in order to minimize the effects of crosstalk between interconnect [148].

12.2 An Overall DFN Capability for High Speed Integrated Circuits

The research directions discussed in the previous section focus on the physical layout level in the design hierarchy of integrated circuits. Another important research objective is to incorporate noise information into higher design levels (such as the logic level or even register transfer level – RTL) within the design hierarchy.

12.2.1 Conditions of Circuit Failure Due to Interconnect Effects

The concept of *interconnect effects* includes the effects of electromagnetically coupled interconnect and voltage fluctuations in power distribution networks. It has been described in this dissertation that the effects of interconnect coupling depends upon the geometric size of the transistors and the signal activity among coupled systems. If the CMOS logic gates driving the coupled interconnections are in transition, the coupling capacitance and mutual inductance can change the effective load impedances, thereby affecting the propagation delay and the waveform shape of the output voltage signal, creating delay uncertainty within the data and clock paths [149–151]. Moreover, fast clock signal transition times make it difficult to satisfy clock skew requirements in high performance integrated circuits. Therefore, special design techniques are required to implement high speed clock distribution networks, which can lead to multiple redesign efforts.

Furthermore, the voltage change on a quiet interconnect line may cause overshoots or undershoots. The overshoots and undershoots may cause carrier injection or collection within the substrate, degrading the logic states in a dynamic logic circuit. Moreover, if the voltage change is greater than the threshold voltage of the following logic gates, circuit malfunctions and excess power dissipation may occur. These deleterious effects caused by coupling noise voltages become aggravated as the relaxation time, the time for the coupling noise to reach a steady state voltage, increases.

Voltage fluctuations in power distribution networks affect the signal delay, creating delay uncertainty since the power supply level temporally changes the local drive current. Furthermore, logic malfunctions may be created and excess

power may be dissipated due to faulty switching if the power supply fluctuations are sufficiently large.

Therefore, it is important to identify these interconnect related circuit failures at the early stage of the integrated circuit design process [105, 152–154]. A significant improvement in the existing capability for estimating on-chip interconnect noise is necessary in order to be able to design circuit blocks composed of millions of high speed transistors [155, 156].

12.2.2 A Unified Algorithm to Estimate Interconnect Noise

Although different noise sources, *e.g.*, interconnect impedances, electromagnetically coupled interconnect, and voltage fluctuations in power distribution networks, have been independently addressed in this dissertation, these noise sources are actually related. The power distribution network is interconnect based since power buss lines are conductors on physical planes. Moreover, the structure of the on-chip power distribution network can affect the interconnect coupling capacitance, changing the ratio of the fringing electrical field flux to the line-to-ground electrical field flux [157, 158]. Furthermore, the inductive return paths are often through power distribution networks, making the layout and location of the power distribution network relative to the high speed data paths of significant importance.

One possible future research topic is to integrate all of these noise mechanisms into a unified design capability for estimating interconnect related noise at the system level. Because the device and interconnect parameters are dependent upon low level physical structures, a bottom-up research strategy will be necessary in the analysis of system level signal integrity. The computational complexity of this problem is a significant issue, requiring efficient and accurate expressions for

modeling these interconnect effects. A second future topic is to integrate this unified noise capability into various circuit optimization strategies. Examples of circuit optimization strategies include clock skew scheduling [159], clock tree synthesis [67, 116], and retiming [160], permitting signal integrity to be incorporated into a variety of system level synthesis tools.

12.3 Design Guidelines for the Power Grids

Optimizing the power distribution network is necessary in order to reduce the effects of both on-chip/off-chip simultaneous switching noise and transient *IR* voltage drops [161, 162]. Certain layout guidelines have been presented to control the maximum length of a power supply rail in order to suppress the peak simultaneous switching noise and transient *IR* voltage drops. However, if the power distribution network is structured as a mesh rather than as an interleaved combed structure, it is necessary to determined the size of the power grids based on the guidelines presented in Chapters 9 and 10.

A power distribution network structured as a mesh is shown in Figure 12.3. The effective impedance of the power supply rail connected to a CMOS logic gate is

$$R = R(x, y, g, w), \tag{12.9}$$

$$C = C(x, y, g, w), \tag{12.10}$$

$$L = L(x, y, g, w), \tag{12.11}$$

where x and y characterize the location of the CMOS logic gate, g is the size of the mesh, and w is the line width of the power supply rail. The parameters defined in (12.9), (12.10), and (12.11) can be determined by impedance extraction

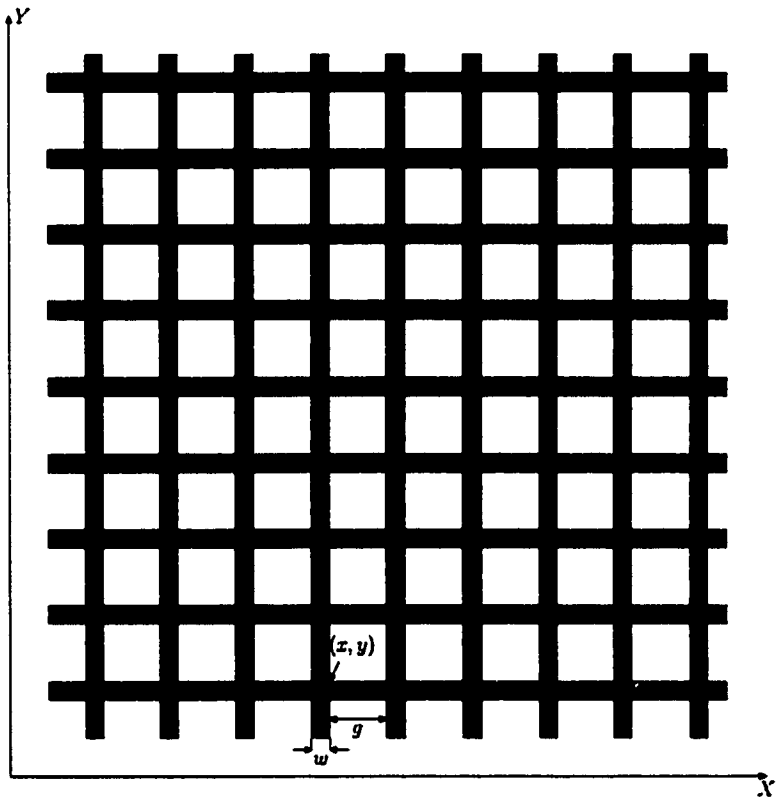


Figure 12.3: A mesh structure of the power distribution network

techniques as discussed in Section 12.1. Therefore, the effective load impedance of the mesh structure can be incorporated into the design guidelines developed in Chapters 9 and 10 to determine the optimal size of the mesh and the optimal width of the power supply rail.

12.4 Novel Circuit Structures with High Noise Immunity

New circuit structures will be required to increase circuit noise immunity. The far end (or receiver end) coupling noise voltage can cause logic malfunctions if the peak noise is greater than the logic threshold. One proposed technique is to increase the switching threshold of the receiver stage by using novel circuit structures. A Schmitt trigger structure [55], which has different switching thresholds for positive- and negative-transitioning input signals, is one effective technique to increase signal noise immunity. A Schmitt trigger structure can convert a noisy or slowly varying input signal into a low noise digital output signal [33, 163].

In order to minimize on-chip simultaneous switching noise, on-chip decoupling capacitors are often required [164–168]. One solution for creating an on-chip decoupling capacitor is to exploit the top metal layer in order to form an on-chip parasitic decoupling capacitance.

12.5 Techniques to Minimize On-chip Interconnect Noise

On-chip interconnect noise can cause circuit malfunctions, dissipate extract power, affect signal quality, and degrade long term reliability. If the on-chip interconnect noise is sufficiently large, design strategies must be modified to mitigate

the effects of the interconnect noise [93]. A potentially important focus of future research is to develop circuit and layout techniques that reduce the effects of on-chip interconnect noise. An advantage of the bottom-up approach presented in this dissertation is that the device and interconnect models are based on physical parameters. Close form design expressions based on the physical behavior can therefore be applied in the development of layout and circuit techniques that reduce the effects of on-chip interconnect noise. Some projected layout and circuit techniques are discussed below.

12.5.1 Layout-Level Techniques

Certain layout routing techniques could be developed to reduce the length of neighboring parallel interconnect. By reordering the conductor lines, the effective coupling factors can be reduced [169–171]. More accurate analytical models of on-chip parasitic capacitances and inductances are necessary at the system level, permitting these models to be embedded into electrical verification tools, as discussed in Section 12.2.2.

A layout strategy could also be developed to eliminate the data corrupted by the minority carrier injection process. A diffusion collector, tied to a power rail, can be placed between the injector and the dynamic node to collect the injected minority carriers. By redistributing the V_{DD}/V_{SS} lines, a metal layer can be used as a reference V_{DD}/V_{SS} plane. The additional ground plane will reduce the coupling noise voltage and current density between adjacent interconnect lines, thereby reducing on-chip simultaneous switching noise.

12.5.2 Circuit-Level Techniques

Repeater insertion is another important circuit technique that can be used to improve signal integrity and reduce coupling noise voltages [172, 173]. The inserted repeaters reduce the coupling between adjacent parallel interconnections, resulting in a decrease in the peak noise voltage. The peak noise voltage is proportional to a coupling factor m_c. For example, the coupling factor with no inserted repeaters $m_{c_{norep}}$

$$m_{c_{norep}} = \frac{C_c}{C_{int} + C_{gate} + C_c}, \tag{12.12}$$

where C_c is the coupling capacitance, C_{int} is the self-interconnect capacitance, and C_{gate} is the gate capacitance of the following logic stage. Assuming a CMOS inverter is inserted in the middle of an interconnect line with the gate capacitance equal to C_{gate}, the coupling factor with inserted repeaters $m_{c_{rep}}$

$$m_{c_{rep}} = \frac{\frac{C_c}{2}}{\frac{C_{int}}{2} + C_{gate} + \frac{C_c}{2}} = \frac{C_c}{C_{int} + 2C_{gate} + C_c} < m_{c_{norep}}. \tag{12.13}$$

Therefore, by inserting repeaters, the coupling factor is reduced. Another advantage of inserting repeater is that the signal distortion caused by long resistive interconnect is minimized.

12.6 Summary

On-chip interconnect noise has become an increasing challenge in the design of high performance integrated circuits. This trend is due to four principle reasons: increasing interconnect densities, faster clock rates, more aggressive use of dynamic logic circuits, and scaling of device threshold voltages. Signal integrity has therefore become a metric of comparable importance to speed, power, and

area in designing CMOS integrated circuits. The most effective strategy for managing signal integrity is the application of physical design synthesis - from the gate level to the physical layout level. Once signal integrity is automated in the design process, design efficiency and circuit performance will be significantly improved.

Bibliography

[1] Semiconductor Industry Association, "The National Technology Roadmap for Semiconductors," 1997.

[2] G. E. Moore, "Progress in Digital Integrated Circuits," *Proceedings of the IEEE International Electron Devices Meeting*, pp. 11–14, December 1975.

[3] C. S. Chang, "Electrical Design of Signal Lines for Multilayer Printed Circuit Boards," *IBM Journal of Research and Development*, Vol. 32, No. 5, pp. 647–657, September 1988.

[4] A. I. Kayssi and K. A. Sakallah, "Delay Macromodels for Point-to-Point MCM Interconnections," *IEEE Transactions on Components, Packaging, and Manufacturing Technology-Part B*, Vol. 17, No. 2, pp. 147–152, May 1994.

[5] J. Peeters and E. Beyne, "Broadband Modeling and Transient Analysis of MCM Interconnections," *IEEE Transactions on Components, Packaging, and Manufacturing Technology-Part B*, Vol. 17, No. 2, pp. 153–159, May 1994.

[6] E. E. Davidson, "Large Chip vs. MCM for a High-Performance System," *IEEE Micro - Chips, Systems, Software, and Applications*, Vol. 18, No. 4, pp. 33–41, July-August 1998.

[7] Semiconductor Industry Association, "The National Technology Roadmap for Semiconductor," 1994.

[8] B. Davari, R. H. Dennard, and G. G. Shahidi, "CMOS Scaling for High Performance and Low Power-The Next Ten Years," *Proceedings of the IEEE*, Vol. 83, pp. 595–606, April 1995.

[9] D. Sylvester and K. Keutzer, "Getting to the Bottom of Deep Submicron," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 203–211, November 1998.

[10] J. A. Davis, V. K. De, and J. D. Meindl, "A Stochastic Wire-Length Distribution for Gigascale Integration (GSI) - Part I: Derivation and Validation," *IEEE Transactions on Electron Devices*, Vol. 45, No. 3, pp. 580–589, March 1998.

[11] J. A. Davis, V. K. De, and J. D. Meindl, "A Stochastic Wire-Length Distribution for Gigascale Integration (GSI) - Part II: Application to Clock Frequency, Power Dissipation, and Chip Size Estimation," *IEEE Transactions on Electron Devices*, Vol. 45, No. 3, pp. 590–597, March 1998.

[12] H. P. Hofstee *et al.*, "Designing for a Gigahertz," *IEEE Micro - Chips, Systems, Software, and Applications*, Vol. 18, No. 3, pp. 66–74, May-June 1998.

[13] H. Iwai, "CMOS Technology—Year 2010 and Beyond," *IEEE Journal of Solid-State Circuits*, Vol. SC-34, No. 4, pp. 357–366, March 1999.

[14] H. B. Bakoglu and J. D. Meindl, "Optimal Interconnection Circuits for VLSI," *IEEE Transactions on Electron Devices*, Vol. ED-32, No. 5, pp. 903–909, May 1985.

[15] H. B. Bakoglu, *Circuits, Interconnections, and Packaging for VLSI.* Addison-Wesley Publishing Company, 1990.

[16] D. Sylvester and K. Keutzer, "A Global Wiring Paradigm for Deep Submicron Design," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. CAD-19, No. 2, pp. 242–252, February 2000.

[17] D. W. Dobberpuhl *et al.*, "A 200-MHz 64-bit Dual-Issue CMOS Microprocessor," *IEEE Journal of Solid-State Circuits*, Vol. SC–27, No. 11, pp. 1555–1565, November 1992.

[18] W. J. Bowhill *et al.*, "Circuit Implementation of a 300-MHz 64-bit Second-Generation CMOS Alpha CPU," *Digital Technical Journal*, Vol. 7, No. 1, pp. 100–118, 1995.

[19] P. E. Gronowski *et al.*, "High-Performance Microprocessor Design," *IEEE Journal of Solid-State Circuits*, Vol. SC-33, No. 5, pp. 676–686, May 1998.

[20] D. W. Bailey and B. J. Benschneider, "Clocking Design and Analysis for a 600-MHz Alpha Microprocessor," *IEEE Journal of Solid-State Circuits*, Vol. SC-33, No. 11, pp. 1627–1633, November 1998.

[21] D. B. Jarvis, "The Effects of Interconnections on High-Speed Logic Circuits," *IEEE Transactions on Electronics Computers*, Vol. EC-12, No. 10, pp. 476–487, October 1963.

[22] K. Lee, "On-Chip Interconnects-Gigahertz and Beyond," *Solid State Technology*, No. 85-89, September 1998.

[23] M. Shoji, *Theory of CMOS Digital Circuits and Circuit Failures.* Princeton University Press, Princeton, New Jersey, 1992.

[24] SRC, "SRC Physical Design Top Ten Problem," Technical Report, SRC Physical Design Task Force, Semiconductor Research Corporation, November 1998.

[25] SRC, "Design Sciences TAB: Physical Design Task Force Report," Technical Report, Semiconductor Research Corporation Physical Design Task Force, Semiconductor Research Corporation, April 1997.

[26] I. Catt, "Crosstalk (Noise) in Digital Systems," *IEEE Transactions on Electronic Computers*, Vol. EC-16, No. 6, pp. 743–763, December 1967.

[27] L. Gal, "On-Chip Crosstalk-the New Signal Integrity Challenge," *Proceedings of the IEEE Custom Integrated Circuit Conference*, pp. 12.1.1–12.1.4, May 1995.

[28] S. Bothra, B. Rogers, M. Kellam, and C. M. Osburn, "Analysis of the Effects of Scaling on Interconnect Delay in ULSI Circuits," *IEEE Transactions on Electron Devices*, Vol. ED-40, No. 3, pp. 591–597, March 1993.

[29] T.-C. Lee and J. Cong, "The New Line in IC Design," *IEEE Spectrum*, pp. 52–58, March 1997.

[30] J. McLeod, "Fab and Silicon Performance," *Integrated System Design*, pp. 27–34, August 1996.

[31] J. T. Wallmark, "Noise Spikes in Digital VLSI Circuits," *IEEE Transactions on Electron Devices*, Vol. ED-29, No. 3, pp. 451–458, March 1982.

[32] J. R. Hauser, "Noise Margin Criteria for a Digital Logic Circuit," *IEEE Transactions on Education*, Vol. 36, No. 4, pp. 363–368, November 1993.

[33] J. M. Rabaey, *Digital Integrated Circuits: A Design Perspective.* Prentice Hall, Inc., 1995.

[34] R. Patton, "The War on Noise: New Tools Needed to Attack the Noise Problem in Deep-Submicron Design," *Electronics Journal*, pp. 14–17, October 1998.

[35] K. Yamashita and S. Odanaka, "Interconnect Scaling Scenario Using a Chip Level Interconnect Model," *IEEE Transactions on Electron Devices*, Vol. 47, No. 1, pp. 90–96, January 2000.

[36] M. B. Anand, H. Shibata, and M. Kakumu, "Optimization Study of VLSI Interconnect Parameters," *IEEE Transactions on Electron Devices*, Vol. 47, No. 1, pp. 178–186, January 2000.

[37] H. R. Shah, "Signal Integrity: Tools Issue, or Methodology Issue," *Computer Design*, pp. 36–36, June 1997.

[38] C. H. Small, "Achieving Signal Integrity Demands Rethinking the Design Process," *Computer Design*, pp. 34–40, June 1997.

[39] H. Johnson, "Planning for Signal Integrity," *Electronics Design*, pp. 135–136, May 1997.

[40] R. Ho, K. Mai, H. Kapadia, and M. Horowitz, "Interconnect Scaling Implication for CAD," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 425–429, November 1999.

[41] T. Sakurai and A. R. Newton, "A Simple MOSFET Model for Circuit Analysis," *IEEE Transactions on Electron Devices*, Vol. ED-38, No. 4, pp. 887–894, April 1991.

[42] S. M. Sze, *Physics of Semiconductor Devices.* Second edition, New York, NY:Wiley, 1981.

[43] Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Figures of Merit to Characterize the Importance of On-Chip Inductance," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 560–565, June 1998.

[44] D. A. Priore, "Inductance on Silicon for Sub-Micron CMOS VLSI," *Proceedings of the IEEE Symposium on VLSI Circuits*, pp. 17–18, May 1993.

[45] F. Moll, M. Roca, and A. Rubio, "Inductance in VLSI Interconnection Modeling," *IEE Proceedings-Circuits, Devices, and Systems*, Vol. 145, No. 3, pp. 176–179, June 1998.

[46] H. Shichman and D. A. Hodges, "Modeling and Simulation of Insulated-Gate Field-Effect Transistor Switching Circuit," *IEEE Journal of Solid-State Circuits*, Vol. SC-3, No. 3, pp. 285–289, September 1968.

[47] L. Bisdounis, S. Nikolaidis, and O. Koufopavou, "Propagation Delay and Short-Circuit Power Dissipation Modeling of the CMOS Inverter," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. 45, No. 3, pp. 259–270, March 1998.

[48] A. I. Kayssi, K. A. Sakallah, and T. M. Burks, "Analytical Transient Response of CMOS Inverters," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. 39, No. 1, pp. 35–42, January 1992.

[49] T. Quarles, A. R. Newton, D. O. Pederson, and A. Sangiovanni-Vincentelli, *SPICE 3B1 User's Guide.* EECS, University of California, Berkeley, 1988.

[50] B. J. Sheu, D. L. Scharfetter, and P. K. Ko, "SPICE2 Implementation of BSIM," ERL Memo ERL 85/42, Electronics Research Laboratory, University of California, Berkeley, May 1985.

[51] Meta-Software, Inc., *HSPICE User's Manual Version 96.1*, 1996.

[52] T. Sakurai and A. R. Newton, "Alpha-Power Law MOSFET Model and Its Application to CMOS Inverter Delay and Other Formulas," *IEEE Journal of Solid-State Circuits*, Vol. SC-25, No. 2, pp. 584–589, April 1990.

[53] W. S. Song and L. A. Glasser, "Power Distribution Techniques for VLSI Circuits," *IEEE Journal of Solid-State Circuits*, Vol. SC-21, No. 1, pp. 150–156, February 1986.

[54] K. Chen and C. Hu, "Performance and V_{dd} Scaling in Deep Submicrometer CMOS," *IEEE Journal of Solid-State Circuits*, Vol. SC-33, No. 10, pp. 1586–1589, October 1998.

[55] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design.* McGraw-Hill Inc., 1996.

[56] P. Larson and C. Svensson, "Noise in Digital Dynamic CMOS Circuits," *IEEE Solid-State Circuits*, Vol. SC-29, No. 6, pp. 655–662, June 1994.

[57] T. Sakurai and K. Tamaru, "Simple Formulas for Two- and Three-Dimensional Capacitances," *IEEE Transactions on Electron Devices*, Vol. ED-30, No. 2, pp. 183–185, February 1983.

[58] J.-H. Chern *et al.*, "Multilevel Metal Capacitance Models for CAD Design Synthesis Systems," *IEEE Electron Device Letters*, Vol. 13, No. 1, pp. 32–34, January 1992.

[59] M. Horowitz and R. W. Dutton, "Resistance Extraction from Mask Layout Data," *IEEE Transaction on Computer-Aided Design on Integrated Circuits and System*, Vol. CAD-2, No. 3, pp. 145–150, July 1983.

[60] N. Delorme, M. Belleville, and J. Chilo, "Inductance and Capacitance Formulas for VLSI Interconnects," *IEE Electronics Letters*, Vol. 32, No. 5, pp. 996–997, May 1996.

[61] M. Gilligan and S. Gupta, "A Methodology for Estimating Interconnect Capacitance for Signal Propagation Delay in VLSIs," *Microelectronics Journal*, Vol. 26, No. 4, pp. 327–336, May 1995.

[62] S. Wong *et al.*, "Interconnect Capacitance Models for VLSI Circuits," *Solid-State Electronics*, Vol. 42, No. 6, pp. 969–977, June 1998.

[63] A. Deutsch *et al.*, "Modeling and Characterization of Long On-Chip Interconnections for High-Performance Microprocessors," *IBM Journal of Research and Development*, Vol. 39, No. 5, pp. 547–567, September 1995.

[64] A. Deutsch *et al.*, "When are Transmission-Line Effects Important for On-Chip Interconnections," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 45, No. 10, pp. 1836–1846, October 1997.

[65] S. Voranantakul, J. L. Prince, and P. Hsu, "Crosstalk Analysis for High-Speed Pulse Propagation in Lossy Electrical Interconnections," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, Vol. 16, No. 1, pp. 127–136, February 1993.

[66] R. Senthinathan and J. L. Prince, "Application Specific CMOS Output Driver Circuit Design Techniques to Reduce Simultaneous Switching Noise," *IEEE Journal of Solid-State Circuit*, Vol. SC-28, No. 12, pp. 1383–1388, December 1993.

[67] E. G. Friedman, *Clock Distribution Networks in VLSI Circuits and Systems.* IEEE Press, 1995.

[68] H. J. M. Veendrick, "Short-Circuit Dissipation of Static CMOS Circuitry and Its Impact on the Design of Buffer Circuits," *IEEE Journal of Solid-State Circuits*, Vol. SC-19, No. 4, pp. 468–473, August 1984.

[69] N. Hedenstierna and K. O. Jeppson, "CMOS Circuits Speed and Buffer Optimization," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. CAD-6, No. 2, pp. 270–280, March 1987.

[70] T. Sakurai and A. R. Newton, "Delay Analysis of Series-Connected MOSFET Circuits," *IEEE Journal of Solid-State Circuits*, Vol. SC-26, No. 2, pp. 122–131, February 1991.

[71] A. Hirata, H. Onodera, and K. Tamaru, "Estimation of Propagation Delay Considering Short-Circuit Current for Static CMOS gates," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. 45, No. 11, pp. 1194–1198, November 1998.

[72] S. Dutta, S. S. M. Shetti, and S. L. Lusky, "A Comprehensive Delay Model for CMOS Inverters," *IEEE Journal of Solid-State Circuits*, Vol. SC-30, No. 8, pp. 864–871, August 1995.

[73] J. M. Daga and D. Auvergne, "A Comprehensive Delay Macro Modeling for Submicrometer CMOS Logics," *IEEE Journal of Solid-State Circuits*, Vol. SC-34, No. 1, pp. 42–55, January 1999.

[74] T. Sakurai, "Approximation of Wiring Delay in MOSFET LSI," *IEEE Journal of Solid-State Circuits*, Vol. SC-18, No. 4, pp. 418–426, August 1983.

[75] R. J. Antinone and G. W. Brown, "The Modeling of Resistive Interconnects for Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. SC-18, No. 3, pp. 200–203, April 1983.

[76] V. Adler and E. G. Friedman, "Repeater Design to Reduce Delay and Power in Resistive Interconnect," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Vol. 45, No. 5, pp. 607–616, May 1998.

[77] V. Adler and E. G. Friedman, "Delay and Power Expressions for a CMOS Inverter Driving a Resistive-Capacitive Load," *Analog Integrated Circuits and Signal Processing*, Vol. 14, No. 1/2, pp. 29–39, September 1997.

[78] T. Sakurai, "Closed-Form Expression for Interconnection Delay, Coupling, and Crosstalk in VLSI's," *IEEE Transactions on Electron Devices*, Vol. ED-40, No. 1, pp. 118–124, January 1993.

[79] J. Qian, S. Pullela, and L. Pillage, "Modeling the 'Effective Capacitance' for the RC Interconnect of CMOS Gates," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. CAD-13, No. 12, pp. 1526–1535, December 1994.

[80] F. Dartu, N. Menezes, and L. T. Pileggi, "Performance Computation for Precharacterized CMOS Gates with *RC* Loads," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. CAD-15, No. 5, pp. 544–553, May 1996.

[81] A. B. Kahng and S. Muddu, "An Analytical Delay Model for *RLC* Interconnects," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 16, No. 12, pp. 1507–1514, December 1997.

[82] M. Shoji, *High-Speed Digital Circuits*. Addison-Wesley Publishing Company, 1996.

[83] K. Nabros, T.-T. Fang, H.-W. Chang, K. S. Kundert, and J. K. White, "Lumped Interconnect Models via Gaussian Quadrature," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 40–45, June 1997.

[84] R. E. Matick, *Transmission Lines for Digital and Communication Networks.* McGraw-Hill Book Company, 1969.

[85] C. Y. Wu and M. Shiau, "Delay Models and Speed Improvement Techniques for RC Tree Interconnections Among Small-Geometry CMOS Inverters," *IEEE Journal of Solid-State Circuits*, Vol. SC-25, No. 10, pp. 1247–1256, October 1990.

[86] S. Dhar and M. A. Franklin, "Optimal Buffer Circuits for Driving Long Uniform Lines," *IEEE Journal of Solid-State Circuits*, Vol. SC-26, No. 1, pp. 32–40, January 1991.

[87] A. M. Hill and S.-M. Kang, "Statistical Estimation of Short-Circuit Power in VLSI Circuits," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 4.105–4.108, May 1996.

[88] V. Adler and E. G. Friedman, "Timing and Power Models for a CMOS Repeater Driving Resistive Interconnect," *Proceedings of the IEEE ASIC Conference*, pp. 201–204, September 1996.

[89] B. M. Ayyub and R. H. McCuen, *Numerical Methods For Engineers.* Upper Saddle River, New Jersey 07548: Prentice Hall, Inc., 1996.

[90] S. R. Vemuru and N. Scheingerg, "Short-Circuit Power Dissipation Estimation for CMOS Logic Gates," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. 41, No. 11, pp. 762–765, November 1994.

[91] Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Dynamic and Short-Circuit Power of CMOS Gates Driving Lossless Transmission Lines," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. 46, No. 8, pp. 950–961, August 1999.

[92] D. Cho, Y. S. Eo, M. Seung, and N. Kim, "Interconnect Capacitance, Crosstalk, and Signal Delay for 0.35 μm CMOS Technology," *Proceedings of the IEEE International Electron Devices Meeting*, pp. 619–622, December 1996.

[93] T. Stohr, H. Alt, A. Hetzel, and J. Koehl, "Analysis, Reduction and Avoidance of Crosstalk on VLSI Chips," *Proceedings of the ACM/IEEE International Symposium on Physical Design*, pp. 211–218, April 1998.

[94] S. M. Sze, *VLSI Technology.* Second edition, New York:McGraw-Hill, 1988.

[95] C. Y. Chang and S. M. Sze, *ULSI Technology.* New York:McGraw-Hill, 1996.

[96] M. Lee, "A Fringing and Coupling Interconnect Line Capacitance Model for VLSI On-Chip Wiring Delay and Crosstalk," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 233–236, May 1996.

[97] E. Barke, "Line-to-Ground Capacitance Calculation for VLSI: A Comparison," *IEEE Transaction on Computer-Aided Design on Integrated Circuits and Systems*, Vol. CAD-17, No. 2, pp. 295–298, February 1998.

[98] K. T. Tang and E. G. Friedman, "Noise Estimation Due To Signal Activity For Capacitively Coupled CMOS Logic Gates," *Proceedings of the IEEE Great Lakes Symposium on VLSI*, pp. 171–176, March 2000.

[99] F. Dartu and L. T. Pileggi, "Calculating Worst-Case Gate Delay due to Dominant Capacitive Coupling," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 46–51, November 1997.

[100] A. Devgan, "Efficient Coupled Noise Estimation for On-chip Interconnects," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 147–153, November 1997.

[101] K. L. Shepard, V. Narayanan, P. C. Elmendorf, and G. Zheng, "GlobalHarmony: Coupled Noise Analysis for Full-Chip *RC* Interconnect Networks," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 139–146, November 1997.

[102] J. Briaire and K. S. Krisch, "Substrate Injection and Crosstalk in CMOS Circuits," *Proceedings of the IEEE Custom Integrated Circuit Conference*, pp. 23.4.1–23.4.4, May 1999.

[103] K. T. Tang and E. G. Friedman, "Interconnect Coupling Noise in CMOS VLSI Circuits," *Proceedings of the ACM/IEEE International Symposium on Physical Design*, pp. 48–53, April 1999.

[104] E. G. Friedman, "Latching Characteristics of a CMOS Bistable Register," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. 40, No. 12, pp. 902–908, December 1993.

[105] A. Rubio, N. Itazaki, X. Xu, and K. Kinoshita, "An Approach to the Analysis and Detection of Crosstalk Faults in Digital VLSI Circuits," *IEEE Transaction on Computer-Aided Design on Integrated Circuits and Systems*, Vol. CAD-13, No. 3, pp. 387–395, March 1994.

[106] A. B. Kahng, S. Muddu, and D. Vidhani, "Noise and Delay Uncertainty Studies for Coupled *RC* Interconnects," *Proceedings of the IEEE International ASIC/SOC Conference*, pp. 3–8, September 1999.

[107] A. Vittal, L. H. Chen, M. Marek-Sadowska, K.-P. Wang, and X. Yang, "Modeling Crosstalk in Resistive VLSI Interconnections," *Proceedings of the IEEE International Conference on VLSI Design*, pp. 470–475, January 1999.

[108] H. Kawaguchi and T. Sakurai, "Delay and Noise Formulas for Capacitively Coupled Distributed *RC* Lines," *Proceedings of the ASP-DAC Asia and South Pacific Design Automation Conference*, pp. 35–43, February 1998.

[109] K. A. Bowman, B. L. Austin, J. C. Eble, X. Tang, and J. D. Meindel, "A Physical Alpha-Power Law MOSFET Model," *IEEE Journal of Solid-State Circuits*, Vol. SC-34, No. 10, pp. 1410–1414, October 1999.

[110] Y. Yang and J. R. Brews, "Crosstalk Estimate for CMOS-Terminated *RLC* Interconnect," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Application*, Vol. 44, No. 1, pp. 82–85, January 1997.

[111] A. R. Djordjević, T. K. Sarkar, and R. F. Harrington, "Time-Domain Response of Multiconductor Transmission Lines," *Proceedings of the IEEE*, Vol. 75, No. 6, pp. 743–764, June 1987.

[112] T. V. Dinh, B. Cabon, and J. Chilo, "SPICE Simulation of Lossy and Coupled Interconnection Lines," *IEEE Transactions on Components, Packaging, and Manufacturing Technology-Part B*, Vol. 17, No. 2, pp. 134–146, May 1994.

[113] C. S. Chang, G. Crowder, and M. McAllister, "Crosstalk in Multilayer Ceramic Packaging," *Proceedings of the IEEE International Symposium on Circuits and Systems*, Vol. 2, pp. 6–11, April 1981.

[114] G. A. Katopis and H. H. Smith, "Coupled Noise Predictors for Lossy Interconnects," *IEEE Transactions on Components, Packaging, and Manufacturing Technology-Part B*, Vol. 17, No. 4, pp. 520–524, November 1994.

[115] Y.-M. Jiang and K.-T. Cheng, "Analysis of Performance Impact Caused by Power Supply Noise in Deep Submicron Devices," *Proceedings of the IEEE/ACM Design Automation Conference*, pp. 760–765, June 1999.

[116] E. G. Friedman, *High Performance Clock Distribution Networks*. Kluwer Academic Publishers, 1997.

[117] G. Katopis, "ΔI Noise Specification for a High Performance Computer Machine," *Proceedings of the IEEE*, Vol. 73, No. 9, pp. 1405–1415, September 1985.

[118] P. Larsson, "*di/dt* Noise in CMOS Integrated Circuits," *Analog Integrated Circuits and Signal Processing*, Vol. 14, No. 1/2, pp. 113–129, September 1997.

[119] A. J. Rainal, "Computing Inductive Noise of CMOS Drivers," *IEEE Transactions on Components, Packaging, and Manufacturing Technology-Part B*, Vol. 19, No. 4, pp. 789–802, November 1996.

[120] A. Vaidyanath, B. Thoroddsen, and J. L. Prince, "Effect of CMOS Driver Loading Conditions on Simultaneous Switching Noise," *IEEE Transactions on Components, Packaging, and Manufacturing Technology-Part B*, Vol. 17, No. 4, pp. 480–485, November 1994.

[121] S. R. Vemuru, "Accurate Simultaneous Switching Noise Estimation Including Velocity-Saturation Effects," *IEEE Transactions on Components, Packaging, and Manufacturing Technology-Part B*, Vol. 19, No. 2, pp. 344–349, May 1996.

[122] Y. Yang and J. R. Brews, "Design for Velocity Saturated, Short-Channel CMOS Drivers with Simultaneous Switching Noise and Switching Time Considerations," *IEEE Journal of Solid-State Circuits*, Vol. SC-31, No. 9, pp. 1357–1361, September 1996.

[123] L.-R. Zheng and H. Tenhunen, "Effective Power and Ground Distribution Scheme for Deep Submicron High Speed VLSI Circuits," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 537–540, May 1999.

[124] S. R. Vemuru, "Effects of Simultaneous Switching Noise on the Tapered Buffer Design," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 5, No. 3, pp. 290–300, September 1997.

[125] R. Gupta, B. Tutuianu, and L. T. Pileggi, "The Elmore Delay as a Bound for *RC* Trees with Generalized Input Signals," *IEEE Transaction on Computer-Aided Design on Integrated Circuits and Systems*, Vol. CAD-16, No. 1, pp. 95–104, January 1997.

[126] Y. I. Ismail and E. G. Friedman, "Equivalent Elmore Delay for *RLC* Tree," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 715–720, June 1999.

[127] K. Nabors and J. White, "FastCap: A Multipole Accelerated 3-D Capacitance Extraction Program," *IEEE Transaction on Computer-Aided Design on Integrated Circuits and Systems*, Vol. CAD-10, No. 11, pp. 1447–1459, November 1991.

[128] M. Kamon, M. Tsuk, and J. White, "FastHenry: A Multipole Accelerated 3-D Inductance Extraction Program," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 42, No. 9, pp. 1750–1758, September 1994.

[129] N. D. Arora, K. V. Raol, R. Schumann, and L. M. Richardson, "Modeling and Extraction of Interconnect Capacitance for Multilayer VLSI Circuits," *IEEE Transaction on Computer-Aided Design on Integrated Circuits and System*, Vol. CAD-15, No. 1, pp. 58–67, January 1996.

[130] S. Kapur and D. E. Long, "IES^2: A Fast Integral Equation Solver for Efficient 3-Dimensional Extraction," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 448–455, November 1997.

[131] J. C. Chen, D. Sylvester, and C. Hu, "An On-chip, Interconnect Capacitance Characterization Method with Sub-Femto-Farad Resolution," *IEEE Transactions on Semiconductor Manufacturing*, Vol. 11, No. 2, pp. 204–210, May 1998.

[132] M. Kamon, N. Marques, Y. Massoud, L. Silveria, and J. White, "Interconnect Analysis: From 3-D Structure to Circuit Models," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 910–914, June 1999.

[133] M. W. Beattie and L. T. Pileggi, "Electromagnetic Parasitic Extraction via a Multipole Method with Hierarchical Refinement," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 437–444, November 1999.

[134] F. Stellari and A. L. Lacaita, "New Formulas of Interconnect Capacitances Based on Results of Conformal Mapping Method," *IEEE Transactions on Electron Devices*, Vol. ED-47, No. 1, pp. 222–231, January 2000.

[135] B. Krauter and S. Mehrotra, "Layout Based Frequency Dependent Inductance and Resistance Extraction for On-chip Interconnect Timing Analysis," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 303–308, June 1998.

[136] K. L. Shpeard and Z. Tian, "Return-Limited Inductances: A Practical Approach to On-Chip Inductance Extraction," *IEEE Transaction on Computer-Aided Design on Integrated Circuits and System*, Vol. CAD-19, No. 4, pp. 425–436, April 2000.

[137] P. Restle, A. Ruehli, and S. G. Walker, "Dealing with Inductance in High-Speed Chip Design," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 904–909, June 1999.

[138] S. V. Morton, "On-chip Inductance Issues in Multiconductor Systems," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 921–926, June 1999.

[139] J. Zhao, W. M. Dai, S. Kapur, and D. E. Long, "Efficient Three-Dimensional Extraction Based on Static and Full-Wave Layered Green's Functions," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 224–229, June 1998.

[140] A. J. Dammers and N. P. van der Meijs, "Virtual Screening: A Step Towards a Sparse Partial Inductance Matrix," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 445–452, November 1999.

[141] J. Wang, J. Tausch, and J. White, "A Wide Frequency Range Surface Integral Formulation for 3-D *RLC* Extraction," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 453–457, November 1999.

[142] X. Qi, B. Kleveland, Z. Yu, S. Wong, and R. Dutton, "On-Chip Inductance Modeling of VLSI Interconnects," *Proceedings of the IEEE International Solid-State Circuits Conference*, Vol. 43, pp. 172–173, February 2000.

[143] J. Cong and D. Z. Pan, "Interconnect Estimation and Planning for Deep Submicron Designs," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 507–510, June 1999.

[144] S. P. Khatri, A. Mehrotra, R. K. Brayton, and A. Sangiovanni-Vincentelli, "A Novel VLSI Layout Fabric for Deep Sub-Micron Applications," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 491–496, June 1999.

[145] M. W. Beattie and L. T. Pileggi, "IC Analysis Including Extracted Inductance Models," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 915–920, June 1999.

[146] H. Zhou and D. F. Wong, "Global Routing with Crosstalk Constraints," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 374–377, June 1998.

[147] Y. Massoud, S. Majors, T. Bustami, and J. White, "Layout Techniques for Minimizing On-Chip Interconnect Self Inductance," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 566–571, June 1998.

[148] K. L. Shepard, "Design Methodologies for Noise in Digital Integrated Circuits," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 94–99, June 1998.

[149] H.-R. Jiang, J.-Y. Jou, and Y.-W. Chang, "Noise-Constrained Performance Optimization by Simultaneous Gate and Wire Sizing Based on Lagrangian Relaxation," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 90–95, June 1999.

[150] J.-S. Yim and C.-M. Kyung, "Reducing Cross-Coupling among Interconnect Wires in Deep-Submicron Datapath Design," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 485–490, June 1999.

[151] S. S. Apatnekar, "Capturing the Effect of Crosstalk on Delay," *Proceedings of IEEE International Conference on VLSI Design*, pp. 364–369, January 2000.

[152] A. Sinha, S. K. Gupta, and M. A. Breuer, "Validation and Test Generation for Oscillatory in VLSI Interconnects," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 289–296, November 1999.

[153] M. Cuviello, S. Dey, X. Bai, and Y. Zhao, "Fault Modeling and Simulation for Crosstalk in System-on-Chip Interconnects," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 297–303, November 1999.

[154] N. NS, F. Cano, D. Young, D. Vohra, and M. Das, "A Practical Approach to Crosstalk Verification of Static CMOS Designs," *Proceedings of IEEE International Conference on VLSI Design*, pp. 370–375, January 2000.

[155] A. R. Conn, R. A. Haring, and C. Visweswariah, "Noise Considerations in Circuit Optimization," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 220–227, November 1998.

[156] J. Cong, L. He, C.-K. Koh, and P. H. Madden, "Performance Optimization of VLSI Interconnect Layout," *Integration - the VLSI Journal*, Vol. 21, No. 1-2, pp. 1–94, November 1996.

[157] H.-P. Tseng, L. Scheffer, and C. Sechen, "Timing and Crosstalk Driven Area Routing," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 378–381, June 1998.

[158] P. Saxena and C. L. Liu, "Crosstalk Minimization Using Wire Perturbations," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 100–103, June 1999.

[159] I. S. Kourtev and E. G. Friedman, *Timing Optimization Through Clock Skew Scheduling*. Norwell, Massachusetts:Kluwer Academic Publishers, 2000.

[160] T. Soyata, E. G. Friedman, and J. H. Mulligan Jr., "Incorporating Interconnect, Register, and Clock Distribution Delays into the Retiming Process," *IEEE Transaction on Computer-Aided Design on Integrated Circuits and System*, Vol. CAD-16, No. 1, pp. 105–120, January 1997.

[161] H. H. Chen, "Minimizing Chip-Level Simultaneous Switching Noise For High-Performance Microprocessor Design," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 544–547, May 1996.

[162] P. Larsson, "Power Supply Noise in Future IC's: A Crystal Ball Telling," *Proceedings of the IEEE Custom Integrated Circuit Conference*, pp. 23.1.1–23.1.8, May 1999.

[163] T. Iima *et al.*, "Capacitive Coupling Immune, Transient Sensitive Accelerator for Resistive Interconnect Signal of Subquarter Micron ULSI," *IEEE Journal of Solid-State Circuit*, Vol. SC-31, No. 4, pp. 531–536, April 1996.

[164] R. Downing, P. Gebler, and G. Katopis, "Decoupling Capacitor Effects on Switching Noise," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, Vol. 16, No. 5, pp. 484–489, August 1993.

[165] P. Larsson, "Parasitic Resistance in an MOS Transistor Used as On-chip Decoupling Capacitance," *IEEE Journal of Solid-State Circuit*, Vol. SC-32, No. 4, pp. 574–576, April 1997.

[166] B. Kanigicherla, S.-H. Oh, and D. Allee, "Determination of Optimum On-chip Bypass Capacitor in CMOS VLSI Systems to Reduce Switching Noise," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1724–1727, May 1997.

[167] P. Larsson, "Resonance and Damping in CMOS Circuits with On-chip Decoupling Capacitance," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. 45, No. 8, pp. 849–858, August 1998.

[168] J. Choi, S. Chun, N. Na, M. Swaminathan, and L. Smith, "A Methodology for the Placement and Optimization of Decoupling Capacitor for Gigahertz Systems," *Proceedings of IEEE International Conference on VLSI Design*, pp. 156–161, January 2000.

[169] T. Gao and C. L. Liu, "Minimum Crosstalk Switchingbox Routing," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 610–615, April 1994.

[170] A. Vittal and M. Marek-Sadowska, "Crosstalk Reduction for VLSI," *IEEE Transaction on Computer-Aided Design on Integrated Circuits and Systems*, Vol. CAD-16, No. 3, pp. 290–298, March 1997.

[171] R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation.* the IEEE Press, 1998.

[172] C. J. Alpert, A. Devgan, and S. T. Quay, "Buffer Insertion for Noise and Delay Optimization," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 362–367, June 1998.

[173] C.-P. Chen and N. Menezes, "Noise-Aware Repeater Insertion and Wire Sizing for On-Chip Interconnect Using Hierarchical Moment-Matching," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 502–506, June 1999.

Appendix A

Both Transistors Operating in the Linear Region for a Two-Line Coupled System

When both active transistors operate in the linear region, the drain-to-source current of each MOS transistor can be characterized by γV_{DS}, where γ is the effective output conductance of a MOS transistor. For an in-phase transition where the outputs of both inverters transition from high-to-low, the differential equations charactering a system of two coupled CMOS inverters are

$$-\gamma_1 V_1 = (C_1 + C_c)(1 + R_1\gamma_1)\frac{dV_1}{dt} - C_c(1 + R_2\gamma_2)\frac{dV_2}{dt}, \tag{A.1}$$

$$-\gamma_2 V_2 = (C_2 + C_c)(1 + R_2\gamma_2)\frac{dV_2}{dt} - C_c(1 + R1\gamma_1)\frac{dV_1}{dt}. \tag{A.2}$$

The general solutions of these coupled differential equations, (A.1) and (A.1), are

$$\begin{aligned} V_1 =& \frac{1}{2}K_3(e^{-\alpha_1 t} + e^{-\alpha_2 t} + \frac{\alpha_c}{\alpha_a}(e^{-\alpha_1 t} - e^{-\alpha_2 t})) \\ &+ K_4\frac{C_c\gamma_2(1 + R_2\gamma_2)}{\alpha_a}(e^{\alpha_1 t} - e^{\alpha_2 t}), \end{aligned} \tag{A.3}$$

and

$$\begin{aligned} V_2 =& \frac{1}{2}K_4(e^{-\alpha_1 t} + e^{-\alpha_2 t} - \frac{\alpha_c}{\alpha_a}(e^{-\alpha_1 t} - e^{\alpha_2 t})) \\ &+ K_3\frac{C_c\gamma_1(1 + R_1\gamma_1)}{\alpha_a}(e^{-\alpha_1 t} - e^{-\alpha_2 t}), \end{aligned} \tag{A.4}$$

where

$$\alpha_1 = \frac{1+R_1\gamma_1}{1+R_2\gamma_2}\frac{\alpha_b+\alpha_a}{C_1C_2+C_c(C_1+C_2)}, \tag{A.5}$$

$$\alpha_2 = \frac{1+R_1\gamma_1}{1+R_2\gamma_2}\frac{\alpha_b-\alpha_a}{C_1C_2+C_c(C_1+C_2)}, \tag{A.6}$$

$$\alpha_a = \sqrt{\alpha_c^2+4\gamma_1\gamma_2C_c^2(1+R1\gamma_1)(1+R_2\gamma_2)}, \tag{A.7}$$

$$\alpha_b = \gamma_1(1+R_2\gamma_2)(C_2+C_c)+\gamma_2(1+R_1\gamma_1)(C_1+C_c), \tag{A.8}$$

$$\alpha_c = \gamma_1(1+R_2\gamma_2)(C_2+C_c)-\gamma_2(1+R_1\gamma_1)(C_1+C_c). \tag{A.9}$$

K_3 and K_4 are integration constants which are determined from the initial conditions of V_1 and V_2 when both transistors enter the linear region, and are

$$K_3 = \frac{CV_1(\tau_l)-BV_2(\tau_l)}{AC-BD}, \tag{A.10}$$

$$K_4 = \frac{AV_2(\tau_l)-DV_1(\tau_l)}{AC-BD}, \tag{A.11}$$

where

$$A = \frac{1}{2}(e^{-\alpha_1\eta}+e^{-\alpha_2\eta}+\frac{\alpha_c}{\alpha_a}(e^{-\alpha_1\eta}-e^{-\alpha_2\eta})), \tag{A.12}$$

$$B = \frac{C_c\gamma_2(1+R_2\gamma_2)}{\alpha_a}(e^{-\alpha_1\eta}-e^{-\alpha_2\eta}), \tag{A.13}$$

$$C = \frac{1}{2}(e^{-\alpha_1\eta}+e^{-\alpha_2\eta}-\frac{\alpha_c}{\alpha_a}(e^{-\alpha_1\eta}-e^{-\alpha_2\eta})), \tag{A.14}$$

$$D = \frac{C_c\gamma_1(1+R_1\gamma_1)}{\alpha_a}(e^{-\alpha_1\eta}-e^{-\alpha_2\eta}). \tag{A.15}$$

τ_l is the time when both transistors start operating in the linear region. $V_1(\tau_l)$ and $V_2(\tau_l)$ are the initial values of V_1 and V_2 at the time τ_l.

Appendix B

One or More Transistors Operating in the Linear Region for a Three-Line Coupled System

For a three-line coupled system, it is assumed that Inv_1 leaves the saturation region first, followed by Inv_3 starting to operate in the linear region, and finally Inv_2 entering the linear region. Therefore, there are three disparate time regions, $\tau_{sat}^1 \leq t \leq \tau_{sat}^3$, $\tau_{sat}^3 \leq t \leq \tau_{sat}^2$, and $\tau_{sat}^2 \leq t$. For a set of equations such as

$$A_1X + B_1Y = D_1, \tag{B.1}$$

$$A_2X + B_2Y + C_2Z = D_2, \tag{B.2}$$

$$B_3Y + C_3Z = D_3, \tag{B.3}$$

the solution is

$$X = \frac{D_1}{A_1} + \frac{B_1(C_3(A_2D_1 - A_1D_2) + A_1C_2D_3)}{A_1((A_1B_2 - A_2B_1)C_3 - A_1B_3C_2)}, \tag{B.4}$$

$$Y = -\frac{C_3(A_2D_1 - A_1D_2) + A_1C_2D_3}{(A_1B_2 - A_2B_1)C_3 - A_1B_3C_2}, \tag{B.5}$$

$$Z = \frac{D_3}{A_3} + \frac{B_3(C_3(A_2D_1 - A_1D_2) + A_1C_2D_3)}{C_3((A_1B_2 - A_2B_1)C_3 - A_1B_3C_2)}. \tag{B.6}$$

B.1 Only Inv_1 Operates in the Linear Region

When only Inv_1 begins operating in the linear region, the discharge current of Inv_2 and Inv_3 (I_2 and I_3) is a constant, *i.e.*, $\frac{dI_2}{dt} = 0$ and $\frac{dI_3}{dt} = 0$ (neglecting the

Early effect). Therefore, the differential equations, (7.3), (7.4), and (7.5), become

$$(1 + R_1\gamma_{n1})C_{1t}\frac{dV_1}{dt} - C_{12}\frac{dV_2}{dt} = -\gamma_{n1}V_1, \tag{B.7}$$

$$C_{2t}\frac{dV_2}{dt} - (1 + R_1\gamma_{n1})C_{12}\frac{dV_1}{dt} - C_{23}\frac{dV_3}{dt} = I_2, \tag{B.8}$$

$$C_{3t}\frac{dV_3}{dt} - C_{23}\frac{dV_2}{dt} = I_3, \tag{B.9}$$

where

$$I_2 = - B_{n2}(V_{dd} - V_{TN})^{n_n}, \tag{B.10}$$

$$I_3 = - B_{n3}(V_{dd} - V_{TN})^{n_n}. \tag{B.11}$$

Defining

$$\psi_1 = t - \tau^1_{sat}, \tag{B.12}$$

substituting t with ψ_1, and applying a Laplace transform to (B.7), (B.8), and (B.9), a solution of the output voltages, $V_1(s)$, $V_2(s)$, and $V_3(s)$, is produced. These expressions maintain the same formulation as (B.4), (B.5), and (B.6). However, the coefficients are

$$A_1 = (1 + R_1\gamma_{n1})C_{1t}s + \gamma_{n1}, \tag{B.13}$$

$$B_1 = - C_{12}s, \tag{B.14}$$

$$D_1 = (1 + R_1\gamma_{n1})C_{1t}V_{nsat} - C_{12}V_2(\tau^1_{sat}), \tag{B.15}$$

$$A_2 = - (1 + R_1\gamma_{n1})C_{12}, \tag{B.16}$$

$$B_2 = C_{2t}, \tag{B.17}$$

$$C_2 = - C_{23}, \tag{B.18}$$

$$D_2 = \frac{I_2}{s^2}e^{-s\tau^1_{sat}} + \frac{C_{2t}V_2(\tau^1_{sat})}{s} - \frac{(1 + R_1\gamma_{n1})C_{12}V_{nsat} + C_{23}V_3(\tau^1_{sat})}{s}, \tag{B.19}$$

$$B_3 = - C_{23}, \tag{B.20}$$

$$C_3 = C_{3t}, \tag{B.21}$$

$$D_3 = \frac{I_3}{s^2}e^{-s\tau^1_{sat}} + \frac{C_{3t}V_3(\tau^1_{sat}) - C_{23}V_2(\tau^1_{sat})}{s}. \tag{B.22}$$

B.2 Both Inv_1 and Inv_3 Operate in the Linear Region

When both Inv_1 and Inv_2 operate in the linear region, the discharge current of Inv_2 is a constant, *i.e.*, $\frac{dI_2}{dt} = 0$ (neglecting the Early effect). Therefore, the

differential equations, (7.3), (7.4), and (7.5), become

$$(1 + R_1\gamma_{n1})C_{1t}\frac{dV_1}{dt} - C_{12}\frac{dV_2}{dt} = -\gamma_{n1}V_1, \tag{B.23}$$

$$C_{2t}\frac{dV_2}{dt} - (1 + R_1\gamma_{n1})C_{12}\frac{dV_1}{dt} - (1 + R_3\gamma_{n3})C_{23}\frac{dV_3}{dt} = I_2, \tag{B.24}$$

$$(1 + R_3\gamma_{n3})C_{3t}\frac{dV_3}{dt} - C_{23}\frac{dV_2}{dt} = -\gamma_{n3}V_3, \tag{B.25}$$

where

$$I_2 = -B_{n2}(V_{dd} - V_{TN})^{n_n}. \tag{B.26}$$

Defining

$$\psi_2 = t - \tau^3_{sat}, \tag{B.27}$$

substituting t with ψ_2, and applying a Laplace transform to (B.23), (B.24), and (B.25), a solution of the output voltages, $V_1(s)$, $V_2(s)$, and $V_3(s)$, is produced. These expression maintain the same formulation as (B.4), (B.5), and (B.6). The coefficients are

$$A_1 = (1 + R_1\gamma_{n1})C_{1t}s + \gamma_{n1}, \tag{B.28}$$

$$B_1 = -C_{12}s, \tag{B.29}$$

$$D_1 = (1 + R_1\gamma_{n1})C_{1t}V_1(\tau^3_{sat}) - C_{12}V_2(\tau^3_{sat}), \tag{B.30}$$

$$A_2 = -(1 + R_1\gamma_{n1})C_{12}, \tag{B.31}$$

$$B_2 = C_{2t}, \tag{B.32}$$

$$C_2 = -(1 + R_3\gamma_{n3})C_{23}, \tag{B.33}$$

$$D_2 = \frac{I_2}{s^2}e^{-s\tau^3_{sat}} + \frac{C_{2t}V_2(\tau^3_{sat})}{s} - \frac{(1 + R_1\gamma_{n1})C_{12}V_1(\tau^3_{sat}) + (1 + R_3\gamma_{n3})C_{23}V_{nsat}}{s}, \tag{B.34}$$

$$B_3 = -C_{23}s, \tag{B.35}$$

$$C_3 = (1 + R_3\gamma_{n3})C_{3t}s + \gamma_{n3}, \tag{B.36}$$

$$D_3 = (1 + R_3\gamma_{n3})C_{3t}V_{nsat} - C_{23}V_2(\tau^3_{sat}). \tag{B.37}$$

B.3 Inv_1, Inv_2, and Inv_3 all operate in the Linear Region

When Inv_1, Inv_2, and Inv_3 all operate in the linear region, the differential equations, (7.3), (7.4), and (7.5), become

$$(1 + R_1\gamma_{n1})C_{1t}\frac{dV_1}{dt} - C_{12}\frac{dV_2}{dt} = -\gamma_{n1}V_1, \tag{B.38}$$

$$(1 + R_2\gamma_{n2})C_{2t}\frac{dV_2}{dt} - (1 + R_1\gamma_{n1})C_{12}\frac{dV_1}{dt} - (1 + R_3\gamma_{n3})C_{23}\frac{dV_3}{dt} = -\gamma_{n2}V_2, \tag{B.39}$$

$$(1 + R_3\gamma_{n3})C_{3t}\frac{dV_3}{dt} - C_{23}\frac{dV_2}{dt} = -\gamma_{n3}V_3. \tag{B.40}$$

Defining

$$\psi_3 = t - \tau_{sat}^2, \tag{B.41}$$

substituting t with ψ_3, and applying a Laplace transform to (B.38), (B.39), and (B.40), a solution of the output voltages, $V_1(s)$, $V_2(s)$, and $V_3(s)$, is produced. These expressions maintain the same formulation as (B.4), (B.5), and (B.6). The coefficients are

$$A_1 = (1 + R_1\gamma_{n1})C_{1t}s + \gamma_{n1}, \tag{B.42}$$

$$B_1 = -C_{12}s, \tag{B.43}$$

$$D_1 = (1 + R_1\gamma_{n1})C_{1t}V_1(\tau_{sat}^2) - C_{12}V_2(\tau_{sat}^2), \tag{B.44}$$

$$A_2 = -(1 + R_1\gamma_{n1})C_{12}s, \tag{B.45}$$

$$B_2 = (1 + R_2\gamma_{n2})C_{2t}s + \gamma_{n2}, \tag{B.46}$$

$$C_2 = -(1 + R_3\gamma_{n3})C_{23}s, \tag{B.47}$$

$$D_2 = (1 + R_2\gamma_{n2})C_{2t}V_{nsat} - (1 + R_1\gamma_{n1})C_{12}V_1(\tau_{sat}^2) - (1 + R_3\gamma_{n3})C_{23}V_3(\tau_{sat}^2), \tag{B.48}$$

$$B_3 = -(1 + R_2\gamma_{n2})C_{23}s, \tag{B.49}$$

$$C_3 = (1 + R_3\gamma_{n3})C_{3t}s + \gamma_{n3}, \tag{B.50}$$

$$D_3 = (1 + R_3\gamma_{n3})C_{3t}V_3(\tau_{sat}^2) - (1 + R_2\gamma\gamma_{n2})C_{23}V_{nsat}. \tag{B.51}$$

Appendix C

Publications

1. T. Tang and X. Zhou, "Multi-Level Digital/Mixed-Signal Simulation with Automatic Circuit Partition and Dynamic Delay Calculation," *Journal of Modeling and Simulation of Microsystems* Vol. 1, No. 2, pp. 83-90, 1999.

2. X. Zhou, T. Tang, L. Seah, C. Yap, and S. Choo, "Numerical Investigation of Subpicosecond Electrical Pulse Generation by Edge Illumination of Silicon Transmission-Line Gaps," *IEEE Journal of Quantum Electronics*, Vol. 34, No. 1, pp. 171-178, January 1998.

3. K. T. Tang and E. G. Friedman, "Delay and Noise Estimation of CMOS Logic Gates Driving Coupled Resistive-Capacitive Interconnections," *Integration - the VLSI Journal* (accepted).

4. K. T. Tang and E. G. Friedman, "Delay Uncertainty Due to On-Chip Simultaneous Switching Noise in High Performance CMOS Integrated Circuits," *2000 IEEE Workshop on Signal Processing Systems - Design and Implementation* (accepted).

5. K. T. Tang and E. G. Friedman, "Transient *IR* Voltage Drops in CMOS-Based Power Distribution Networks," *2000 Midwest Symposium on Circuits and Systems* (accepted).

6. K. T. Tang and E. G. Friedman, "Lumped Versus Distributed *RC* and *RLC* Interconnect Impedances," *2000 Midwest Symposium on Circuits and Systems* (accepted).

7. K. T. Tang and E. G. Friedman, "On-Chip Delta-I Noise in the Power Distribution Networks of High Speed CMOS Integrated Circuits," *2000 IEEE ASIC/SoC Conference* (accepted).

8. K. T. Tang and E. G. Friedman, "Delay Uncertainty Due to On-Chip Simultaneous Switching Noise in CMOS Power Distribution Networks," *2000 SRC's Premier Technical Conference* (accepted).

9. K. T. Tang and E. G. Friedman, "Delay and Power Expressions Characterizing a CMOS Inverter Driving an *RLC* Load," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 4.269-4.272, May 2000.

10. K. T. Tang and E. G. Friedman, "Transient Analysis of a CMOS Inverter Driving Resistive Interconnect," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 3.283-3.286, May 2000.

11. K. T. Tang and E. G. Friedman, "Noise Estimation Due to Signal Activity for Capacitively Coupled CMOS Logic Gates," *10th IEEE Great Lakes Symposium on VLSI*, pp. 171-176, March 2000.

12. K. T. Tang and E. G. Friedman, "Estimation of On-Chip Simultaneous Switching Noise in VDSM CMOS Circuits," *International Conference on Modeling and Simulation of Microsystems*, pp. 313-316, March 2000.

13. K. T. Tang and E. G. Friedman, "Peak Crosstalk Noise Estimation in CMOS VLSI Circuits," *Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems*, pp. 1539-1542, September 1999.

14. K. T. Tang and E. G. Friedman, "Peak Noise Prediction in Loosely Coupled Interconnect," *Proceedings of the IEEE International Symposium on Circuits And Systems*, pp. 1.541-544, May 1999.

15. K. T. Tang and E. G. Friedman, "Interconnect Coupling Noise in CMOS VLSI Circuits," *Proceedings of the ACM/IEEE International Symposium on Physical Design*, pp. 48-53, April 1999.

16. K. T. Tang and E. G. Friedman, "Crosstalk Between Loosely Coupled Interconnect," *Proceedings of the IEEE 22nd Annual Electron Devices Activities in Western New York Conference*, pp. 9-10, November 1998.

17. S. Rofail, K. Yeo, K. Chew, X. Zhou, and T. Tang, "An Experimentally-Based DC Model for the Bi-CMOS Structure and Its Adaptation to a Circuit Simulation Environment," *Proceedings of the IEEE Canadian Conference on Electrical and Computer Engineering*, Vol. 1, pp. 37-40, May 1998.

18. D. Jacobs-Perkins, M. Currie, K. Tang, C. Wang, C. Williams, and T. Hsiang, "Subpicosecond Electro-optic Imaging System Using Interferometric and Polarimetric Apparatus," *OSA TOPS on Ultrafast Electronic and Optoelectronics*, Vol. 13, pp. 202-207, 1997.

19. T. Tang and X. Zhou, "A Dynamic Timing Delay for Accurate Gate-Level Circuit Simulation," *Proceedings of the 39th IEEE Midwest Symposium on Circuits and Systems*, pp. 325-327, August 1996.

20. X. Zhou and T. Tang, "Accurate Timing Simulation of Mixed-Signal Circuits with Dynamic Delay Model," *Proceedings of the International Workshop on Computer-Aided Design, Test, and Evaluation for Dependability (CADTED)*, pp. 309-311, July 1996.

21. T. Tang and X. Zhou, "Modeling and Simulation of GaAs High-Speed HBT, MESFET, and HEMT Analog/Digital Circuits," *Proceedings of the 2nd MINDEF-NTU Joint Seminar*, pp. 77-83, January 1996.

22. T. Tang and X. Zhou, "Mixed-Mode Simulation of High-Speed HFET Logic Circuit," *Proceedings of the 6th International Symposium on Integrated Circuits and Systems (ISICS-95)*, pp. 510-514, September 1995.

23. X. Zhou and T. Tang, "Multi-Level Modeling of GaAs High-Speed Digital Circuits," *The EEE Journal*, School of Electrical and Electronic Engineering, Nanyang Technological University, Vol. 7, No. 1, pp. 58-64, July 1995.

24. T. Tang, Z. Jiang, and Z. Qiao, "Two Dimensional Model and Length Simulation in VLSI LOCOS Isolation Technology," *Proceedings of the 8th National Annual Semiconductor and Materials Conference*, 1993.

25. N. Yu, B. Shi, and T. Tang, "Design and Verification of a VTL (Variable Threshold Logic) Cell Chip in an Image Processor," *Proceedings of the 6th National Annual Network Conference*, 1991.