

ANALOG VS. DIGITAL: A COMPARISON OF CIRCUIT IMPLEMENTATIONS FOR LOW-POWER MATCHED FILTERS

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ABSTRACT

The matched filter or correlator block of a spread-spectrum communication system occupies a place in the receiver that just follows the analog RF-to-baseband or RF-to-IF downconversion circuitry and just precedes the digital data-decoding circuitry. A matched filter may, therefore, be implemented via either digital or analog circuit techniques. This paper analyzes and compares a digital and an analog implementation of a programmable parallel matched filter using power efficiency—as a function of signal integrity, filter size, operating frequency, and technology scaling—as the primary metric of comparison. A methodology is presented and results are given that indicate where in the multidimensional design space the digital circuit is more power-efficient than the analog one, and vice versa.

1. INTRODUCTION

The time frame over which groups and individuals have debated whether a digital or an analog circuit technique should be used to realize a given functional block can be measured in decades. For many functions, the debate has been settled for quite some time. There is not much question, for example, that digital is the preferred circuit implementation for a multiplier with precision equivalent to 64 bits, nor is there much question that analog is the proper choice for a 2 GHz RF modulator.

There still exists, however, areas where the choice between a digital or an analog circuit implementation is unclear. Recent commercial interest in spread-spectrum systems for wireless data networks [1-3] provides the motivation for evaluating one of these remaining areas, that of programmable parallel matched filters. With portable data terminals—such as cellular phones—being the primary commercial outlet for this new interest in spread-spectrum communications, the issue of low-power is of foremost concern in choosing a circuit format— analog or digital— for the implementation of the matched filter blocks.

The discussion that follows compares analog and digital circuits using the specific application of matched filters as the backdrop for the comparison. Power consumption is used as the primary metric of comparison, while data precision, technology scaling, operating frequency, and filter length are used as the common design parameters. The function and purpose of a matched filter are briefly discussed in section 2. A low-power digital matched filter circuit and a low-power analog matched filter circuit are presented and analyzed in sections 3 and 4, respectively. In section 5, the digital and analog circuits are

compared, and conclusions are presented that indicate how a variation of the design space parameters changes the relative power efficiency of the digital and analog matched filters.

2. A REVIEW OF MATCHED FILTERS

The matched filter block (shown in Figure 1a) of a radio occupies a place between the RF input circuitry and the digital data processing circuitry. As such, the conversion from analog to digital can take place either just before the matched filter input or just after its output. This leaves the designer with the freedom to use the most suitable matched filter, analog or digital.

The function and utility of the matched filter within a communications system is described in detail in the literature [4-6]. The matched filters that may be employed within the recently proposed spread-spectrum communication systems operate at medium speeds (one MHz to, perhaps, several tens of MHz), require a relatively coarse representation of data (six bits equivalent or less), and have a structure that is identical to that of a FIR filter with asymmetric taps [1-3].

3. DIGITAL IMPLEMENTATION

The digital programmable parallel matched filter structure that is used in this analysis is pictured in block diagram form in Figure 1b. The operation of the filter is such that each new input data sample appears simultaneously at the input of each multiplier block. After multiplication with the N stored reference coefficients, the partial sums of products are shifted one cell to the right during each clock cycle, with the final sum at the bottom right being the desired matched filter output. The structure is commonly used to implement FIR filters (*e.g.*, [7]) and has several advantages over a direct implementation of Figure 1a, such as ease of layout and no need for a single large adder to generate the output result.

The power consumption of the digital matched filter can be estimated by summing the contribution of the major logic blocks: the registers, adders, and multipliers. In the following analysis, it is assumed that the dynamic charging and discharging of the inherent circuit capacitances is the primary contributor to the total power consumption. The total dynamic CV^2f power can be estimated by computing or measuring the effective switched capacitance of each of the major logic blocks. However, in the spirit of [8], supply voltage can vary as a function of operating frequency and quantization level. A single supply voltage is assumed for the entire matched filter, with the value of V_{DD} being determined by the speed requirements of the most performance-limiting circuit elements, the multipliers.

From [8], an estimate of gate propagation delay T_d is given as a function of supply voltage V_{DD} , threshold voltage V_T , load capacitance C_L , oxide capacitance per unit area C_{ox} , electron

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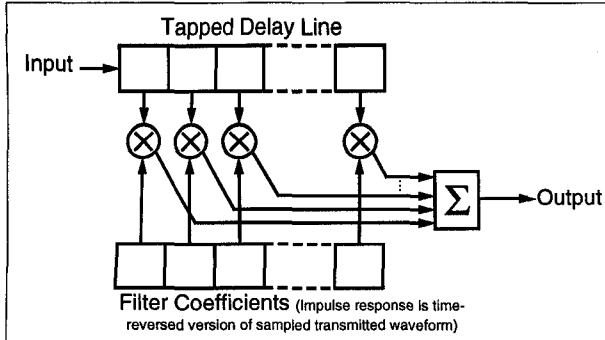


Figure 1a. Parallel matched filter structure.

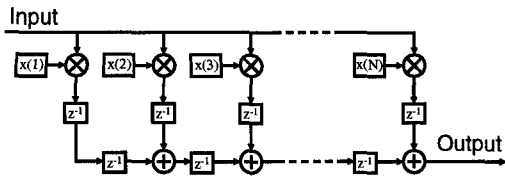


Figure 1b. Digital matched filter architecture.

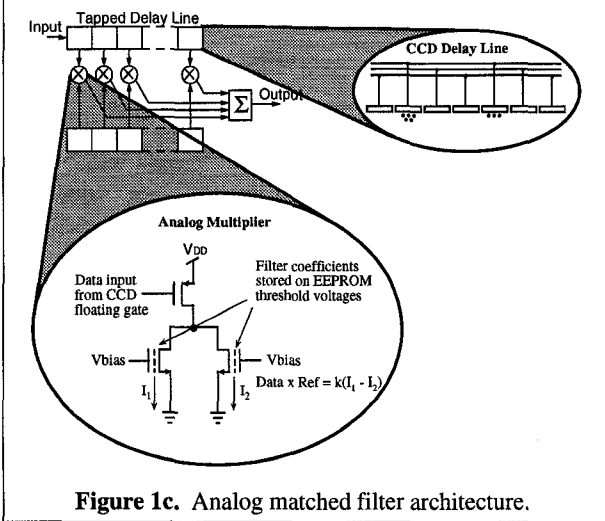


Figure 1c. Analog matched filter architecture.

mobility μ , and the CMOS gate width-to-length ratio W/L :

$$T_d \cong \frac{C_L}{\mu C_{ox} W/L} \cdot \frac{V_{DD}}{(V_{DD} - V_T)^2} \quad (1)$$

Also, for a given technology, the time required to complete a Q_d bit \times Q_r bit multiplication can be approximated as [9,10]

$$T_{multiply} \cong M(Q_d + Q_r - 1) \quad (2)$$

where M is the delay of a one-bit adder, with units of seconds/bit, and Q_d and Q_r are the level of data and reference quantization, respectively. Combining (1) and (2) gives

$$T_{multiply} \cong K_d(Q_d + Q_r - 1) \cdot \frac{V_{DD}}{(V_{DD} - V_T)^2} \quad (3)$$

where $\frac{C_L}{\mu C_{ox} W/L}$ and M have been merged to form K_d , a technology dependent constant with units of volt \cdot seconds / bit.

The value of V_{DD} that is derived from (3) can be used to estimate the total power consumption of a digital multiplier,

$$P_{multiply} \cong \frac{K_p Q_d (Q_r - 1)}{T_{multiply}} \left[\frac{1}{2} (\beta + \sqrt{\beta^2 - 4V_T^2}) \right]^2 \quad (4)$$

where $\beta = 2V_T + \frac{K_d(Q_d + Q_r - 1)}{T_{multiply}}$, and K_p is a technology dependent constant with units of farads / bit².

The total power consumption of the digital matched filter, P_{DMF} , is

$$P_{DMF} \cong NP_{multiply} + AC_{ADDER}V_{DD}^2f_{clk} + RC_{REGISTER}V_{DD}^2f_{clk} \quad (5)$$

where $N = 2^k$ is the number of filter taps, f_{clk} is the operating frequency of the matched filter, C_{ADDER} and $C_{REGISTER}$ are the effective switched capacitance of the full adders and one-bit registers, respectively, and A and R are the number of full adders and one-bit registers in the digital matched filter, respectively, as given by

$$A = (2^k - 1)(Q_d + Q_r) - K + \sum_{m=1}^{k-1} (m2^m),$$

$$\text{and } R = 2^{k+1}(Q_d + Q_r) - (2^k + 1) + \sum_{m=1}^{k-1} (m2^m).$$

In the plots that follow, the values below are assumed for a 2.0 μm CMOS process: $V_T = 1.0$ volt, $K_p = 1.5$ pF / bit², $K_d = 10^{-8}$ volt \cdot sec / bit, $C_{REGISTER} = 250$ fF, and $C_{ADDER} = 600$ fF.

The choice of implementing technology has an enormous effect on the power consumption of a digital matched filter. Assuming the operating frequency of the matched filter can be satisfied by a particular technology, the supply voltage in a scaled technology can be decreased to realize additional power savings [8] beyond those achievable by a direct application of classical scaling rules [11,12]. The reduction in power dissipation depends on the degree of technology scaling (represented by the scaling constant κ [11]) and the ratio of the threshold voltage to the supply voltage in the unscaled technology,

$$\rho = \frac{V_{T_{unscaled}}}{V_{DD_{unscaled}}} \quad (6)$$

The power scaling constant, which is defined in this paper as S_{C^*} is

$$S_{C_{ce}} = \frac{1}{\kappa^2} \left(\rho + \frac{(1-\rho)^2}{2\kappa} + \frac{(1-\rho)}{2} \sqrt{\frac{4\rho}{\kappa} + \left(\frac{1-\rho}{\kappa}\right)^2} \right)^2 \quad (7)$$

or

$$S_{C_{cvr}} = \frac{1}{\kappa} \left(\rho + \frac{(1-\rho)^2}{2\kappa^2} + \frac{(1-\rho)}{2\kappa} \sqrt{4 - \left(\frac{1-\rho}{\kappa}\right)^2} \right)^2 \quad (8)$$

$S_{C_{ce}}$ is applicable assuming ideal constant electric-field scaling [11]. $S_{C_{cvr}}$ is applicable assuming the threshold voltage does not scale with the other device parameters. The current industry trend lies somewhere between the two schemes, as shown in Figure 2.

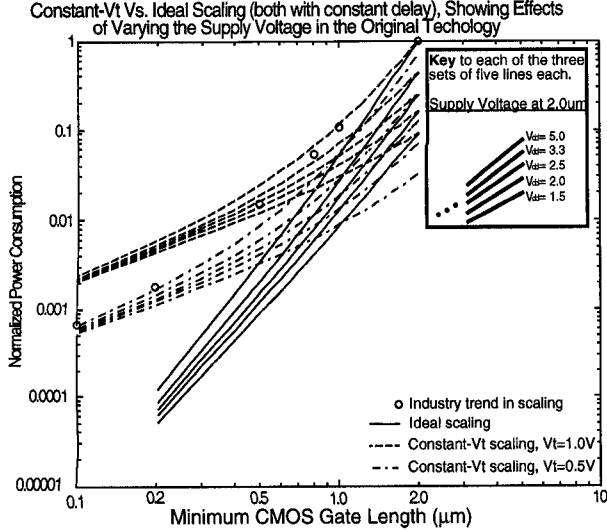


Figure 2. Effects of technology scaling on digital circuit power consumption.

The estimate of the power consumption of the digital matched filter is a function of operating frequency, quantization levels, filter length (number of taps), and technology scaling:

$$P_{DMF_{ce}} \cong S_{C_{ce}} P_{DMF}, \quad (9a)$$

or

$$P_{DMF_{cvt}} \cong S_{C_{cvt}} P_{DMF}, \quad (9b)$$

depending on which scaling procedure is used to shrink the device dimensions and operating voltages.

4. ANALOG IMPLEMENTATION

The analog matched filter structure shown in Figure 1c is used to compare the analog and digital circuit-implementing technologies. The tapped delay line function is realized by a surface channel charge-coupled-device (CCD) analog shift register, which may be simply understood as a bank of sequentially switched MOS capacitors. The signal is in the form of electrically injected minority carriers present under the appropriately clocked CCD gates. A surface channel device is used rather than a buried channel device because it is inherently more linear and, due to electrical injection of the signal charge, the surface channel device is capable of higher signal integrity [13].

In the configuration shown in Figure 1c, the signal is non-destructively sensed by a floating gate tap [14] that is attached to every third CCD gate. The multiply function and reference coefficient storage are achieved by the two-transistor EEPROM structure shown in the figure. The tap reference voltage V_{REF} is stored by altering the threshold voltages of the two EEPROMs in the cell via control circuitry (not shown in Figure 1c). The sources of the two EEPROMs are connected to separate current-summing busses, both of which are held at virtual ground. When operating in the triode region, the difference in the drain currents through the two EEPROMs is proportional to a multiplication of the drain voltage and the stored reference voltages.

The structure and circuit elements pictured in Figure 1c have appeared in the literature in various forms for over two decades [14-17]. The structure is used here because, so far as the authors are aware, it is the most power-efficient means to implement an

analog parallel programmable matched filter using readily available silicon technology. As such, the structure is suitable for comparison with its digital counterpart, as discussed above.

Throughout this section, the power consumption of the analog matched filter is given as a function of the signal-to-noise ratio (SNR). This is completely analogous to considering the power consumption of the digital matched filter as a function of quantization level. The analog SNR and the digital quantization level are related via

$$SNR = \sqrt{3}(2^{Q_d} - 1), \quad (10)$$

where Q_d is the data quantization level that is used in (2).

The static current of the multiplier/tap structures and the dynamic switching of the CCD gates are the dominant sources of power dissipation within the analog matched filter. The dominant noise sources are the thermal noise of the tap and multiplier FETs and interface trapping effects under the CCD gates [13,18,19]. The problem of flicker noise is assumed to be alleviated by a correlated-double-sampling amplifier [20] on the matched filter output. Making this assumption, an estimate of the power dissipation within the entire analog matched filter is

$$P_{AMF} \cong 8 \cdot SNR^2 \cdot f_{clk} \cdot kT \cdot N \left(\frac{a(a-b)}{a-\sqrt{ab}} + \frac{b(a-b)}{\sqrt{ab}-b} \right), \quad (11)$$

$$\text{where } a = \frac{1}{4} \ln(2) \cdot N \cdot N_{ss} \cdot \frac{q}{C_{ox}} \cdot \frac{V_{DD}}{V_{DD} - \phi_s},$$

$$b = \frac{\sqrt{2} \cdot V_{DD}}{3(V_{DD} - 3V_T)} + \frac{V_{DD}(V_{DD} - 2V_T)}{(V_{DD} - 5V_T/2)V_T},$$

the thermal energy kT is in units of joules, N is the number of filter taps, f_{clk} is the operating frequency, N_{ss} is the surface state density, V_T is the threshold voltage of the PFETs and EEPROMs (assumed to be equal in magnitude), q is the charge of an electron, C_{ox} is the oxide capacitance per unit area, and ϕ_s is the minimum surface potential under the CCD gates.

It has been noted above that by scaling the device dimensions and power supply voltage an enormous power savings for the digital circuitry can be achieved. Such is not the case with the analog matched filter implementation of Figure 1c. The decrease in anneal time for thinner gate oxides may lead to an increase in surface state density [21]. Thus, even though the switched capacitance of a scaled analog matched filter may be smaller than the unscaled filter, the supply voltage may need to be raised to offset the negative effects of the increased surface state density within the scaled device. Thus, the effect of scaling on the power consumption of the analog matched filter is process dependent. Similar, more general conclusions pertaining to analog circuits and scaling issues are drawn in [22].

The supply voltage level is more flexible in the analog filter than in the digital filter. This flexibility exists because a matched filter of equivalent performance can be made from a circuit with a higher supply voltage if the CCD gate areas are decreased. In Figure 3 it is shown that wide changes in the supply voltage result in only a small change in the power dissipation of the analog matched filter.

5. COMPARISON AND CONCLUSIONS

Both of the circuit implementations under consideration perform the same operation and use the same physical device

—the MOS capacitor— as the primary circuit element. The digital implementation, in treating the MOS capacitor-based devices as binary switches, sacrifices power efficiency for the ability to regenerate weak or degraded signals within the circuit.

The analog implementation uses the fundamental device I-V transistor relationships to efficiently achieve the sum and multiplication functions. However, the analog circuit is unable to regenerate weak or degraded internal signals. Thus, at the cost of additional power consumption, the analog circuit must inject added signal quality (surplus SNR) at the start of the shift register structure, so that the design specifications are still satisfied by the degraded signal at the end of the shift register. This difference is born out in the power consumption equations, which show that power consumption as a function of filter length increases at a quadratic rate for the analog circuit, while at a nearly linear rate for the digital circuit.

The digital circuit is more sensitive to changes in speed. This sensitivity is due to the ability of the digital circuit to exploit a decrease in operating frequency by supporting a corresponding decrease in the supply voltage. The digital circuit is also more sensitive to changes in technology. By decreasing the minimum feature size of the CMOS technology, a significant power savings is achieved. This behavior is not necessarily true for the analog circuit, since device physics limit the analog circuit more severely than the digital circuit.

Since changes in filter size, technology scaling, and operating frequency have different effects on the power consumption of the analog and digital circuits, it follows that there may be points in the design space where the digital circuit is more power-efficient than the analog one, and still other points in the design space where the opposite may be true. As shown in Figure 4, for a given effective quantization level, there is a surface in the multidimensional design space defining the boundary between the regions of superior power efficiency of the analog and digital circuits. Inside the volume in the figure, it is more efficient to implement the digital circuit. Outside the volume, the analog circuit is more power-efficient. Specific power estimates of the digital and analog circuit implementation are obtained with (9) and (11), respectively.

In conclusion, the analog circuit implementation discussed in this paper is more power-efficient for shorter, faster matched filters, and, conversely, the digital circuit is more power-efficient where the filters are longer and slower. Also, since the linearity of the analog devices is limited to approximately six bits of quantization, the digital circuit will have an advantage if

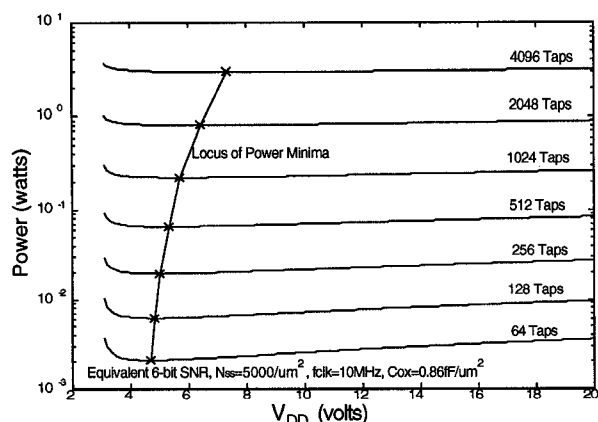


Figure 3. Analog matched filter power as a function of supply voltage and filter length.

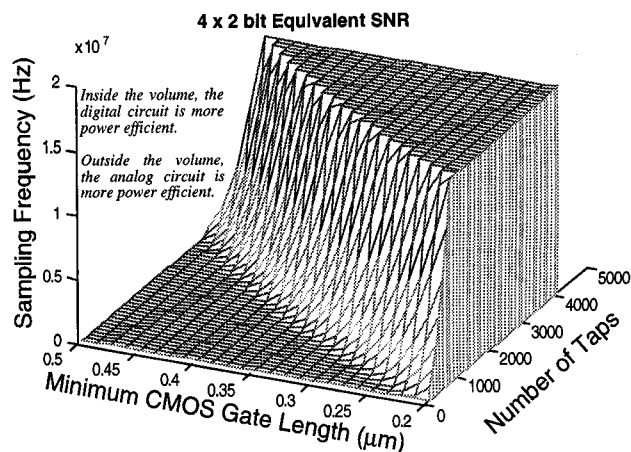


Figure 4. Surface of equal power dissipation for the analog and digital matched filter implementations as a function of filter length, sampling frequency, and technology.

higher levels of precision are required. These concepts and the preceding analyses may be applied to electronic circuit design in general and provide insight into why choosing the preferred implementation of a 64 bit multiplier or a 2 GHz modulator is straightforward, while determining the most power-efficient means to implement a programmable parallel matched filter requires close investigation.

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