Peak Crosstalk Noise Estimation in CMOS VLSI Circuits

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Abstract— **Interconnect between a CMOS driver and receiver can be modeled as a lossy transmission line in high speed CMOS VLSI circuits as transition times become comparable to or less than the time of flight delay of the signal through the interconnect. In this discussion, a linear resistor model is used to approximate the CMOS driver stage, and the CMOS receiver is modeled as a capacitor. A closed form expression for the coupling noise between adjacent interconnect is presented to estimate the coupling noise voltage on a quiet line based on the assumption that these interconnections are loosely coupled, where the effect of the coupling noise on the waveform of the active line is small and can be neglected. It is demonstrated that the output impedance of the CMOS driver should be comparable to the interconnect impedance in order to reduce the propagation delay of the CMOS driver stage.**

I. Introduction

The trend in modern high speed, high density CMOS VLSI circuits is decreasing feature sizes as well as increasing chip dimensions. The delay of these highly scaled circuits is dominated by the interconnect [1]. Furthermore, up to 30% of the dynamic power is consumed by the interconnect [2]. In addition to the interconnect delay and power consumption, coupling noise (or crosstalk) between adjacent interconnect lines is also a primary concern for present and future generations of CMOS VLSI circuits [3], [4].

Coupling noise between adjacent interconnect can cause disastrous effects on the logical functionality and long-term reliability of a VLSI circuit [5]. Coupling effects become more significant as the feature size is decreased to deep submicrometer dimensions because the spacing between conductor lines is decreased and the thickness of the conductors is increased in order to reduce the parasitic resistance of the conductors. If the peak noise voltage at the receiver is greater than the threshold voltage of the CMOS receiver, a circuit malfunction may occur. Furthermore, the induced noise voltage may cause extra power to be dissipated on the quiet line due to momentary glitches at the output of the logic gates. Carrier injection or collection into the substrate may occur as the coupling noise voltage rises above the power supply voltage V_{dd} or falls below ground [6].

An analysis of the coupling noise can be performed in both the frequency domain and the time domain, but most of these analyses result in numerical solutions [7], [8] or an equivalent circuit simulation [9]. A numerical solution is not convenient to use at the system (or chip) level to predict noise effects since it requires significant simulation time and computer memory. An analytical analysis of coupled lossless transmission lines in the time domain has been addressed in [10]. This lossless model is not appropriate for interconnect in CMOS VLSI circuits, since the parasitic interconnect resistance cannot be neglected.

An analysis of coupled interconnect in CMOS VLSI circuits is presented in this paper. For simplicity, the interconnect is modeled as a uniform transmission line. The analytical equations are derived from time domain differential equations using Laplace transforms and the assumption of a loosely coupled condition, in which the coupling capacitance and the mutual inductance are assumed to be less than 30% of the self-capacitance and the self-inductance, respectively. The CMOS driver stage is modeled as a linear resistor. The CMOS receiver stage is modeled as a capacitor.

The accuracy of the predicted peak noise voltage based on these closed form expressions is within 20% for the driver end coupling noise voltage and 15% for the receiver end coupling noise voltage. The dependency of the propagation delay of the CMOS driver stage on the driver impedance, and the relationship between the relaxation time of the coupling noise and the driver impedance is also investigated.

The analytical model for a CMOS driver and receiver structure, as well as closed form expressions of the coupling noise voltage at both ends of the quiet interconnect line, are addressed in Section II. The predicted coupling noise voltage based on the analytical equations is compared with simulation in Section III. A discussion of the coupling noise voltage of lossy interconnect, the effects of the coupling noise on CMOS VLSI circuits, the driver output impedance, and the relaxation time of the coupling noise voltage are discussed in Section IV followed by some concluding remarks in Section V.

II. Analytical Equations

Consider a typical CMOS driver and receiver structure in a high speed VLSI circuit, an example of which is shown in Fig. 1a. The interconnect between the CMOS driver and receiver is modeled as a lossy transmission line. In order to analyze the coupling noise, the CMOS driver is modeled as a linear resistor (R_1 and R_2) and the receiver is modeled as a capacitor, where the impedance is larger than the line impedance and the reflection coefficient at the receiver is approximated as one.

The equivalent circuit model is shown in Fig. 1b, where two coupled lossy transmission lines have similar impedance characteristics, *i.e.*, R, L, and C are the same for each line. Line 1 is the active (or aggressor) line and line 2 is the quiet (or victim) line.

Laplace transforms are used to solve the time domain differential equations characterizing this structure. The resulting formulation is

$$\frac{\partial^2}{\partial x^2}V_1(x,s) = A_1V_1(x,s) + B_1V_2(x,s), \tag{1}$$

$$\frac{\partial^2}{\partial x^2}V_2(x,s) = A_2V_1(x,s) + B_2V_2(x,s), \tag{2}$$

where

$$A_1 = B_2 = sRC + s^2LC - s^2L_mC_m, \tag{3}$$

$$B_1 = A_2 = s^2L_mC - s^2LC_m - sRC_m. \tag{4}$$

The minus sign in (3) and (4) occurs since C_m is a positive value [8], [12].

In order to simplify this analysis, a condition that the interconnect lines are loosely coupled is assumed, implying that L_m and C_m are small as compared to L and

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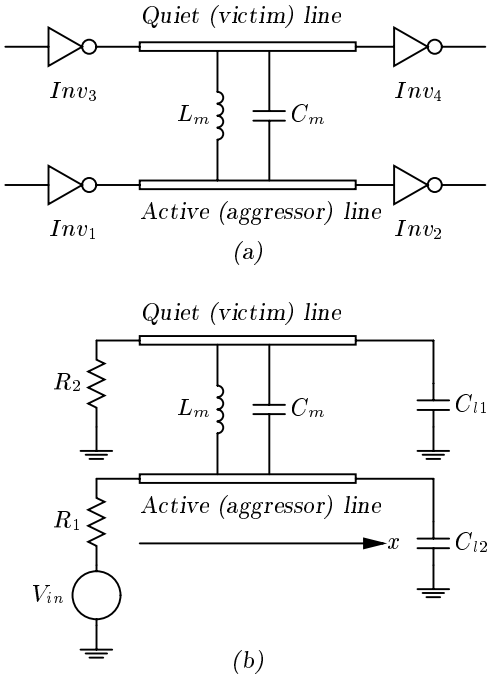

Fig. 1. An example of a CMOS driver and receiver structure. a) Two adjacent CMOS drivers and receivers. b) A simplified circuit model of the structure.

C such that the third term in (3) can be neglected. To quantify this assumption,

$$\frac{L_m}{L}\frac{C_m}{C} < 0.1. \tag{5}$$

The error is less than 5% with this assumption. Based on this loosely coupled assumption, (1) and (2) can be simplified to

$$\frac{\partial^2}{\partial x^2}V_1(x,s) = \gamma^2 V_1(x,s), \tag{6}$$

$$\frac{\partial^2}{\partial x^2}V_2(x,s) = \gamma^2 V_2(x,s) + \alpha V_1(x,s), \tag{7}$$

where

$$\gamma = \sqrt{sRC + s^2LC}, \tag{8}$$

$$\alpha = (s^2L_mC - sRC_m - s^2LC_m). \tag{9}$$

The solution of (6) is

$$V_1(x,s) = V_+e^{-\gamma x} + V_-e^{+\gamma x}. \tag{10}$$

V_+ and V_- can be solved based on the terminal condition of line 1. The general solution of (7) is

$$V_2(x,s) = (a_1x + c_1)e^{-\gamma x} + (a_2x + c_2)e^{+\gamma x}. \tag{11}$$

a_1 and a_2 are determined by solving the non-homogeneous differential equation, (7). c_1 and c_2 are calculated by using the boundary conditions of line 2. Therefore, all of the coefficients are determined based on boundary conditions, permitting the general closed form solutions of $V_1(x,s)$ and $V_2(x,s)$ to be determined.

The time domain solutions of $V_1(x,s)$ and $V_2(x,s)$ can be obtained by applying an inverse Laplace transform. However, in many of these cases, a numerical solution results, because the inverse Laplace transform of $\frac{1}{1+e^{-2\gamma x}}$ cannot be derived explicitly. In order to determine a closed form analytical expression for use in chip level noise analysis, some approximating assumptions are necessary.

The propagation factor γ, defined in (8), is

$$\gamma = \sqrt{sRC + s^2LC} = s\sqrt{LC}(1 + \frac{R}{sL})^{\frac{1}{2}}$$
$$\approx s\sqrt{LC}(1 + \frac{R}{2sL}) \qquad sL \gg R. \tag{12}$$

The assumption of $sL \gg R$ is equivalent to $\omega L \gg R$ in the frequency domain, *i.e.*, the losses are small but not necessarily negligible. If the driver output impedances of line 1 and line 2 match the line impedance, no reflections will occur at each of the driver ends. V_+ and V_- can be determined as

$$V_+ = V_{in}(s)/2 \quad and \quad V_- = e^{-2\gamma l}V_{in}(s)/2, \tag{13}$$

where l is the length of the transmission line. c_1 and c_2 can be calculated based on V_+ and V_- as well as a_1 and a_2.

A. Coupling noise voltage at the driver end

For the near end coupling noise voltage V_{NE}, *i.e.*, $x = 0$,

$$\frac{V_{NE}(s)}{V_{in}(s)} = -\frac{l}{2}e^{-2\gamma l}\frac{s^2L_mC - s^2LC_m - sRC_m}{\gamma} + \frac{1}{8}(1 - e^{-4\gamma l})(\frac{sL_m}{R + sL} + \frac{C_m}{C}). \tag{14}$$

Assuming the input is a fast ramp signal, $v_{in}(t) = V_{dd}/\tau_r[tu(t) - (t-\tau_r)u(t-\tau_r)]$. The first constraint for τ_r is $\tau_r \leq \tau_0$, where τ_0 is the time of flight delay of the signal through the transmission line, $\tau_0 = l\sqrt{LC}$. This constraint requires that the interconnect inductance not be neglected. The second constraint is the assumption that $\omega L \gg R$. The frequency corresponding to this rise time is $\omega = 2\pi * 0.33/\tau_r = 2.0/\tau_r$ [11]. The requirement becomes $2\tau_1/\tau_r \gg 1$, where $\tau_1 = L/R$. $e^{-2\gamma l} \approx e^{-2s\tau_0 l - Rl/Z_0}$, where Z_0 is $\sqrt{L/C}$ – the characteristic impedance of a lossless transmission line. Using the approximation of γ in (12) and an inverse Laplace transform, the driver end coupling noise voltage $V_{NE}(t)$ in the time domain is

$$V_{NE}(t) = -\frac{\tau_0 e^{-\frac{Rl}{Z_0}}V_{dd}}{2\tau_r}V_{n1}(t) + \frac{V_{dd}}{8\tau_r}V_{n2}(t),$$
$$V_{n1}(t) = \frac{L_m}{L}V_{n3}(t) - \frac{C_m}{C}V_{n4}(t) - \frac{C_mR}{2CL}V_{n5}(t),$$
$$V_{n3}(t) = e^{-\frac{t-2\tau_0}{2\tau_1}}u(t-2\tau_0) - e^{-\frac{t-2\tau_0-\tau_r}{2\tau_1}}u(t-2\tau_0-\tau_r),$$
$$V_{n4}(t) = u(t-2\tau_0) - u(t-2\tau_0-\tau_r),$$
$$V_{n5}(t) = V_{n8}(t-2\tau_0),$$
$$V_{n2}(t) = V_{n6}(t) - e^{-\frac{2Rl}{Z_0}}V_{n6}(t-4\tau_0),$$
$$V_{n6}(t) = \frac{L_m}{L}(V_{n7}(t) - V_{n7}(t-\tau_r)) + \frac{C_m}{C}V_{n8}(t),$$
$$V_{n7}(t) = \tau_1(1 - e^{-\frac{t}{\tau_1}})u(t),$$
$$V_{n8}(t) = tu(t) - (t-\tau_r)u(t-\tau_r). \tag{15}$$

B. Coupling noise voltage at the receiver end

For the far end coupling noise voltage V_{FE}, where $x = l$,

$$\frac{V_{FE}(s)}{V_{in}(s)} = -\frac{l}{2}e^{-\gamma l}\frac{s^2L_mC - sRC_m - s^2LC_m}{\gamma} + \frac{1}{4}(e^{-\gamma l} - e^{-3\gamma l})(\frac{sL_m}{R+sL} + \frac{C_m}{C}). \quad (16)$$

For a fast ramp input signal, the approximation of γ in (12) and $V_{in}(s)$ are inserted into (16), permitting an inverse Laplace transform to be used to determine the receiver end coupling noise voltage $V_{FE}(t)$ in the time domain.

$$\begin{aligned}
V_{FE}(t) &= -\frac{\tau_0 e^{-\frac{Rl}{2Z_0}}V_{dd}}{2\tau_r}V_{f1}(t) + \frac{V_{dd}}{4\tau_r}V_{f2}(t),\\
V_{f1}(t) &= \frac{L_m}{L}V_{f3}(t) - \frac{C_m}{C}V_{f4}(t) - \frac{C_mR}{2CL}V_{f5}(t),\\
V_{f3}(t) &= e^{-\frac{t-\tau_0}{2\tau_1}}u(t-\tau_0) - e^{-\frac{t-\tau_0-\tau_r}{2\tau_1}}u(t-\tau_0-\tau_r),\\
V_{f4}(t) &= u(t-\tau_0) - u(t-\tau_0-\tau_1),\\
V_{f5}(t) &= (t-\tau_0)u(t-\tau_0) - (t-\tau_1-\tau_0)u(t-\tau_0-\tau_1),\\
V_{f2}(t) &= e^{-\frac{Rl}{2Z_0}}V_{f6}(t-\tau_0) - e^{-\frac{3Rl}{2Z_0}}V_{f6}(t-3\tau_0),\\
V_{f6}(t) &= \frac{L_m}{L}(V_{f7}(t) - V_{f7}(t-\tau_r)) + \frac{C_m}{C}V_{n8}(t), \quad (17)
\end{aligned}$$

and $V_{f7}(t) = V_{n7}(t)$.

III. Comparison with Simulation

To verify the accuracy of the analytical expressions, (15) and (17), to describe the coupling noise voltage at both ends of a quiet line, a criterion is defined to measure the error of these closed form approximations. This criterion quantifies the error between the predicted peak noise voltage and the simulated peak noise voltage, permitting the accuracy of these analytical equations to be determined. The criterion is defined as

$$\epsilon_{peak} = |V_p - V_s|/|V_s|, \quad (18)$$

where V_p is the value of the peak noise voltage predicted by the analytical expressions, and V_s is the peak noise voltage obtained by a circuit simulator (SPICE).

The parameters used in the SPICE simulation are $R = 3\ \Omega/cm$, $C = 1\ pF/cm$, $L = 2\ nH/cm$, $L_m/L = 0.2$, $C_m/C = 0.1$, $l = 2\ cm$, $V_{dd} = 5.0\ V$, $\tau_r = 120\ ps$, and $N = 20$. The value of two linear resistors, which are used to approximate the driver output impedance, is $R_1 = R_2 = \sqrt{L/C} = 44.72\ \Omega$. Both the analytical and simulation results are depicted in Figs. 2 and 3 for the driver end and the receiver end coupling noise voltage, respectively. The error of the peak noise voltage is within 6.0% at the driver end and less than 1.0% at the receiver end.

IV. Discussion

The validity of these analytical expressions are investigated in this section based on certain assumptions. The fast ramp input constraint, *i.e.*, the high frequency assumption, permits the interconnect to be modeled as a low loss transmission line, and the matched load condition at the driver end permits the use of the inverse Laplace transform to obtain explicit solutions in the time domain.

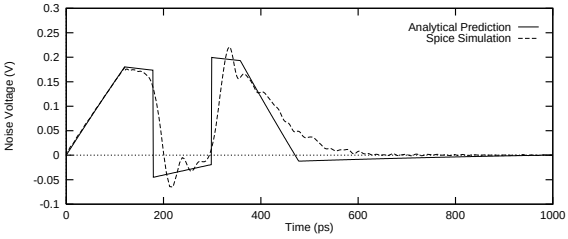

Fig. 2. Coupling noise voltage at the driver end

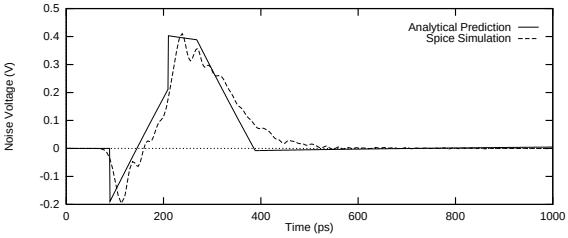

Fig. 3. Coupling noise voltage at the receiver end

A. Low loss or high frequency assumption

The rise time constraint, *i.e.*, $\tau_r < \tau_0$, is the condition that the interconnect inductance must be included in the interconnect model. If $2\tau_1/\tau_r \gg 1$, *i.e.*, $\omega L > R$ — the assumption made in (12), the interconnect should be modeled as a low loss transmission line under the high frequency condition. Two different regions of operation are defined for medium and high frequencies: condition 1 — medium frequency: $\tau_1/\tau_r = 2$, and condition 2 — high frequency: $\tau_1/\tau_r = 4$. The total line resistance (Rl) is varied from 0 to $1.0Z_0$ for each condition to test for low and high loss conditions. The error of the peak noise voltage calculation as compared to SPICE is shown in Figs. 4 and 5 at the driver end and the receiver end, respectively. The horizontal axis is the ratio of Rl/Z_0. The error is within 20% at the driver end and 15% at the receiver end for the worst case, *i.e.*, $Rl/Z_0 = 1.0$. If the interconnect is modeled as a high loss transmission line ($Rl \leq 1.0Z_0$), these analytical equations can accurately predict the peak noise voltage.

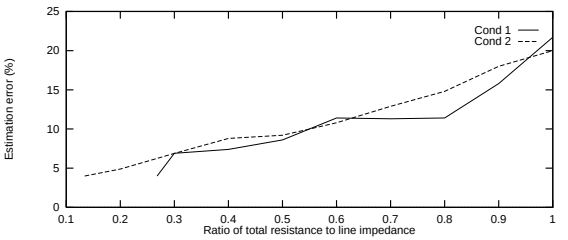

Fig. 4. Estimation of peak noise voltage of different lossy interconnect lines at the driver end. The solid line (Cond 1) is the condition $\tau_1/\tau_r = 2$, and the dashed line (Cond 2) is the condition $\tau_1/\tau_r = 4$.

B. Output impedance of the CMOS driver stage

A second assumption is that the driver impedance matches the line impedance. The following analysis investigates the coupling noise voltage under the condition of a varying driver to load impedance ratio.

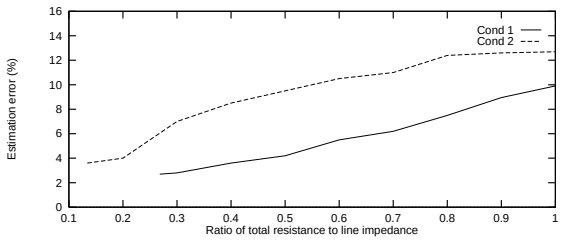

Fig. 5. Estimation of peak noise voltage of different lossy interconnect lines at the receiver end. The solid line (Cond 1) is the condition $\tau_1/\tau_r = 2$, and the dashed line (Cond 2) is the condition $\tau_1/\tau_r = 4$.

B.1 Propagation delay versus the driver impedance

The driver impedance in terms of the propagation delay is shown in Fig. 6. Note that the lower the driver impedance, the shorter the propagation delay. However, if the driver impedance is less than the interconnect impedance, a negative reflection occurs at the active driver end, and overshoots (the signal rises above the power supply voltage V_{dd}) or undershoots (the signal falls below ground) occur. The overshoot (undershoot) may cause the drain of the PN junction of the PMOS (NMOS) transistor to be forward biased, collecting (injecting) electrons into the substrate, dissipating extra power [6], and delaying the time response. The output voltage of the active driver stage oscillates due to reflections at both ends of the active line before a final steady state voltage is reached.

Fig. 6. Propagation delay of the active CMOS driver stage versus the driver stage output impedance

B.2 Relaxation time versus the driver impedance

Another effect of the low driver impedance is that the relaxation time, the time required for a signal to reach the steady state voltage of the coupling noise voltage at the quiet line, increases. The relationship between the relaxation time of the coupling noise voltage and the active driver impedance is shown in Fig. 7. The waveform of the coupling noise voltage on the quiet line is strongly dependent on the transition occurring on the active line. Therefore, the shortest relaxation time occurs when the active driver impedance matches the line impedance, where no reflections occur at the driver end on the active line. The relaxation time of the coupling noise voltage increases as the driver impedance deviates from the matched load condition.

B.3 Non-matching driver impedance

The peak noise voltage for a variety of driver impedances is shown in Fig. 8. The peak noise voltage decreases as the driver impedance increases. The maximum error of the peak noise voltage as compared to SPICE simulation is less than 15% at the driver end and within 20% at the receiver end of the quiet line where the driver impedance is in the range of $0.8Z_0$ to $2.0Z_0$. These analytical equations, (15) and (17), can therefore be used as a first order approximation to predict the coupling noise voltage in high speed CMOS VLSI circuits.

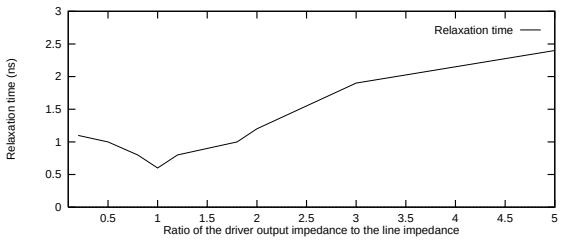

Fig. 7. Relaxation time of the coupling noise on the quiet line versus the driver impedance

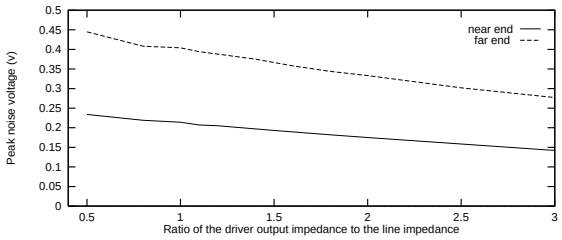

Fig. 8. Peak noise voltage versus the driver impedance

V. Conclusion

Closed from expressions for the peak coupling noise voltage between two neighboring interconnect lines in CMOS VLSI circuits have been presented for different load and waveform conditions. These analytical equations provide an estimate of the noise with an error within 20% at both ends of the quiet line.

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