Performance Criteria for Evaluating the Importance of On-Chip Inductance

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Abstract

Two figures of merit are presented for determining whether a section of interconnect should be modeled as either an *RLC* or an *RC* impedance. The attenuation that a signal undergoes as it propagates a distance equal to the length of the interconnect line is shown to be a useful figure of merit. The second figure of merit considered in this paper is the ratio of the rise time of the input signal at the driver of an interconnect line to the time of flight of the signals across the line. Circuit simulations of an *RLC* transmission line and a five section *RC* Π circuit are used to quantify and determine the relative accuracy of an *RC* model. One primary result of this study is evidence demonstrating that a range of interconnect length exists for which inductance effects are prominent. It is also shown that under certain conditions, inductance effects are negligible despite the length of the section of interconnect.

I. Introduction

It has become well accepted that interconnect delay dominates gate delay in current deep submicrometer VLSI circuits [1]-[3]. With the continuous scaling of technology and increased die area, this situation is expected to become worse. In order to properly design complex circuits, more accurate interconnect models and signal propagation characterization are required. Historically, interconnect has been modeled as a single lumped capacitance in the analysis of the performance of on-chip interconnects. With the scaling of technology and increased chip size, the crosssectional area of wires has been scaled down while interconnect length has increased. The resistance of the interconnect has therefore become significant, requiring the use of more accurate *RC* impedance models. Interconnect is typically modeled as a lumped *RC* circuit. To further improve accuracy, the interconnect has been modeled as a distributed *RC* impedance (multiple T or Π sections) for those nets requiring more accurate delay models. A well known method used to determine which nets require more accurate delay models is to compare the driver resistance R_t and the load capacitance C_L to the total resistance and capacitance of the section of interconnect, R_t and C_t [4], [5]. Those nets that require more accurate *RC* models are more highly resistive.

Currently, inductance is becoming more important with faster on-chip rise times and longer wire lengths. Wide wires are frequently encountered in clock distribution networks and in upper metal layers. These wires are low resistance wires that can exhibit significant inductive effects. Furthermore, performance requirements are pushing the introduction of new materials for low resistive interconnect [6]. In the limiting case, high temperature superconductors may become commercially available [7]. With these trends it is becoming crucial to be able to determine which nets within a high speed VLSI circuit exhibit prominent inductive effects.

The focus of this paper is the introduction of simple figures of merit that can be used as criteria to determine which nets require more accurate transmission line models. A closed form solution for the output signal of a CMOS inverter driving an *RLC* transmission line based on the alpha power law [8] for deep submicrometer (DSM) technologies is presented in section II. The attenuation constant of an *RLC* transmission line and the rise time of the input signal at the driver of the interconnect are used to derive two figures of merit that describe the relative significance of inductance of a local interconnect line. These figures of merit are also presented in section II. Finally, some conclusions are offered in section III.

II. Analysis of inductance effects in *RLC* interconnect

The attenuation constant α of an *RLC* transmission line [9] can be derived from the basic equations and is

$$\alpha = \omega\sqrt{LC}\sqrt{\frac{1}{2}\left(\sqrt{\left(1+\left(\frac{R}{\omega L}\right)^2\right)}-1\right)}, \tag{1}$$

where R, L, and C are the resistance, inductance, and capacitance per unit length, respectively.

The attenuation constant as a function of frequency is plotted in Fig. 1 with $L=10^{-8}$ *H/cm*, $R=400$ *Ω/cm*, *and* $C=10^{-12}$ *F/cm* [10]. The attenuation constant saturates with increasing frequency to an asymptotic value given by

$$\alpha_{asym} = \frac{R}{2}\sqrt{\frac{C}{L}}, \tag{2}$$

and the radial frequency at which this saturation begins is given by

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$$\omega_{asym} \approx \frac{R}{L}. \tag{3}$$

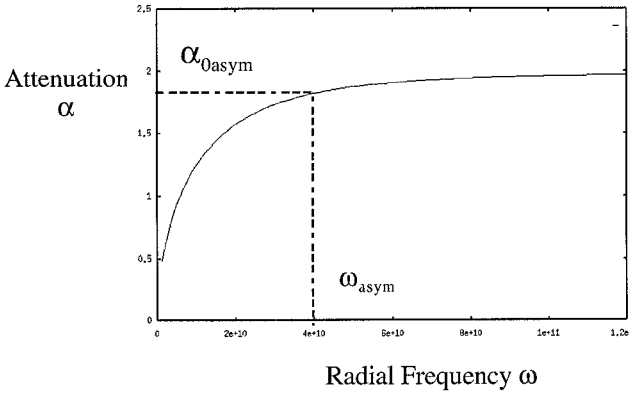


Fig. 1. The attenuation constant α verses the radial frequency ω.

The characteristic impedance of an *RLC* transmission line is complex with a portion that is negative and imaginary. Therefore, the characteristic impedance looks like a resistance in series with a capacitance. Thus, the characteristic impedance can be expressed as

$$Z_0 = R_0 - j\frac{1}{\omega C_0}, \tag{4}$$

where R_0 and C_0 are given by

$$R_0 = \sqrt{\frac{L}{C}}\sqrt{\frac{1}{2}\left(\sqrt{\left(1+\left(\frac{R}{\omega L}\right)^2\right)}+1\right)}, \tag{5}$$

$$C_0 = \frac{1}{\omega\sqrt{\frac{L}{C}}\sqrt{\frac{1}{2}\left(\sqrt{\left(1+\left(\frac{R}{\omega L}\right)^2\right)}-1\right)}}. \tag{6}$$

Both R_0 and C_0 saturate to the asymptotic values given by

$$R_{0asym} = \sqrt{\frac{L}{C}}, \tag{7}$$

$$C_{0asym} = \frac{2\sqrt{LC}}{R}, \tag{8}$$

where the saturation frequency is given by (3).

An *RLC* transmission line driven by a CMOS inverter can be approximated at high frequency as shown in Fig. 2, for the period of time, $0<t<2T_0$, where T_0 is the time required for the waves to travel a distance equal to the length of the transmission line. T_0 is frequently described as the time of flight of the transmission line. The input is assumed to be a ramp with a fall time t_f. The asymptotic values for the characteristic impedance and the attenuation are assumed in the following analysis. The technology used in this analysis is a 0.25 μm CMOS technology with a 2.5 volt power supply. The alpha power law is used to characterize the devices [8]. A pulse is generated at V_{out} for the period of time $0<t<2T_0$, where the time reference is chosen when the input signal reaches $V_{DD}+V_{Tp}$ where V_{Tp} is the threshold voltage of the P-channel devices and for an enhancement mode device is negative. Under the aforementioned conditions and the assumption that the PMOS transistor is saturated and neglecting the effect of the NMOS transistor, V_{out} is given by

$$V_{out}(t) = P_{Cp}\frac{W_p}{L_p}(V_{in}(t))^{\alpha p}\left[\sqrt{\frac{L}{C}}+\frac{Rt}{2\sqrt{LC}}\right]u(t) = P(t), \tag{9}$$

for $0<t<2T_0$, where $u(t)$ is the unit step function.

The pulse propagates across the transmission line. At the load, the signal is completely reflected assuming an open circuit (or a small load capacitor) at the end of the line. This reflected signal propagates back towards the driver and reaches the driver at a time $t = 2T_0$. After this round trip is completed, the pulse that reaches the source is attenuated by a factor of $e^{-2\alpha l}$ and can be described mathematically by $P(t-2T_0)\cdot e^{-2\alpha l}$. As long as the transistor is in saturation, the transistor maintains a relatively constant current. Thus, the current reflection coefficient is -1 and consequently the voltage reflection coefficient is 1. Therefore the pulse is multiplied by 2. This cycle repeats as long as the transistor is saturated. The complete solution for the period when the transistor is saturated is

$$V_{out}(t) = P(t) + \sum_{i=1}^{n}\left[2P(t-2nT_0)e^{-2\alpha nl}\right], \tag{10}$$

for $2nT_0<t<2(n+1)T_0$. This solution is compared to an *RC* representation of the line, as shown in Fig. 3.

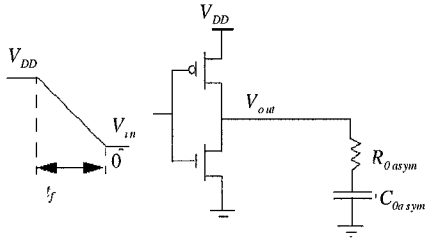


Fig. 2. A CMOS inverter driving the equivalent characteristic impedance of an *RLC* transmission line.

The solution for V_{out} using this model when the PMOS transistor is in saturation is

$$V_{out} = P_{Cp}\frac{W_p}{L_p}(V_{in}(t))^{\alpha p}\left[\frac{Rl}{2}+\frac{t}{Cl}\right]. \tag{11}$$

The analytical solution in (10) is compared with AS/X simulation [14] results for the *RLC* transmission line shown in Figs. 4 and 5, with $L=10^{-7}$ *H/cm* and $C=10^{-12}$ *F/cm*. The analytical solution agrees with the simulations of an *RLC* transmission line for a wide variety of interconnect resistances and input fall times. As implied by the analytical solution, the output signal follows the changing input signal. The period when the input signal is falling represents the fast rising parts of the response that depend on the transition time of the input signal. Once the input signal is settled, the current provided by the transistor is constant and the output signal changes slowly due to the charging of the equivalent capacitor of the transmission line. This period of time represents the slow rising part of the response that depends upon the value of the

equivalent capacitance of the transmission line. Note in Fig. 4 that as R increases, the slope of those portions of the response increases since the value of the equivalent capacitor decreases, as given by (8).

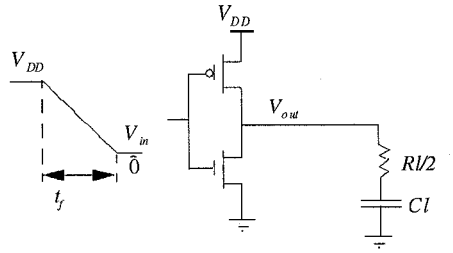
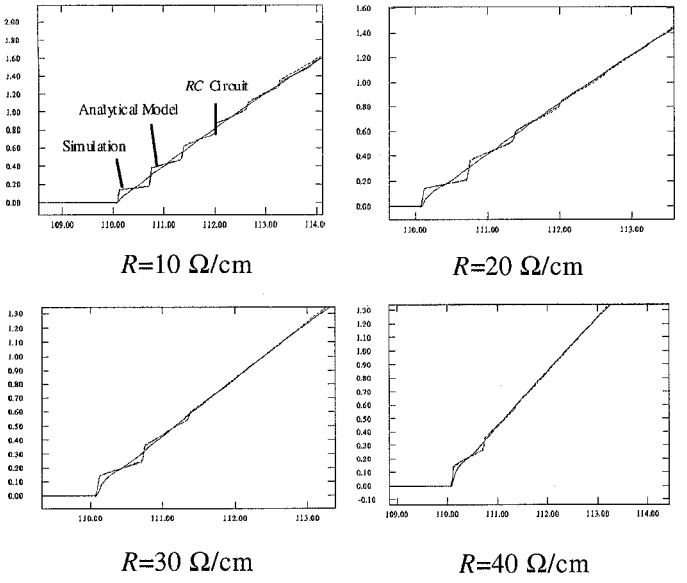


Fig. 3. A CMOS inverter driving an RC approximation of an interconnect line.



R=10 Ω/cm R=20 Ω/cm

R=30 Ω/cm R=40 Ω/cm

Fig. 4. Analytical solution in (10) compared to AS/X simulations and a five section RC Π circuit. The fall time of the input signal is held constant at 60 ps, while R is varied.

The output response of the RLC transmission line tracks the output response of the RC circuit. The points of intersection with the RC response can be calculated by equating (10) and (11), and are given by

$$t_n = \frac{\left[T_0(2K_n - 1) + 4T_0\xi \cdot \frac{dK_n}{d(2\alpha l)} - \frac{RCl^2}{2}\right]}{\left[1 - \xi(2K_n - 1)\right]}, \qquad (12)$$

where K_0=1 and

$$K_n = \frac{e^{-2\alpha l(n+1)} - 1}{e^{-2\alpha l} - 1} \qquad n=1,2... \qquad (13)$$

The interesting point to note is that those times at which the RC response intersects the RLC transmission line response are not dependent on the transition time of the input signal. This characteristic can be observed in Fig. 4. Thus, as the attenuation across the transmission line increases, the reflected signals become smaller. Since the times at which the RLC response intersect with the RC response are constant, the RLC transmission line response approaches the RC circuit response. A figure of merit to characterize the importance of inductance can be derived from this observation and is given by

$$\alpha_{asym} l = \frac{Rl}{2}\sqrt{\frac{C}{L}} < 1. \qquad (14)$$

When this inequality is satisfied, inductance becomes important. This relationship is physically intuitive, since ξ represents the degree of attenuation the wave suffers as it propagates a distance equal to the length of the line. As this attenuation increases, the effects of the reflections decrease and the RC model becomes more accurate. Therefore ξ is a useful figure of merit that anticipates the importance of considering inductance in a particular interconnect line. This figure of merit is the same parameter described in [11] and [12] but is derived in a different way. Note that if (14) is squared, this figure of merit compares the time constant L/R to the time constant RC, which is the same result described in [1], [3], and [13].

As the transition time of the input signal increases, the slope of the fast changing portions of the response decreases, which reduces the width of the slowly varying parts of the response. This behavior makes the response of the RLC transmission line appear more continuous. Since the times at which the RLC response intersect with the RC response are constant, the RLC transmission line response approaches the RC circuit response.

As the transition time of the input signal becomes equal to or greater than $2T_0$, the slowly varying portions of the RLC transmission line response disappear, and the response coincides with the RC approximation. This behavior is evident from Fig. 5 which leads to the second figure of merit given by

$$t_r < 2l\sqrt{LC}. \qquad (15)$$

When this inequality is satisfied, inductance becomes important. Note that the figure of merit in (15) is accurate only if the line is matched (the width of the transistor driving the line is adjusted to match the transistor output impedance with the load impedance of the line) or underdriven (the width of the transistor driving the line is less than is necessary to make the transistor impedance match the load impedance). However, this condition does not affect the validity of the results since in most practical cases, it is undesirable to overdrive the line (using a transistor wider than the matched size). If the line is overdriven, overshoots occur which degrade performance. Also, to overdrive the line, wider transistors are needed which places a larger capacitive load on the previous stage. It can also be seen that as the resistance of the line increases, the attenuation of the reflections increases, which makes the RC response approach the RLC transmission line response.

The two figures of merit in (14) and (15) can be combined into a two sided inequality that determines the range of the

length of interconnect in which inductance effects are significant. This condition is given by

$$\frac{t_r}{2\sqrt{LC}} < l < \frac{2}{R}\sqrt{\frac{L}{C}}. \quad (16)$$

This range depends upon the parasitic impedances of the interconnect per unit length as well as on the rise time of the signal at the input of the CMOS circuit driving the interconnect. In certain cases, this range can be non-existent if the following condition is satisfied,

$$t_r > 4\frac{L}{R}. \quad (17)$$

In this case, inductance is not important for any length of interconnect. For short lines, the time of flight across the line is too small compared to the transition time of the input signal. As the line becomes longer, the attenuation becomes large enough to make the effects of the inductance negligible. If the effect of the attenuation comes into play before the effect of the rise time vanishes, the inductance is not important for any length of interconnect.

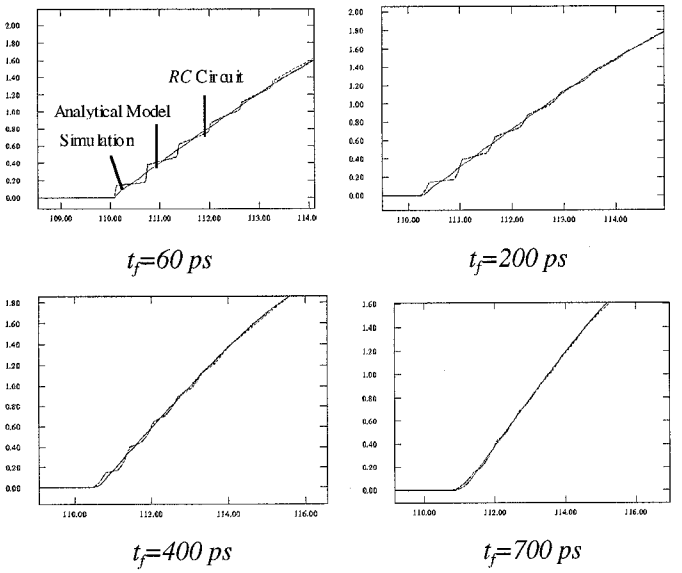


Fig. 5. Analytical solution in (10) compared to AS/X simulations and a five section *RC* Π circuit. *R* is held constant at *10* Ω/cm, while the fall time of the input signal is changed.

III. Conclusions

A closed form solution for the output response of a CMOS inverter driving an *RLC* transmission line is presented using the alpha power law for deep submicrometer CMOS. Simple to use figures of merit have been developed that determine the relative accuracy of an *RC* model to model on-chip interconnect. The range of length of interconnect where a more accurate transmission line model becomes necessary is presented based on the parasitic impedances of the line (*R*, *L*, and *C*) and the rise time of the input signal of the gate driving the line. AS/X simulations exhibit good agreement with these figures of merit. These figures of merit can be used to determine which nets needs to be modeled as inductive transmission lines. These figures of merit can also be used to properly size the interconnect and buffers along a line during the initial design phase of a high frequency circuit.

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