NOTE TO USERS

Noise Issues in Mixed-Signal Integrated Circuits

by

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Submitted in Partial Fulfillment
of the
Requirements for the Degree
Doctor of Philosophy

Supervised by
Professor Eby G. Friedman

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Rochester, New York

2004

Dedication

To my wife Jing Liu, son Barry, and daughter Emily.

Curriculum Vitae

The author was born in Nanjing, China on October 13, 1961. From 1978 to 1982, he studied at the Department of Electrical Engineering, Nanjing Institute of Post and Telecommunications where he received his B.S. degree in Electrical Engineering. After graduation, he worked for four years as an assistant engineer at Nanjing General Semiconductor Device Plant in China on process development and circuit design of NMOS ICs. From 1986 to 1990, he was a research engineer at the Solid-State Device Research Institute, Nanjing, China working in the area of millimeter wave and microwave power transmitters (MMIC). He came to the University of Rhode Island in September 1990, where he received his Masters degree in Electrical Engineering in 1993.

He was with TCI Corporation from 1993 to 1997 in Boston, Massachusetts and Philadelphia, Pennsylvania, working on the design of linear CCD and TFT LCD displays, respectively. He joined the Eastman Kodak Company, Rochester, New York in 1997. He is now a senior IC design engineer at Kodak, working on the design of CMOS mixed-signal integrated circuits.

He is currently completing his Ph.D. degree in the area of substrate coupling noise test and analysis at the University of Rochester.

Acknowledgments

I would like to express my sincere gratitude towards Professor Eby G. Friedman, my academic advisor. Through his continuous and enthusiastic encouragement, Professor Friedman guided me across the bridge connecting engineering and academic research. He has spent countless hours discussing with me research ideas and teaching me how to improve my presentation skills and academic writing style.

I would like to thank Professors Mark J. Bocko, Christopher M. Brown, and Hui Wu for acting as members of my Ph.D. committee. I would also like to thank RuthAnn Williams for her administrative support.

I would like to express my special thanks to my wife Jing Liu for her incredible support and understanding through the years of my graduate studies at the University of Rochester. I would also like to promise my son Barry and daughter Emily more time together with them.

My appreciation goes to Eastman Kodak for providing me with full support both financially and technically during the years of my part time Ph.D. studies. My research work would have taken much longer time without the support from Kodak

in the area of design tools, chip fabrication, and laboratory testay. Special thanks to my colleagues at the University of Rochester, Andrey Mezhiba, Volkan Kursun, Boris Andreev, Dimitris Velenis, Magdy El-Moursy, Junmou Zhang, Mikhail Popovich, Guoqing Chen, Jonathan Rosenfeld, and Vassilis Pavlidis for their help and discussions. I would also like to thank my colleagues at Eastman Kodak, Mike Mattern, Mike Guidash, Simon Cooper, Bruce Johnson, Ravi Mruthyunjaya, David Madziarz, David Sacktte, Bruce McDemott, Michael Shamberger and all who gave their kind help and support.

Abstract

Complex high-speed digital circuits are commonly integrated together with high performance analog circuits onto the same substrate. In such mixed-signal systems, fast switching transients produced by digital circuits can couple into sensitive analog components through both the substrate and line-to-line capacitances, thereby limiting the achievable analog precision. Furthermore, performance degradation caused by substrate and capacitive coupling noise is difficult to control and even more difficult to predict. The need for highly accurate noise measurement to identify and manage noise has therefore become increasingly evident.

An analysis of clock feedthrough in CMOS analog transmission gate switches is presented in this dissertation. A clock feedthrough mechanism and a related model of a transmission gate switch are established in the current-voltage domain. Region and zone maps of the transmission gate during switch-off are developed and used to efficiently estimate clock feedthrough noise.

The charge-sharing effect (CSE) in switched-capacitor CMOS circuits is studied and evaluated. A technique using Miller capacitance in a sample-and-hold circuit is introduced to reduce the charge sharing effect caused by the parasitic capacitances and clock feedthrough from a sampling switch. A ten-fold reduction in CSE and clock feedthrough is achieved.

An on-chip circuit has also been developed to directly measure substrate and line-to-line coupling noise voltages and waveforms. This test circuit has been manufactured in a 0.35 μm CMOS process and consists of noise generators and switched-capacitor signal processing circuitry. The experimental data show that on-chip generators ranging in area from 1 μm^2 to 6 μm^2 produce noise at the receiver, decreasing from 3.14 mV/μm to 0.73 mV/μm. The efficiency with which including substrate guard rings reduces substrate noise has also been studied and evaluated in this research effort. Supported by experiment measurement, open loop and closed guard rings reduce the noise by 20% and 85%, respectively. The difference between experimental and analytic models of the line-to-line coupling capacitance ranges from 8.5% to 17.7% for different metal layers.

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Chapter One: Introduction

From Bell Labs inventing the transistor in 1947 to today's deep submicrometer CMOS processes and systems-on-a-chip integration, the semiconductor industry has experienced a rapid pace of improvement during the past four decades. Texas Instrument built the first integrated circuit in 1961, Gordon Moore in 1965 predicted exponential growth (biannual doubling) known as "Moore's Law," and Intel in 1971 invented the SRAM and EPROM and introduced the microprocessor 4004. With reduced feature sizes and power supply voltages, and higher levels of integration, characterizing noise in integrated circuits has become increasingly difficult and important. In this chapter, the development of microelectronics is briefly reviewed in sections 1.1 and 1.2. Difficulties in modeling and testing analog ICs (integrated circuits) are also discussed in section 1.3. The cause for the mergence of mixed-signal ICs is reviewed and noise measurement in mixed-signal ICs is discussed in sections 1.4 and 1.5, respectively. Each chapter in this research proposal is introduced at the end of this chapter.

1.1. Development of the Integrated Circuit

The first transistor, the point-contact transistor, was invented by Bardeen and Brattain of Bell Telephone Laboratories in 1947 [1]. The first field-effect transistor (FET) was reported by Shockley in 1952 [2]. Metal Oxide Silicon (MOS) devices began taking a major role after the invention of the planar silicon process around 1960. Although the first MOS calculator was introduced in 1965, the commercial use of a MOS device was only limited to a few applications until 1967 due to silicon material and quality control problems. Even then, single-polarity p-type transistors were favored until the emergence of MOS silicon-gate transistor technology about 1971. The use of both polarity devices on the same substrate was invented by at least two people in the early 1960s. P. K. Weimer of RCA filed a patent on May 31st, 1962 [3]. Frank Wanlass of Fairchild Semiconductor Research and Development filed a patent on June 18th, 1963 that covered the CMOS concept [4]. The first microprocessor was developed in 1974. Since then, the performance, density, die size, and speed of ICs have experienced a dramatic growth due to rapid technological advances. During the past two decades, processor clock frequencies have been increasing at an average rate of about 1.25X per year. Transistor counts have been increasing at a steady rate of about 1.4X per year, while die size has been increasing at about 1.15X per year [5].

1.2. IC Generations and Scaling of Semiconductor Processing Technologies

These trends were clearly defined by Gordon Moore in 1960s and captured as Moore's Law. The current version of Moore's law is that succeeding generations will support a four times increase in circuit complexity, and new generations will emerge on an approximately two or three year interval. The associated observations are that the linear dimensions of device features change by a factor of 0.7 and the economically viable die size grows by a factor of 1.6 [6]. The minimum feature size stated in micrometers is the unit that is most frequently used to label a technology generation (or technology node). An individual device generation has been observed to have a reasonably well-defined life cycle that covers about 17 years. Usually, the first three to five years are university research, the second three to five years are industrial research, the third period of about four years is industrial development, and the last four to five years are the volume manufacturing phase. The first year of volume manufacture is the reference point for a generation.

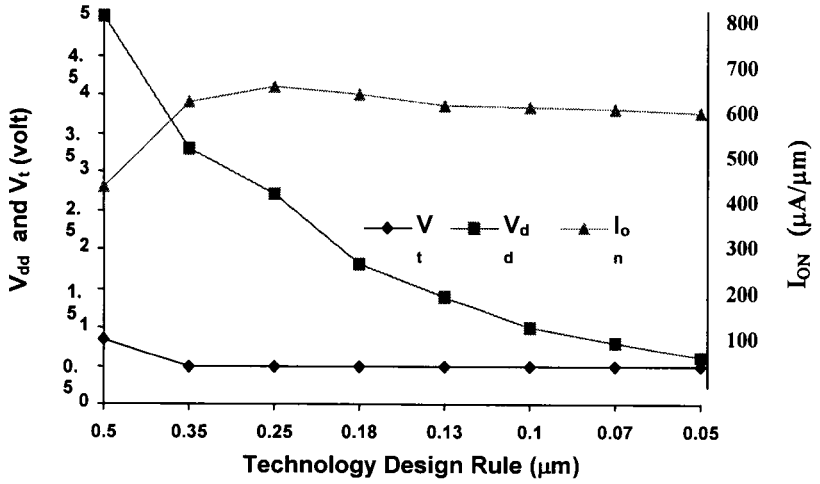


Figure 1-1: Scaling of conventional CMOS ICs

Scaling of CMOS technologies has defied all predictions of technology limitations, and continues beyond the deep submicrometer minimum feature size. The scaling of conventional MOSFETs, however, is facing several problems arising from reduced power supply voltages and a rapidly decreasing gate oxide thickness.

Table 1-1: Summary of 2000/2001 SIA Roadmap [a]

Year	**Unit**	**1993**	**1995**	**1999**	**2001**	**2003**	**2005**	**2008**	**2011**	**2014**	**2016**
Feature Size	*Nanometers*	500	350	180	130	100	80	70	50	34	22
Internal Clock (high performance)	*GHz*	0.2	0.3	0.75	1.68	2.31	5.17	6.74	11.5	19.3	28.7
Logic transistors	*Million/cm^2*	2	4	6.6	13	24	44	109	269	664	
Microprocessor	*Million transistors/chip*	5.2	12	23.8	47.6	95.2	190	539	1523	4308	
DRAM size	*Gbit*	0.016	0.064	0.256	0.512	1	2	6	16	48	
SRAM size	*Mbit*	1	4	16	64	256					
Voltage	V_{dd}	5	3.3	2.5	1.2	1.0	0.9	0.7	0.6	0.5	0.4

1.3. Difficulties in Characterizing Analog Circuit Technologies

Different from digital ICs, the design of analog integrated circuits is tightly dependent upon the manufacture process parameters. The accuracy of modeling these process related parameters directly affects the performance and yield of analog ICs. In the following subsections, difficulties in device characterization for analog circuits are discussed.

[a] http://public.itrs.net/Files/2001ITRS/ORTCTables.pdf

1.3.1. Subthreshold characteristics of MOSFET's are difficult to model

In sampled data circuits, subthreshold conduction of switches in the off state, particularly at high temperatures, may lead to significant leakage, thereby corrupting the stored information. This effect also becomes important in determining the lower bound on the speed of dynamic latches in mixed-signal and digital circuits. A difficulty in subthreshold modeling is DC and AC slope discontinuity in the vicinity of strong inversion as V_{GS} increases. Substantial dynamic errors are exhibited in the time-domain simulation of circuits in which MOSFETs operate between the linear and saturation regions. This issue remains unresolved in most mainstream device models.

1.3.2. Modeling of output resistance of short-channel MOS transistors

Another troublesome effect is the output resistance of short-channel MOS transistors and, in particular, the variation of the output resistance with the drain-to-source voltage in the saturation region. This effect causes the intrinsic gain gmro to behavior nonlinearly, thereby creating nonlinearity in the amplifiers.

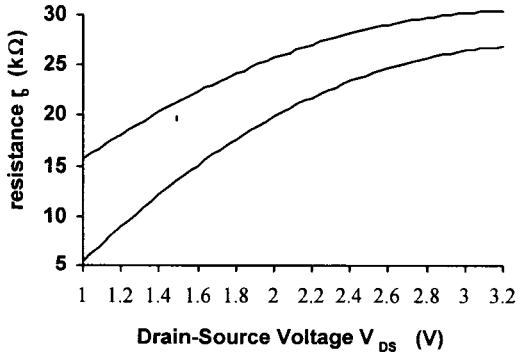


Figure 1-2: Transistor output impedance

1.3.3. Modeling of the capacitance of the well-to-substrate

A rarely available process parameter is the capacitance of the well-to-substrate. If the source and n-well of a PMOS (or p-well of a NMOS) device are connected to avoid the body effect, the n-well capacitance must be considered. The capacitance of the resistor made from the well may also be important.

1.3.4. Linearity of Passive Devices

Linearity of both passive and active devices plays a critical role in many analog circuits. Nonlinear terms appear in the device values as $x \approx x_0 \cdot \left(1 + \alpha_1 V + \alpha_2 V^2\right)$. x0 is the ideal device value, and $\alpha 1$ and $\alpha 2$ are coefficients of the nonlinear terms. The coefficients α1 and α2 are measured for different types of resistors and capacitors available in a process. The linearity of polysilicon resistors, however, typically improves with the length [8].

1.3.5. Modeling of MOSFET Transconductance

MOS transistors are voltage controlled current devices. The transconductance is an important parameter of a MOSFET. With the scaling of process feature sizes, the effective transconductance of a MOSFET is strongly affected. Modeling of the MOSFET effective transconductance has become significantly more difficult. Experimentally derived MOSFET current versus the effective channel length and gate oxide thickness is shown in Fig. 1.3. The data are in good agreement with the theoretical model [9].

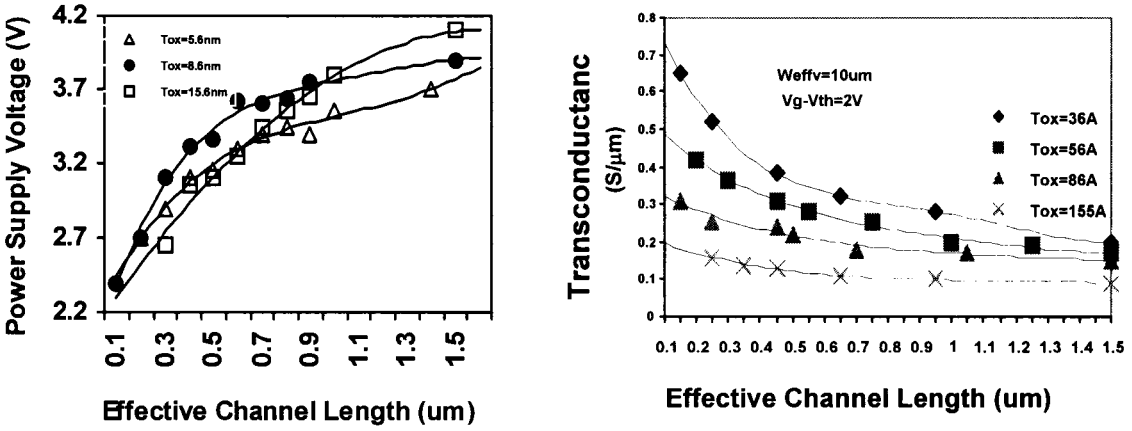


Figure 1-3: MOSFET Ttransconductance vs effective channel length

1.4. Fabricating Analog and Digital circuits on the Same Substrate: Mixed-Signal ICs

The evolution of scaled digital processes has shifted the boundary between the digital and analog parts of a system [10]. Although large electronic systems can be constructed almost entirely with digital techniques, many systems still require analog parts. Storage media, transmission media, and physical sensors are fundamentally analog in nature. The analog circuits will remain irreplaceable components of a System-On-a-Chip (SOC). In addition to analog-to-digital (A/D) and digital-to-analog (D/A) conversion circuits, analog circuits are required to perform a variety of critical tasks to interface digital circuits with the external world, such as amplification, prefiltering, demodulation, signal conditioning for

line transmission, storage, display, generation of absolute values (voltages, currents, frequencies), and to implement compatible on-chip sensors.

As CMOS technology continues to benefit from both scaling and the enormous momentum of the digital market, mixed-signal integrated circuits emerged around the early 1980's. With an increase in circuit size, the basic environment for a system-on-a-chip has become available. Many systems are integrated on a single IC in different areas, like medical audiometric system [11], telecommunication systems [12] [13], and imaging system [14] [15]. Analog-to-digital and digital-to-analog converters are commonly required in mixed-signal SOCs.

1.5. Analog and Mixed-Signal Circuit Noise Testing

A typical strategy for testing a mixed-signal IC involves, when possible, first individually testing the digital and analog components (these are test cells built on the same substrate). This effort is followed by certain system tests to evaluate the at-speed interaction among components. In this case, the digital parts are tested with standard methods, aided by software for automation test pattern generation, scan chains, and built-in self-test (BIST), which has become a mature and cost effective technology. Testing the analog parts and the combined system is less well understood [16]. Unlike digital signals, analog signals require significantly greater precision in the signal magnitude. Noise added at the input of an analog circuit is seen at the circuit output. Noise directly affects the performance and accuracy of

the test results of an analog circuit. Measuring noise in an analog circuit is important for improving circuit performance and reducing failure in mixed-signal ICs. Due to the generation mechanisms in ICs, these noise voltages are usually weak, making noise testing quite difficult.

1.6. Topics Presented in This Research Proposal

In this research proposal, some noise analysis and techniques for testing noise signals in mixed-signal ICs are presented. The research presented in this proposal focuses on the development of accurate noise signal measurement techniques for different types of noise sources in mixed-signal CMOS ICs. Basic noise sources and non-ideal factors in mixed-signal ICs are reviewed in Chapters 2 and 3, respectively.

In Chapter 4, a technique to accurately measure substrate coupling noise is proposed. On chip A/D conversion is used to minimize the signal contamination due to the parasitic impedances along an IC test path. An on chip circuit calibration is also used to further extend the accuracy.

A circuit used to test capacitive coupling noise between conductive lines is presented in Chapter 5. Capacitive coupling between different conductive layers can be accurately measured without the signal contamination from bonding wire to package fame and external test circuit.

In Chapter 6, an analysis of clock feedthrough in CMOS analog transmission gate (TG) switches is presented in this chapter in details. A model of clock feedthrough in analog transmission gate switches is established in the voltage/current domain. In this analysis, a region map is developed for the TG switch during the period when both devices are turned off. In the first region, full conduction (or strong inversion), both the PMOS and NMOS transistors operate in the linear region. The second region is a half conduction region where one MOSFET is in the linear region and the other transistor is either in the subthreshold region and/or the off state. In the third region, both of the MOSFETs are in the subthreshold/cutoff. The region map is further divided into zones. From these region and zone maps, the sign and relative magnitude of clock feedthrough noise can be efficiently estimated for different signal levels.

The parasitic capacitance affects the performance of the analog circuits, particularly switched-capacitor circuits. The charge sharing effect in CMOS switched-capacitor sample-and-hold (S/H) circuit is used as an example noise problem in Chapter 7.

A circuit technique based on the Miller effect to reduce the charge sharing effect noise and clock feedthrough noise in S/H circuit is proposed in Chapter 8. A compact cascode amplifier is used in the Miller feedback circuit. A ten times reduction in CSE and clock feedthrough is achieved. The S/H capacitor is split into two, Csh1 and Csh2, in the circuit. One of these S/H capacitors effectively reduces

the CSE while the other capacitor reduces clock feedthrough. Transistor mismatch affecting CMOS operational amplifiers is presented in Chapter 9.

The experimental data obtained from the test chip is presented and discussed in Chapter 10. A summary of this research is offered in Chapter 11. Future research in modeling substrate coupling and line-to-line capacitive coupling in mixed-signal ICs is described and suggested in Chapter 12.

Chapter Two: Noise Sources in Mixed-Signal CMOS ICs

Noise in various forms exists in all kinds of electronic systems such as integrated circuits. The noise can be random or fixed pattern, signal related or signal independent, and semiconductor process dependent or independent. In this chapter, common noise sources in mixed-signal CMOS ICs are reviewed. Noise in integrated circuits and electronic devices is briefly described in section 2.1. Random noise and some related characteristics are reviewed in section 2.2. Major types of random noise sources in CMOS ICs are described in section 2.3. Substrate noise, capacitive coupling, clock feedthrough, charge sharing effect, and power/ground noise are each reviewed in section 2.4.

2.1. Noise in Integrated Circuits and Electronic Devices

Noise can be described as any signal appearing at the output of an IC that is not predicted by a DC and AC input error analysis [17]. Noise can be random or repetitive, internal or external, current or voltage, narrow band or wide band, and high frequency or low frequency.

With the development in IC process technologies, many new challenges in analog and mixed-signal circuits have emerged due to the demands of modern electronic systems. With the extension of CMOS process technologies into the

UDSM (ultra-deep submicrometer) regime and the increasing popularity of battery-powered mobile electronic systems, the demand for low-voltage mixed-signal IC circuits has greatly increased. In addition, the drive to reduce system costs is forcing the integration of analog and digital circuitry onto a single die. Both of these changes have a significant impact on mixed-signal circuit performance. With the scaling of the power supply voltage, both the SNR (signal-to-noise ratio) and the dynamic range of an analog circuit have decreased. Integrating sensitive analog circuitry and noisy digital circuitry onto the same substrate further degrades the performance of the analog circuit due to noise injection through the substrate, the power supply, and/or the power distribution network, as well as capacitive coupling between conducting wires. In low voltage CMOS analog and mixed-signal integrated circuits, many noise mechanisms generate low frequency noise such as 1/f noise, wideband white noise such as shot noise, and thermal noise. These types of noise, as described in [18], together with other types of noise that are commonly found in mixed-signal CMOS ICs are reviewed in the following sections.

2.2. Random Noise

Electronic devices and circuits exhibit random fluctuations in the voltage (or current) at the terminals. Since the terminals exhibit unpredictable instantaneous values, these fluctuations are known as stochastic processes and are characterized in terms of the average or statistical properties. These fluctuations are usually

referred to as random noise [18]. The noise is inherent in the devices or circuits and can not be eliminated. The mean value and power spectral density are principal statistical quantities to characterize the random noise. The most important noise sources (thermal noise, shot noise, and 1/f noise) in electronic devices and circuits exhibit normal or Gaussian distributions [18] in the frequency domain as shown in (2-1).

$$F(x) = \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left\{-(x-\bar{x})^2 / 2\sigma^2\right\} \quad , \tag{2.1}$$

where $\bar{x}$ is the mean and $\sigma^2 \equiv x^2(t) - \bar{x}^2$ is the variance of the process x(t).

The mean value at t = t1 is

$$\overline{x(t_1)} = \lim_{N\to\infty} \frac{1}{N} \sum_{i=1}^{N} x^{(i)}(t_1) = \int_{-\infty}^{\infty} x_1 p_1(x_1, t_1) dx_1 \quad , \tag{2.2}$$

where p1(x1,t1) is the possibility density function.

The mean-square value at t = t1 is

$$\overline{x^2(t_1)} = \lim_{N\to\infty} \frac{1}{N} \sum_{i=1}^{N} \left[x^{(i)}(t_1)\right]^2 = \int_{-\infty}^{\infty} x_1^2 p_1(x_1, t_1) dx_1 \quad . \tag{2.3}$$

The overbar in these or the following expressions denotes an ensemble average, the symbol E{} is the expected value, and N is the number of functions in the process ensemble.

2.2.1. Noise Bandwidth

The evaluation of the noise response of a circuit is often difficult except in the case of a simple transfer function. If the frequency response curve is transformed to a normalized transfer function with a step response function (see Fig. 2-1), the analysis becomes much simpler. The normalized frequency fN of a circuit can be expressed as

$$f_N = \frac{1}{A_{v0}^2} \int_0^\infty |A_v(jf)|^2 df \quad , \tag{2.4}$$

where Av0 is the DC gain of the circuit, Av(f) is the gain as a function of frequency, and fN is the normalized noise bandwidth of a circuit.

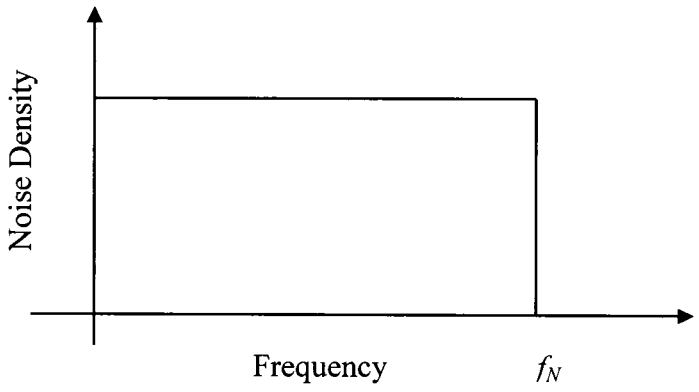


Figure 2-1: Bandwidth of an abrupt response function

2.2.2. Noise Factor and Noise Figure

The noise factor (F) and noise figure (NF) are commonly used figures of merit for specifying the noise performance of a circuit. The noise factor is the ratio of the total output noise power to the noise power attributable to the source resistance.

$$F = \frac{(S/N)_{IN}}{(S/N)_{OUT}} \quad , \tag{2.5}$$

and

$$NF = 10\log(F) = 10\log\left(\frac{(S/N)_{IN}}{(S/N)_{OUT}}\right) \quad , \tag{2.6}$$

where S is the signal and N is the noise in units of power or voltage square.

2.3. Major Types of Random Noise in CMOS ICs

Many random noise sources exist in CMOS ICs. These noise sources have different characteristics and affect circuits differently. In the following subsections, the major types of random noise in CMOS ICs are reviewed.

2.3.1. Shot (Schottky) Noise

Random generation and the flow of mobile charge carries in a material produce a current. This current is identified with "shot noise." Shot noise is a white noise that exhibits a uniform spectral density over all frequencies. In semiconductors,

shot noise is related to charge crossing a potential barrier. It is the dominant noise mechanism in transistors and operational amplifiers at medium and high frequencies [19]. Assume electrons flow from A to B in a material with a permittivity of ε. The current pulse due to a single electron as observed from an external circuit is

$$i_e(t) = \frac{qv(t)}{d} \quad , \tag{2.7}$$

where v(t) is the instantaneous velocity and d is the separation between A and B. The Fourier transform of a single current pulse is [18]

$$F(\omega) = \frac{q}{2\pi d}\int_0^{t_a} v(t)e^{-j\omega t}dt \quad , \tag{2.8}$$

where ta is the arrival time of an electron emitted at t = 0. If the transit time of an electron is sufficiently small such that ωt a << 1,

$$F(\omega) = \frac{q}{2\pi d}\int_0^{t_a} v(t)e^{-j\omega t}dt = \frac{q}{2\pi} \quad , \tag{2.9}$$

and the power density spectral is

$$S(\omega) = 4\pi\bar{N}\left|F(\omega)\right|^2 \quad , \tag{2.10a}$$

$$\bar{I} = q\bar{N} \quad . \tag{2.10b}$$

The associated current is

$$\overline{i_N^2(f)} = S(\omega)\Delta\omega = 2q\bar{I}\Delta f \quad , \tag{2.11}$$

where I is the DC current, and Δf is the noise bandwidth.

The noise described by (2.7) - (2.11) is referred to as shot noise. Because the power density spectrum is constant, shot noise is characterized as a white noise.

2.3.2. Thermal (Johnson) Noise

Thermal noise (or Johnson noise or Nyquist noise) describes fluctuations in the voltage across a dissipative circuit element (such as a resistor or transistor). These fluctuations are most often caused by thermal motion of the charge carriers. The charge neutrality of an electrical resistance is satisfied when the entire volume is considered, but locally the random thermal motion of the carriers sets up fluctuating charge gradients or a fluctuating ***ac*** voltage. A resistor R can be modeled as an ideal resistor in series with a noise voltage source vn [18],

$$v_n^2 = \frac{4hf \cdot R(f) \cdot \Delta f}{e^{\hbar\omega/kT} - 1} \approx 4kT \cdot R(f) \cdot \Delta f \quad , \tag{2.12}$$

or in parallel with a noise current generator of mean square value,

$$i_n^2 = \frac{4hf\Delta f}{R(f)\cdot(e^{\hbar\omega/kT}-1)} \approx \frac{4kT\Delta f}{R(f)} \quad , \tag{2.13}$$

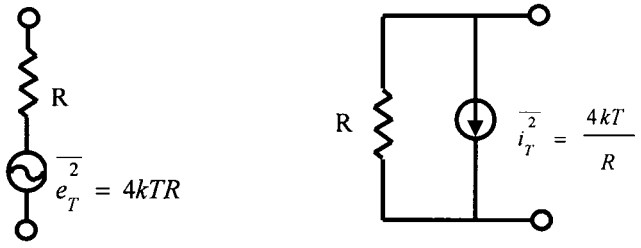
where k is the Boltzmann constant, T is the absolute temperature, R is the MOS transistor channel resistance, and Δf is the frequency range of interest (the MOS transistor cut-off frequency fT or the amplifier bandwidth).

The power spectral density of the thermal noise of a MOS transistor channel resistance is

$$R(f) = \frac{md}{Ne^2\tau_0 A} \quad , \tag{2.14}$$

$$S(f) = \frac{4NVe^2\tau_0 kT}{md^2(1+\omega_0^2\tau_0)} \approx \frac{4kT}{R(f)} \quad , \tag{2.15}$$

where A is the area of the channel cross-section of a MOS transistor, V is the volume of the channel, and $\tau 0$ is the mean scattering time of the channel electrons.



(a) (b)

Figure 2-2: Models of resistor thermal noise in the form of (a) a voltage source, (b) a current source

Thermal noise is also a white noise where the power is distributed uniformly over the entire frequency range. The thermal noise of a submicrometer MOS transistor does not satisfy the long-channel approximation $\overline{i_n^2} = 4kT \cdot [2/(3g_m)]$ [20]. More accurate models of the channel noise are described in [21] and [22]. The thermal noise generated in the substrate or body also affects the MOSFET threshold voltage. Due to the distributed nature of the body resistance, this effect exists in differential circuits as well.

2.3.3. *KTC* Noise

KTC noise is called "KT over C noise". It originates from the thermal noise. As shown by (2-12), the thermal noise of a resistor will become infinite when the resistance R becomes infinite. The thermal noise voltage, however, can not become infinite because there is always a capacitor shunting the resistor, thereby limiting the voltage [18]. In Fig. 2-3, the output noise voltage is determined by the bandwidth of the circuit. The high-frequency cut-off is determined by the RC time constant. The output noise voltage von is

$$v_{no}(f) = \frac{v_{in}}{\sqrt{1 + \omega^2 C^2 R^2}} \quad . \tag{2.16}$$

The power in the output noise signal is

$$P_{no} = \int_0^\infty v_{no}^2(f)df = \int_0^\infty \frac{4kTR\Delta f}{1+\omega^2 C^2 R^2} = \frac{kT}{C} \quad . \tag{2.17}$$

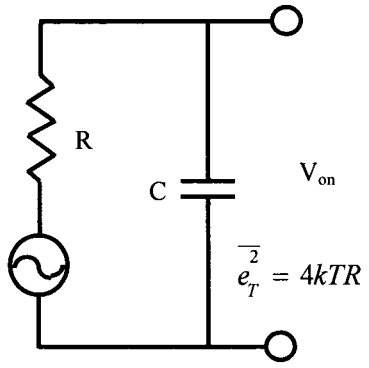


Figure 2-3: Capacitive shunting of a noisy resistor

KTC noise is one of the dominant noise sources in switched capacitor circuits.

2.3.4. *1/f* (Flicker) Noise

Flicker noise is associated with the combination-recombination of carriers in a transistor caused by contamination and defects in the silicon lattice structure. This noise type is also called 1/f noise because the noise amplitude increases as the frequency decreases.

$$\overline{v_n^2} = \frac{K_F}{C_{ox} \cdot f}. \tag{2.18}$$

To determine the noise, the technology constant KF is measured for both PMOS and NMOS devices. The dependence on f and Cox is of the form (Cox)a*fb [19].

These parameters may vary from one process to another process. Direct measurement of device noise is difficult because the noise is too small to be directly sensed by typical instrumentation. Amplification of the noise signal at the device output is usually required, but the noise contributed by the gain stage must be sufficiently lower than that of the device under test.

Low frequency noise in silicon MOSFET's is dominated by flicker noise. Experimental results in [23] suggest that 1/f noise in an N-channel MOS transistor is dominated by carrier density fluctuation while 1/f noise in a P-channel transistor is primarily due to mobility fluctuation. Much effort has been spent in understanding and reducing 1/f noise in MOSFET's [24]-[32].

2.3.5. Corner Frequency

Thermal and shot noises are flatband noise. At the frequency where the 1/f noise is "buried" in the flatband noise, 1/f noise is indistinguishable from thermal and shot noise. The frequency fC, as shown in Fig. 2-4, is called the corner frequency of the 1/f noise.

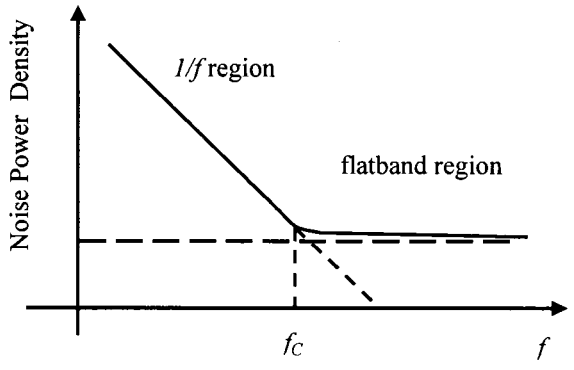


Figure 2-4: Flicker Noise Spectrum and Corner Frequency

2.4. Noise Sources in Mixed-Signal ICs from Parasitic Components

Mixed-signal CMOS ICs typically have analog circuits that operate in a noisy digital environment. The noise sources are typically much larger than the random noise described in section 2.3. With increased speeds and scaling of semiconductor technologies, noise from parasitic coupling has become a serious problem affecting the performance of mixed-signal ICs. Parasitic coupling noise between the on-chip analog and digital circuits can corrupt low level analog signals. Near field coupling (usually only the electrical field is considered and is called capacitive coupling) between neighboring circuits and coupling between widely separated circuits through the substrate and power rails are significant problems that currently affect the performance of mixed-signal integrated circuits. For certain applications with sensitive analog circuits, the analog and digital circuits are built on separated substrates to remove any substrate coupling. In this section, certain important noise sources in mixed-signal ICs are discussed.

2.4.1. Substrate Coupling Noise

CMOS static logic is widely used in mixed-signal integrated circuits because of the wide range of available circuit libraries, high packing densities, and large noise margin. It is well known that static logic circuits dissipate high power at high frequencies is due to the large current pulses drawn from the power supply to ground (or substrate) during state transitions [33].

The current spikes generated by CMOS logic gates flow through parasitic resistances, capacitances, and inductances, potentially causing several hundred millivolts or more of "digital switching noise" (also known as ground and Vdd bounce) [34]-[36].

When current is injected into the substrate, a local fluctuation in the substrate voltage will occur. This voltage fluctuation is due to the substrate noise. In mixed-signal integrated circuits, the injected current can be caused by

- power busses coupling noise into the substrate through ohmic contacts
- capacitively coupling noise through the reverse biased bulk/well junctions, and/or
- transistors capacitively coupling noise through the source/drain diffusions.

In order to develop high performance analog circuits on a mixed-signal substrate, it is important to reduce the coupling of digital noise to the analog circuits. Separately connecting power and ground to the analog and digital circuits can reduce the digital switching noise (or the power/ground bounce) in the analog circuits [33]. Digital switching noise, however, can couple through the substrate and is difficult to reduce.

It is important to understand the noise coupling process and transmission mechanisms in evaluating noise in mixed-signal SoCs (systems-on-a-chip).

Substrate coupling noise and techniques for testing substrate coupling noise are presented in Chapter 4.

2.4.2. Capacitive Coupling Noise

Noise can be coupled through the silicon substrate and on the surface level of the IC, the later called capacitive and inductive coupling. With two or more neighboring lines are near, an electric field can be established, creating interference between the wires. The signals on these wires interact through an electric field flux, which can be represented by a coupling capacitance. The capacitive coupling strongly depends upon the physical distance between the two lines. The coupling noise between the on-chip analog and digital circuits can corrupt sensitive analog signals, generating a significant error in the analog signal voltage. A simple closed form expression for coupling in arbitrary networks has been an open problem for more than three decades, since the late 1960's [37]. Many models have been developed for capacitive coupling (some commonly accepted models are described in Appendix B). Other relevant research in this area includes the work described in [38], [39] which a system of partial differential equations is solved for a pair of lines in order to arrive at a coupling expression [40], [41]. Techniques for accurately measuring the capacitive coupling noise voltage are proposed and discussed in Chapter 5.

2.4.3. Clock Feedthrough

Clock feedthrough is a fundamental problem in analog ICs. The most commonly accepted clock feedthrough mechanism (in the charge domain) occurs when the switch is turned off, dispersing the charge in the inversion channel, thereby forcing current to flow either into the substrate or the load capacitor at the MOSFET drain or source. This mechanism produces an error voltage on the load capacitor.

In this thesis proposal, the clock feedthrough error is considered to be primarily due to capacitive coupling to the S/H capacitor CL from the overlap capacitor Cgd and the gate capacitor Cox. The MOSFET drain current ID supplies charge to compensate for the error voltage generated from the coupling until the MOSFETs are completely cut-off (see Fig. 2-5). The clock feedthrough error voltage on the S/H capacitor CL, ΔVerror, is determined by the difference between the coupled charge and the charge injected by the transistor current,

$$\Delta V_{error} = \frac{\Delta Q}{C_L} = \frac{1}{C_L} \cdot \left(\Delta Q_{coupling} - \int_0^t I_D(t)dt \right), \tag{2.20}$$

where ΔQcoupling is the charge coupled through capacitors Cox and Cdg when the transmission gate switch is turned off.

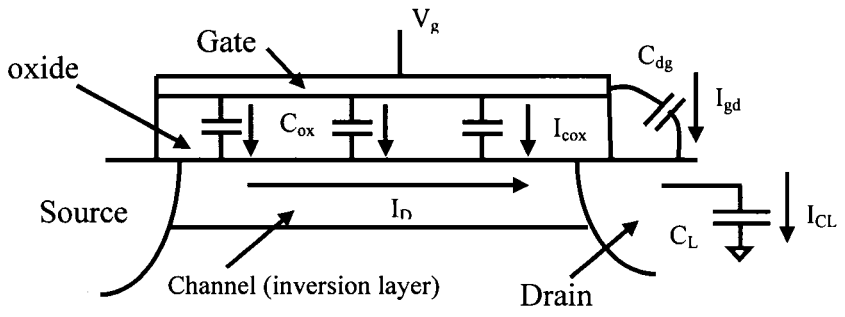


Figure 2-5: Current flow in a MOSFET

2.4.4. Charge Sharing Effect

The charge sharing effect is a phenomenon of charge re-distribution (or charge loss to parasitic capacitors) when a capacitor network with parasitic capacitors is reconfigured. The capacitor network does not have any source to pump in/out charge such that the total amount of charge in the network is conserved. Charge sharing effect noise is a significant issue in many switched capacitor CMOS circuits. Parasitic capacitance, such as the amplifier input capacitance and S/H node wire capacitance of a sample/hold (S/H) circuit, can cause large charge sharing effect noise errors in many applications (such as S/H circuit, digital filters, A/D, and D/A converters).

2.4.5. Power Supply/Ground Noise

In high speed, high density CMOS mixed-signal ICs, many digital output drivers can switch simultaneously. When these outputs switch simultaneously, a significant amount of power/ground noise can be generated in the on-chip

power/ground busses. The characteristics of power/ground noise (i.e., the amplitude, width, and damping behavior) not only depend on the drive strength of these output drivers, but also depend on the parasitic impedances of the package [42].

Consider n CMOS output drivers switching simultaneously with several different drive strengths and switching speeds. Assume each output is switching symmetrically around the time T0. Based on an equivalent lumped (R, L, C) model for the parasitic impedance of the package from an on-chip ground bus to the end of the package ground pin, the ground noise as described in [43] is

$$V_n = V_k + \frac{1}{L^1}\frac{p}{\sum_{i=1}^{n}(K_i/T_i)}\left\{1-\left[1+2V_k\frac{\sum_{i=1}^{n}(K_i/T_i)}{p}L^1\right]^{1/2}\right\} \quad , \qquad (2.21)$$

where Vn is the ground noise produced by n simultaneously switching output drivers, Ki = μnCox(W/L) for the ith N-channel output driver device, p is the number of Vss bond pad-package pin connections, Ti is the time required for the ith switching current spike to transition from zero to the maximum voltage, L1 is the effective inductance of each Vss pad-pin connection, and Vk = Vin – Vt.

2.5. Conclusions

The various noise sources in integrated circuits are reviewed in this chapter, providing background for the specific research results based on these noise sources that are described in the following chapters. Random noise exists in ICs operating at low frequencies such as 1/f noise, to the medium frequency range such as KTC noise, to white noise such as shot noise and thermal noise. Other types of noise, such as substrate coupling noise, capacitive coupling noise, charge sharing effect noise, clock feedthrough noise, and power/ground noise have also been reviewed. Each of these sources of noise has an accumulative effect on the signal error. An integrated approach to interpreting, managing, and evaluating these noise sources is therefore an important research objective.

Chapter Three: Non-Ideal Factors in Mixed-Signal CMOS ICs

Many non-ideal factors exist in semiconductor processes and are difficult to remove. These non-ideal factors affect the performance of an IC, reduce product yield, and may make a circuit not function correctly. Some non-ideal factors that affect mixed-signal CMOS ICs are presented in the following sections of this chapter. Component mismatch in CMOS ICs is reviewed in section 3.1. The matching properties of a MOS transistor are described in section 3.2. Capacitor mismatch is discussed in section 3.3.

3.1. Component Mismatch in CMOS ICs

The matching properties of passive and active devices have been extensively studied [44]–[47]. Mismatches due to process variations exist in components (MOSFETs, capacitors, and resistors), and circuits (such as amplifiers, comparators, and gain blocks). Characterizing component matching is quite difficult. For example, for small capacitors in the range of 0.1 pF to 1 pF, common in most analog circuits, direct measurement suffers from many uncertainties resulting from parasitic impedances within the physical set-up. An efficient

approach for measuring capacitor mismatch is described in [48]. In this chapter, mismatches in MOSFETs and capacitors are reviewed.

3.2. Matching Properties of a MOS Transistor

Mismatches in threshold voltage, transconductance parameter μ*Cox*W/L where μ is the channel carrier mobility, Cox is the unit gate capacitance, and L and W are the transistor channel length and width, respectively, and the body-effect coefficient γ of a MOS transistor are a result of several random processes which occur during each device fabrication step. These mismatches include batch-to-batch variations, wafer-to-wafer variations, and unwanted offsets.

In general, the value of a parameter P is composed of a fixed part and a randomly varying part, resulting in differing values of P at different coordinate pairs (x, y) on a wafer. The actual mismatch in parameter P between two identical areas (A) at coordinates (x1, y1) and (x2, y2) is [49]

$$\Delta P(x_{12}, y_{12}) = \frac{1}{A}\left[\iint_{A(x1,y1)} P(x,y)dxdy - \iint_{A(x2,y2)} P(x,y)dxdy \right] \quad . \tag{3.1}$$

By means of a two-dimensional Fourier transformation, the geometry-dependent part is separated from the mismatch source,

$$\Delta \mathcal{P}(\omega_x, \omega_y) = \mathcal{G}(\omega_x, \omega_y)\mathcal{P}(\omega_x, \omega_y) \quad . \tag{3.2}$$

The geometry function G(ωx, ωy) for a pair of rectangular devices with area W*L is determined from a straight forward Fourier analysis,

$$\mathcal{G}(\omega_x,\omega_y)=\frac{\sin(\omega_x L/2)}{\omega_x L/2}\frac{\sin(\omega_y W/2)}{\omega_y W/2}\{2\sin(\omega_x D_x/2)\} \quad . \tag{3.3}$$

For convenience, both areas are assumed to have spacing Dx along the x-axis. The variance of the stochastic parameter can be represented as a power content in the Fourier domain.

$$\sigma^2(\Delta P)=\frac{1}{4\pi^2}\int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty}\left|\mathcal{G}(\omega_x,\omega_y)\right|^2\cdot\left|\mathcal{P}(\omega_x,\omega_y)\right|^2 d\omega_x d\omega_y \quad . \tag{3.4}$$

The variance of parameter ΔP between two rectangular devices is found by substituting (3.3) into (3.4),

$$\sigma^2(\Delta P)=\frac{A_P^2}{WL}+S_P^2 D_x^2 \quad . \tag{3.5}$$

A2P is the area proportionality constant for parameter P, while SP describes the variation of parameter P with spacing. These proportionality constants can be measured and used to predict the mismatch variance of a circuit. In the following

sections, variations of the threshold voltage, transconductance parameter, and body-effect coefficient γ of a MOS transistor are discussed.

3.2.1. Variations in MOS Transistor Parameters

MOS transistors are basic components in an integrated circuit. The key parameters of a MOSFET directly affect circuit performance, particularly in analog integrated circuits where not only the absolute values of these parameters are important but also the relative values (the matching characteristics). Almost all MOSFETs in analog ICs operate in the saturation region. The I-V relationship of a MOS transistor operating in saturation is (for example, an NMOS transistor),

$$I_D = \frac{C_{OX}\mu_n}{2}\left(\frac{W}{L}\right)\cdot\left(V_{gs}-V_{TN}\right)^2\left(1+\lambda\cdot V_{DS}\right)= k\cdot\left(V_{gs}-V_{TN}\right)^2\left(1+\lambda\cdot V_{DS}\right). \qquad (3.6)$$

λ is the channel modulation coefficient. The most important MOS transistor parameters are reviewed below.

3.2.1.1. MOS Transistor Gate Capacitance

A MOS transistor is a voltage-controlled current device. The gate capacitance directly affects the transconductance of a MOS transistor. The MOS transistor gate capacitance is defined as $C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$, where tox is the gate dielectric layer thickness and εox is the permittivity of silicon dioxide. The mismatch in Cox is due

to the variations in the dielectric layer thickness tox. The variation of εox is usually small as compared to that of tox [50]. As shown in [51],

$$\sigma^2_{Cox} = \frac{C^2_{OX} A_{Cox}}{LW} \quad . \tag{3.7}$$

3.2.1.2. Threshold Voltage

Once a voltage is applied to the gate of a MOS transistor, an inversion layer is generated underneath the gate oxide if the voltage between the gate and body is greater than a certain voltage. This voltage is called the threshold voltage and is

$$|V_T| = |V_{T0}| + \gamma\left(\sqrt{2|\phi_p| + |v_{SB}|} - \sqrt{2|\phi_p|}\right) \quad , \tag{3.8a}$$

$$|V_{T0}| = \phi_{GB} - 2\phi_F - \frac{\sqrt{2qN\varepsilon_{si} - 2|\phi_p|} + Q_{ss}}{C_{OX}} \quad , \tag{3.8b}$$

where ϕGB and ϕf are the Fermi potential difference and substrate material Fermi potential, respectively. Qss is the silicon gate interface charge density. VTO can be treated as a constant in most cases. γ is a device constant, called the body-effect coefficient, and is

$$\gamma = \frac{\sqrt{2\varepsilon_{si} qN}}{C_{ox}} \quad . \tag{3.9}$$

Mismatches in γ can be caused by variations in the carrier density N and the gate capacitance COX. The MOS transistor threshold voltage VT changes with the process parameter variations due to the variation in the doping process and variations in the thickness of the gate dielectric layer. Variations in VT affect many basic analog components, such as clock feedthrough error in switches, operational amplifier and comparator offset voltages, errors in current mirrors, all of which degrade the performance of analog circuits. The dependence of the threshold voltage on the process and voltage VSB is characterized by (3.8). From (3.5), the standard deviations of VT and γ are [53]

$$\sigma^2(V_T) = \frac{A_{VT}^2}{WL} + S_{VT}^2 D^2 \quad , \tag{3.10a}$$

$$\sigma^2(\gamma) = \frac{A_\gamma^2}{WL} + S_\gamma^2 D^2 \quad . \tag{3.10b}$$

3.2.1.3. Carrier Mobility

In most cases, the carrier mobility μ is a constant. However, for short channel lengths, the electric field in an MOS transistor channel is sufficiently high such that the carrier drift velocity saturates. The effective mobility of the carriers increases

once drift saturation occurs. As reported in [52], at room temperature and moderate gate bias, the electron mobility is primarily governed by scattering due to interface charge centers and phonons. An empirical relationship for μ is [18]

$$\mu = \frac{\mu_o(N_A)}{1+\alpha(N_A)N_f} \quad , \tag{3.11}$$

where μ o(NA) and α(NA) are empirical constants that exhibit a minimal dependence on the dopant concentration. Nf is the interface charge density. The mismatch in μ can be approximated to be entirely due to the non-uniformity of Qf. As the fixed oxide charges exhibit a Poisson distribution, the deviation of the mobility μ can be represented as [53]

$$\sigma_\mu^2 = \frac{\mu_o^2\alpha^2}{\left(1+\alpha\overline{Q_f}\right)^4}\cdot\frac{\overline{N_f}}{LW} = \frac{\mu^2 A_\mu}{LW} \quad . \tag{3.12}$$

In analog ICs, short channel transistors are less often used due to these short-channel effects. The mismatch in the carrier mobility is usually small as compared to mismatches in other parameters.

3.2.1.4. Variations in Transistor Transconductance Parameter

In order to have a large transconductance, most MOS transistors in analog ICs operate in the saturation region. The following long channel I-V relation to characterize this behavior is

$$I_D = \frac{C_{OX}\mu_n}{2}\left(\frac{W}{L}\right)\cdot\left(V_{gs} - V_{TN}\right)^2 = k\left(V_{gs} - V_{TN}\right)^2, \tag{3.13}$$

where k is the MOS transconductance parameter. By examining the mutually independent components W, L, μ, and Cox, the matching properties of the transconductance parameter k can be determined from [53]

$$\frac{\sigma^2(k)}{k} = \frac{\sigma^2(W)}{W^2} + \frac{\sigma^2(L)}{L^2} + \frac{\sigma^2(C_{OX})}{C_{XO}^2} + \frac{\sigma^2(\mu_n^2)}{\mu_n^2} \quad . \tag{3.14}$$

The first and second terms characterize variations in W and L that originate from edge roughness, and the third and fourth terms characterize variations in the gate oxide and carrier mobility. The edge roughness can be treated as a one-dimensional variance with $\sigma^2(L) \propto 1/W$ and $\sigma^2(W) \propto 1/L$. Equation (3.14) can be simplified to

$$\frac{\sigma^2(k)}{k^2} = \frac{A_W^2}{W^2 L} + \frac{A_L^2}{L^2 W} + \frac{A_{Cox}^2}{WL} + \frac{A_\mu^2}{WL} + S_k^2 D^2 \approx \frac{A_k^2}{WL} + S_k^2 D^2 \quad , \tag{3.15}$$

where AW, AL, ACox, A_μ, Sk, are process-related constants. The relative mismatch in the transconductance parameter can be approximated by the inversion area variation Sk as seen in the last term of (3.15) if W and L are sufficiently large.

3.2.1.5. Drain Current Mismatch

Current match is required in many basic analog integrated circuits, such as current mirrors, amplifier differential-pair stage, biasing circuits, reference voltage generators, and almost all current-mode circuits. In this section, mismatch in MOS transistor current is reviewed and discussed.

MOS transistor drain current mismatch originates primarily from two sources: threshold voltage VT mismatch and transconductance parameter k mismatch. The relationship between the drain current mismatch and mismatches in VT and k has been established in [53] for transistors operating in the linear region.

$$\frac{\sigma^2(\Delta I)}{I^2} = \frac{\sigma^2(\Delta k)}{k^2} + 4\frac{\sigma^2(\Delta V_T)}{(V_{GS} - V_T)^2} \quad . \tag{3.16}$$

Variations in mismatch between equal area MOS transistors, which have been observed in VT and k, are transferred to drain current ID mismatch through the relationships shown in (3-6). Although (3.16) is intended for a transistor operating in the linear region, the measured data described in [53] show that the measured mismatch for a transistor operating in the saturation region is well predicted using (3.16). Equation (3.16) shows that at low values of VGS, the dominant factor causing mismatch in the drain current is the variation in the threshold voltage. Variations in the current fact k affect drain current matching at high values of VGS.

The measurement described in [54] indicates that for equal area transistors, shorter channel lengths and wider channel widths have poorer matching than longer lengths and narrower channel widths. Similar to mismatches in threshold voltage Vt and transconductance parameter k, small W/L transistors have higher drain current matching than equal area transistors with a larger W/L ratio.

3.3. Capacitor Mismatch

Unlike in digital integrated circuits, the performance of analog MOS integrated circuits, such as analog-to-digital converters [53]-[55], digital-to-analog converters [56], [57], switched-capacitor amplifiers, sample/hold circuits [58], and filters, depends heavily on the accuracy of component matching. The matching accuracy is mostly for passive components such as capacitors and resistors. With the scaling of the power supply voltage, current-mode operation has become more attractive. The

matching accuracy of active components, the transistors, is also of great importance.

MOS integrated circuits are inherently subject to mismatch errors from two sources. One is systematic error, which affects adjacent elements with identical geometries. This error can be reduced by proper matching techniques. The other source of mismatch error is random error, which differs from element to element, and therefore cannot be corrected by improved matching techniques. Random mismatch error represents a significant limitation to the achievable accuracy of a circuit. Shyu and Temes proposed statistical models to analyze random error effects in [59], [50].

3.3.1. Variations in Capacitance

Capacitors and resistors are common passive components in analog circuits. In analog integrator circuits, however, ratios of these components rather than absolute values of these components are typically used due to the inaccuracy of the capacitance and resistance. In current CMOS technologies, typical variations of the capacitance and resistance are about ±15%, and ratios of the capacitance and resistance are in the range of 0.1% to 1%.

The inaccuracy of the capacitance and resistance is caused by variations in the dimensions, dielectric layer thickness, permittivity constant, and resistance per square. Such inaccuracies can be improved but not completely eliminated.

3.3.1.1. MOS Capacitor

The MOS capacitor is built from a MOSFET gate capacitor by generating an inversion layer under the gate. The capacitance Cox of a MOS capacitor is

$$C_{ox} = WL\frac{\varepsilon_{ox}}{t_{ox}} \quad . \tag{3.17}$$

The error of the capacitance in (3.17) is due to variations in W, L and tox, where the variation in εox is assumed to be negligible. Once the MOS capacitor is patterned on a silicon wafer, jagged edges are generated from both masks and the lithography process. These jagged edges cause an error in the value of the capacitor. Usually, W and L are much larger than the variations of the dimensions. The variation of the gate dielectric thickness also contributes to the capacitance error and may dominate the variation of the MOS capacitor for certain semiconductor processes. The error of this type of capacitor can be represented by the following equation [49],

$$\Delta C_o = WL\frac{\varepsilon_{ox}}{t_{ox}} - (W+\Delta W)(L+\Delta L)\frac{\varepsilon_{ox}}{t_{ox}+\Delta t_{ox}} \approx C_o\frac{\Delta t_{ox}}{t_{ox}+\Delta t_{ox}} - \frac{W\Delta L + L\Delta W}{t_{ox}+\Delta t_{ox}} \quad . \tag{3.18}$$

The relative error is

$$\frac{\Delta C_o}{C_o} = \frac{\Delta t_{ox}}{t_{ox} + \Delta t_{ox}} - \frac{t_{ox}\left(\Delta L/L + \Delta W/W\right)}{t_{ox} + \Delta t_{ox}} \quad . \tag{3.19}$$

With technology scaling, tox has become quite small (80 ′ for a 0.15 μm CMOS technology). The gate dielectric thickness tox is small as compared to W and L. ⊿L and ⊿W are much smaller than L and W. The second term in (3.19) dominates the MOS capacitance error. Assuming ⊿L and ⊿W are independent random variables with equal standard deviation $\sigma_L = \sigma_W$, the standard deviation of ⊿Cox is

$$\sigma_C = C_{ox}\sigma_W \sqrt{\frac{1}{W^2} + \frac{1}{L^2}} \quad . \tag{3.20}$$

The relative error σ_C / C_{ox} is minimized if W is chosen equal to L. Thus, for a minimum possible relative capacitance error due to edge variations, the shape of the capacitors should be square. Equation (3.20) is valid for absolute rather than relative values of Cox. A highly accurate capacitance is difficult to obtain. The ratio of two capacitors, however, can be accurate if the capacitors are placed physically close to each other (using special layout techniques). Assume two capacitors C1 and C2 have the size, W1 L1 and W2 L2, respectively. The ratio of

two capacitors C_1/C_2 is α. If all of the dimensions of C1 and C2 have the same standard error σ, the relative error of ratio α is [18]

$$\frac{\sigma_\alpha}{\alpha} = \sigma\sqrt{\frac{1}{W_1^2} + \frac{1}{L_1^2} + \frac{1}{W_2^2} + \frac{1}{L_2^2}} \quad . \tag{3.21}$$

The error of the relative ratio σ_α/α is minimum when $L_1 = W_1 = \sqrt{\alpha}\cdot L_2 = \sqrt{\alpha}\cdot W_2$. The minimum value is

$$\left.\frac{\sigma_\alpha}{\alpha}\right|_{\min.} = \frac{\sqrt{2}\sigma}{L_1}\cdot(1+\alpha)^{1/2} \quad . \tag{3.22}$$

The ratio α must be greater than one to satisfy (3.22).

3.3.1.2. Two Plate Capacitor

In modern CMOS processes, two or more polysilicon layers are often available in analog technologies. The double-polysilicon capacitor is one of the most widely adapted capacitor structures in analog ICs. The structure utilizes two layers of heavily doped polysilicon as the plates. The basic structure of this type of capacitor in an MOS process is shown in Fig. 3.1.

This type of capacitor is built on a thick field oxide such that the parasitic capacitance to the underlying silicon is relatively small. The double-polysilicon

capacitor is highly linear as compared to other types of MOS capacitors. The capacitance of a double-polysilicon structure is [49]

$$C = S \cdot C_o \cdot \left(1 + \alpha \cdot (V_1 - V_2) + \beta \cdot (V_1 - V_2)^2\right) \quad , \tag{3.23}$$

where α and β are process related parameters, and β is much smaller than α. Co is the ideal unit capacitance (without considering the electric field edge effect) and S is the area of the top plate.

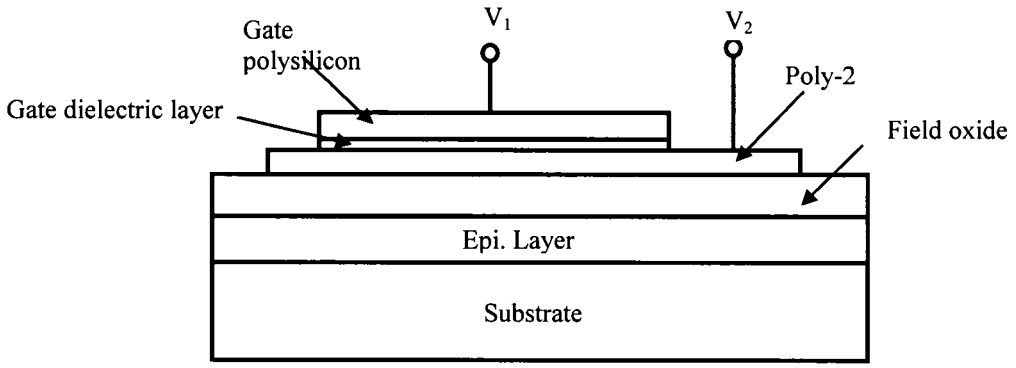


Figure 3-1: Double polysilicon capacitor (an epitaxial layer is a thin silicon film with a specific doping level, thickness, crystal direction, and is grown on a low receptivity single crystal silicon substrate)

In order to obtain higher linearity, the capacitor can be divided into an even number of small, equally sized (usually square) capacitors. These capacitors are connected in parallel with half of the top plates connected to V1 and bottom plates

to V2 and the other half top plates are connected to V2 and bottom plates are connected to V1. From (3.22), the second and third terms cancel.

The dielectric layer between two polysilicon layers is thicker than the thickness of the gate dielectric. The unit capacitance is therefore smaller than the unit capacitance of a MOS gate capacitor, but with a smaller error. The relative error of a double-polysilicon capacitor is about the same as described in (3.19)-(3.21) but with different dielectric thicknesses.

3.3.2. Random Error in MOS Capacitors

During the IC manufacture process, the position of an edge of a line or device can be affected such that an ideally straight line can appear wavy. The edge variation includes a local jagged edge variation and a global distorted edge variation. Both the local and global edge variations introduce random error. In addition to edge variations, uncertainty in the dielectric thickness can cause random errors in the capacitance.

Random capacitance errors due to the local and global edge and oxide effects have been combined into a relative capacitance error and is expressed in [45] as

$$\frac{\Delta C_o}{C_O} = \sqrt{K_{le}C^{-3/2} + K_{ge}C^{-1} + K_{lo}C^{-1} + K_{go}} \quad , \qquad (3.24)$$

where Kle is the local edge effect factor, Kge is the global edge effect factor, Klo is the local oxide effect factor, and Kgo is the global oxide effect factor [45],

$$K_{le} \approx 8 d_e \sigma_{le}^2 \left(\frac{\varepsilon}{t_{ox}} \right)^{3/2} \quad , \tag{3.25}$$

$$K_{ge} \approx \frac{7\varepsilon}{t_{ox}} \sigma_{ge}^2 \quad , \tag{3.26}$$

$$K_{lo} \approx 8 d_o^2 \frac{\varepsilon}{t_{ox}} \left(\frac{\sigma_{le}^2}{\varepsilon^2} + \frac{\sigma_{lt}^2}{t_{ox}^2} \right) \quad , \tag{3.27}$$

$$K_{go} \approx \frac{\sigma_{ge}^2}{\varepsilon^2} + \frac{\sigma_{gt}^2}{t_{ox}^2} \quad . \tag{3.28}$$

In (3.25) – (3.28), de is the correlation radius and σle is the standard deviation of the local edge variation, σge is the standard deviation of the variation in the global edge, σl_ε and σlt are the standard deviations of ε and tox for local effects, respectively, do is the local oxide correlation radius, and σg_ε and σgt are the standard deviations of ε and tox for global effects, respectively.

In order to avoid process reflected systematic errors, MOS capacitors are often digitized into several small unit capacitors connected in parallel. For such capacitors, the overall relative error is

$$C_o = nC_i \quad , \tag{3.29}$$

$$\frac{\sigma_{nCi}}{C_o} = \sqrt{\frac{n^{1/2}K_{le}}{C_o^{3/2}} + \frac{nK_{ge}}{C_o} + K_{lo}C_o^{-1} + K_{go}} \quad . \tag{3.30}$$

In most applications, the ratio α of two capacitances C1 and C2 is more important than the individual values of these two capacitors. Assuming C1 = n Ci and C2 = m Ci, the relative rms error of α is

$$\frac{\sigma_{\alpha i}}{\alpha} = \sqrt{\left(\frac{\sigma_{nci}}{C_1}\right)^2 + \left(\frac{\sigma_{nci}}{C_2}\right)^2} = \sqrt{\left(\frac{1}{n} + \frac{1}{m}\right)\left(\frac{K_{le}}{C_i^{3/2}} + \frac{K_{lo}}{C_i}\right) + K_{ge}C_i^{-1} + 4K_{go}} \quad . \tag{3.31}$$

Equation (3.31) shows that placing unit capacitors in parallel improves the relative error caused by random error effects.

3.4. Conclusions

Mismatches in IC components, such as the MOS transistor and capacitor, are discussed and reviewed in this chapter. Mismatches in the MOS transistor are primarily due to errors in the gate capacitance, threshold voltage, carrier mobility, and transistor transconductance parameter. Mismatch errors in two types of IC capacitors, the MOS capacitor and the double polysilicon capacitor, are reviewed. The primary sources of capacitor mismatch error are error in the capacitor size and

error in the thickness of the dielectric layer. Mismatch error in the ratio of two capacitors is much smaller than the error of a single capacitor. Capacitors built into square shapes have a smaller capacitance ratio mismatch error.

Chapter Four: Accurate Substrate Noise Testing Technique

The push for reduced cost, more compact circuit boards, and added customer features has provided incentives for including analog functions with primarily digital MOS integrated circuits (IC). Complex high speed digital circuits together with high performance analog circuits are therefore commonly integrated on the same IC substrate. In such mixed-signal systems, fast switching transients produced by the digital circuits can couple into sensitive analog components, thereby limiting analog precision. Performance degradation caused by substrate noise has become difficult to control and even more difficult to predict. The capability of accurately measuring substrate noise to identify and avoid these problems has therefore become increasingly important.

Substrate noise was reported in the 80's [60], followed by significant research in the late 1980's [61], [63], and in the 1990's [63]-[71]. In order to evaluate substrate noise, on-chip test circuits are required to accurately and efficiently measure the substrate current [64]-[70]. These measurements, however, are based on simple single MOS transistor test structures [34], [71], voltage comparator structures [69], [70], or single stage MOS different amplifier structures [72]. A common problem in these measurements is the difficulty of acquiring output

signals without other noise signals mixed in the measured signal. Due to the small peak-to-peak voltage, an accurate substrate noise test is difficult to achieve. Noise from the test board, power supply, and integrated circuit package adds noise to the substrate coupling current sensed by the on-chip test circuitry (see Fig. 4-1). The parasitic components of the pads, bonding wires, package frame, external circuitry, and the cable affect the analog output signal, severely decreasing the accuracy of the measurement. Expensive equipment is also typically required to test these circuits. In order to produce accurate test results and to simplify the measurement process, dedicated data sensing and analog-to-digital conversion circuitry must also be included on-chip.

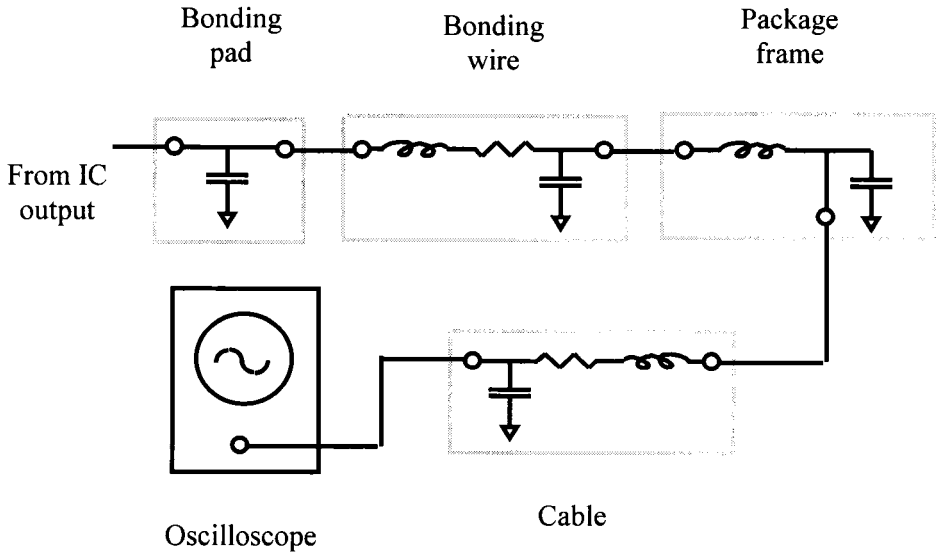


Figure 4-1: Parasitic impedances along an IC test path

In this chapter, an accurate substrate noise testing technique is presented. The proposed substrate coupling noise measuring technique rejects other types of noise such as common-mode noise, power/ground noise, *1/f* noise, and any random noise while only collecting the substrate coupling noise. The circuit output is in the form of a digital code so that the noise from the pads, bonding wires, package frame, and external test circuit does not affect the accuracy of the test result. Simple test equipment is required for reading out the measured data.

This chapter is organized as follow. The substrate noise mechanism is reviewed in Section 4.1. In Section 4.2, the principle used in the on-chip substrate noise test circuitry is described. Design details of the circuit are presented in Section 4.3. The error of the test circuit is considered in Section 4.4. Amplifier and comparator are designed in section 4-5. Analytic and SPICE simulation results are presented and compared in Section 4.6. Finally, some conclusions are provided in Section 4.7.

4.1. Substrate Coupling Noise

When current is injected into the substrate, a local fluctuation in the substrate voltage will occur. This voltage fluctuation is the substrate noise. In mixed-signal integrated circuits, the injected current can be caused by

- power busses coupling noise into the substrate through ohmic contacts [36], [73],

- the wells capacitively coupling noise through the reverse biased bulk/well junctions,
- and/or the transistors capacitively coupling noise through the source/drain diffusions.

When the drain of an MOS transistor switches, the switching voltage is coupled through the drain junction capacitor into the substrate (see Fig. 4-2). Due to the change in the substrate voltage, a substrate pulse current flows into the substrate. The induced switching current flow causes the substrate potential to change. Due to the body effect and the junction capacitance of a sensitive transistor, changes in the backgate voltage induce noise spikes in the drain current and, consequently, the drain voltage. The substrate noise coupling produces different effects for different types of substrates. For low resistance, heavily doped, and thick substrates, the injected noise current flows directly through the epitaxial layer into the bulk and up through the epi. layer to the substrate contact on the surface [36]. The injected current flows first vertically in the high resistive epitaxial layer, enters the low impedance substrate flowing horizontally, and then re-enters the epitaxial layer flows into the collecting node (or the receiver called in [36]). The voltage induced by the current flow within the substrate is small, decreasing the substrate coupling. Fig. 4-2 is a cross section of a NMOS and PMOS transistors fabricated on a p substrate. These substrate coupling noise sources are shown in Fig. 4-2 below.

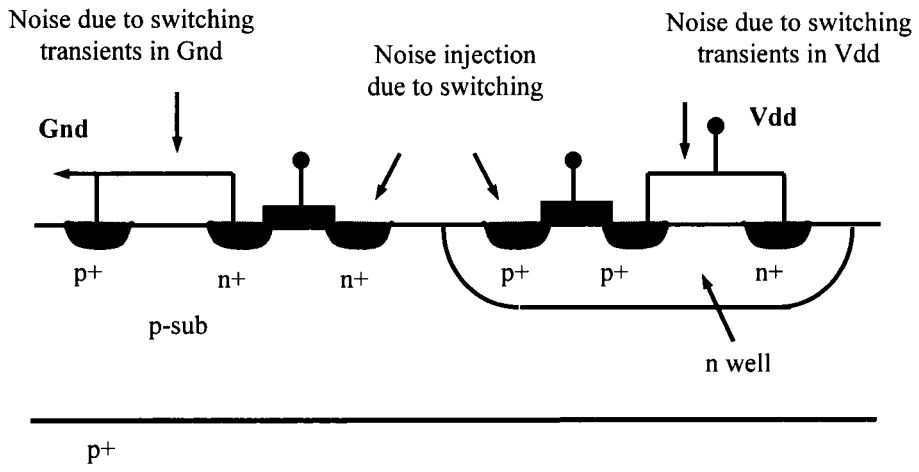


Figure 4-2: Sources of noise coupling within the substrate

Masui reported in [34] that the noise voltage decreases with increasing spacing in lightly doped substrates; however, in heavily doped substrates, the substrate coupling noise depends little on the spacing. The experimental results described in [70] also show that the peak-to-peak noise amplitude is independent of the distance between the current source and the noise source; increasing the separation from 40 μm to 850 μm does not reduce the measured noise. Additionally, physical separation has no observable effect on the noise settling time. A P+ guard ring placed close to the current source (noise victim) provides a substrate noise reduction of about 20% (from10 mV to 8 mV), while a similar but more distant ring has less of an effect (measured substrate noise changes from 10 mV without ring to 0.9 mV). Guard rings connected to large substrate contacts result in an increase in the observed noise.

The current flow in the substrate also affects the MOS transistors by changing the effective threshold voltage. Substrate noise reduction techniques include separate analog and digital power/ground lines, physical separation between the analog and digital circuits, guard rings, a low inductance bias path for the substrate, and the application of additional substrate contacts as reported in [36].

4.2. Principle of the Substrate Noise Testing Technique

The proposed substrate noise test technique operates in a differential architecture and consists of a substrate coupling noise sensing circuit, an integrator, a comparator, a counter, and a digital timing circuit (see Fig. 4-3). The differential operation reduces or removes the common-mode noise from the power distribution network, thereby producing a more accurate capacitive coupling voltage. The substrate noise sensing part of the test circuit is shown in Fig. 4-4.

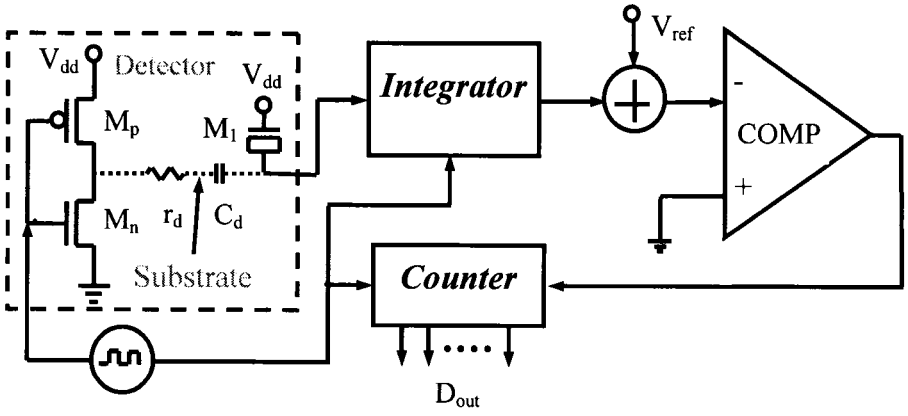


Figure 4-3: Substrate coupling noise test circuit

4.2.1. Generating and Detecting Substrate Noise

The substrate noise is generated by an inverter that has a large drain area for effective current injection. A digital clock signal is applied onto the input of the inverter. The voltage change at the inverter output generates a substrate current injected through the drain PN junction capacitor. Sensing of this substrate noise due to the current injection from the inverter drain PN junction capacitor is achieved by a MOS (transistor M_1) capacitor C_d (see Fig. 4-4). The gate of M_1 is connected to the power supply V_{dd}; the source and drain are tied together. The depletion capacitor C_d of the PN junction between the S/D and the substrate is formed as shown in Fig. 4-4.

The substrate noise generator and the sensor are separated by a space S. The injected current flows from the drain PN junction through the epi-layer to a low resistive substrate, then flows back to the epi-layer and finally reaches the sensing capacitor C_d. r_d is the resistance of the epi-layer between the inverter drain (inverter output) PN junction the substrate. Resistance of epi-layer can be estimated by the following formula [74]:

$$R_{epi} = \left(\frac{k_1 \rho_{epi} T}{(L+\delta)(W+\delta)} \right) \Bigg\| \left(\frac{k_2 \rho_{epi}}{2(W+L+2\delta)} \right) \tag{4.1}$$

k1, k2, and δ are empirical fitting parameters. T is the thickness of epi-layer and W and L are the contact width and length. k1 = 0.96, k2 = 0.71, and δ = 0.5 μm.

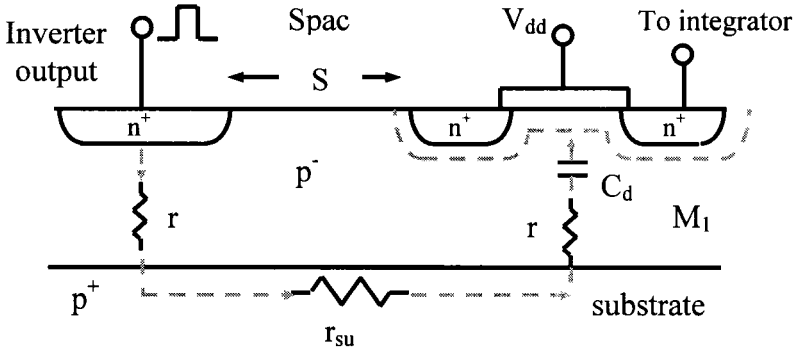


Figure 4-4: The sensing part of the substrate noise test circuit

In this substrate coupling noise measuring technique, the resistance rd and rsub (as shown in Fig. 4-4) do not affect the test result. Only voltage at the input node of sensing capacitor Cd is measured. The substrate coupling sensing NMOS (M1 shown in Fig. 4-3) is placed near inverter with distance S. The rest of substrate noise testing circuit is placed far from the sensing part and is surrounded by two or more N+/P+/N+ rings. So, the substrate coupling to the processing circuit is minimized. Inputs to the inverters can be connected to clock $\phi 2$ for test or power supply for calibration

4.2.2. Circuit Operation

When a clock is applied to the input of the inverter (see Fig. 4-3), the output of the inverter switches between Vdd and ground. Current is injected into the substrate through the drain capacitance at the output of the inverter. In order to increase the injection current, a large drain area for both the PMOS and NMOS transistors is selected for the inverter. The injected current flows in the substrate and causes a

voltage change along the path and is sensed by a MOS gate capacitor Cd (M1 shown in Fig. 4-4).

The substrate coupling noise is stored in the form of charge on the MOS sensing capacitor C_d. An integrator (see Fig. 4-3) processes the sensed substrate coupling noise voltage for N clock cycles until the next stage comparator changes state. The comparator compares the integrated substrate coupling voltage with a reference voltage V_{ref} every clock cycle. After N clock cycles, the output of the integrator is equal to the reference voltage, and the output state of the comparator changes. The updated comparator output terminates the counter that sums the number of digital cycles that have been applied to the noise source (the inverter) before the counter is terminated. The output of the counter is stored in an output buffer-register and passed from the test circuit. The sensing MOS capacitor C_d is small and is able to be quickly charged/discharged. The substrate coupling noise over a wide range of frequency can therefore be measured with this sensing circuit. The substrate coupling noise per switching event is

$$V_{sub} = \frac{C_f}{NC_d} V_{ref} \quad , \tag{4.2}$$

where C_f is the feedback capacitance in the integrator (see Fig. 4-5), C_d is the sensing capacitance of transistor M_1, N is a number converted from the output digital code, and V_{ref} is the reference voltage.

The change in the MOS capacitance C_d with the substrate voltage or the sensed substrate coupling noise voltage is small. In (4-2), C_f and C_d are design variables which have fixed values after the circuit design is completed. N is the decimal value of the output digital code. The measured result is not affected by the parasitic impedances along the substrate coupling path and the external test path. Note in (4-2) that a precise reference voltage V_{ref} is required for achieving an accurate measurement. The substrate coupling voltage can be measured independent of the type of substrate. This substrate coupling noise test technique is therefore an effective tool for evaluating different substrate coupling noise models.

4.3. Detailed Circuit Characteristics

A detailed circuit analysis of the substrate noise integration block is presented in this section. The proposed calibration process for improving the accuracy of the substrate noise measurement is also described.

4.3.1. Integration of the Substrate Noise

A schematic of the substrate coupling noise integrator circuit is shown in Fig. 4-5. The integrator is a fully symmetric differential switched capacitor circuit. The common-mode noise (such as the noises from power supply, ground, and the reference voltage V_{cm}) is removed or reduced by the differential circuit architecture. There is noise from the clock feedthrough from switches, OPAMP offset, mismatch of the two differential pathes, and some other random noise. Other noise sources

such as *1/f* noise, thermal noise, and *kTC* noise also exist in the integrator output analog voltage. In order to achieve accurate results, these noise sources must be removed from the integrator output. An on-chip calibration process is used in this test circuit to remove the integrator offset and other noise voltages. The circuit principle and operation are described in section 4.4.2.

The operation of circuit shown in Fig. 4-5 is as follow. V_{cm} is a common-mode reference DC voltage that sets the OPAMP output common-mode voltage, and V_{xp} and V_{xn} are the voltages at OPAMP input nodes. Δ is the amplifier offset voltage. There are two clock phases to complete an integrating cycle. The first phase is the sampling phase when clock ϕ_1 is "high" and clock ϕ_2 is "low". During the sampling phase, the substrate noise at the input of the substrate noise sensor (node *a* in Fig. 4-5) is sampled onto capacitor C_d, while the capacitor C_h holds the integrator output at the previous voltage which is sampled onto the capacitor C_f. The second phase is the output phase where the present sampled substrate noise is added to the previous substrate noise samples.

When clock ϕ_1 is "high" capacitors C_f are charged to $(V_o[n-1] + \Delta - V_{cm})$ and two capacitors C_h hold the previous output voltages $V_{outm}[n-1]$ and $V_{outp}[n-1]$. Capacitor C_d is charged to $V_{in}[n] - V_{cm}$. When clock ϕ_2 is high and ϕ_1 low, capacitor Charges stored in capacitors C_d and C_f are re-distributed in C_f and C_d. Apply the charge conversion law to the OPAMP inputs, the output differential voltage can be obtained

$$\Delta V_o[n] = \frac{C_d}{C_f} V_{in}[n] + \Delta V_o[n-1] + 2\Delta - \frac{C_d}{2C_f}\Delta + \delta[n], \tag{4.3}$$

where $V_{in}[n]$ is the voltage at sensor input node a during ϕ_1, and Δ is the integrator offset voltage. δ is lumped noise voltage during each integration cycle.

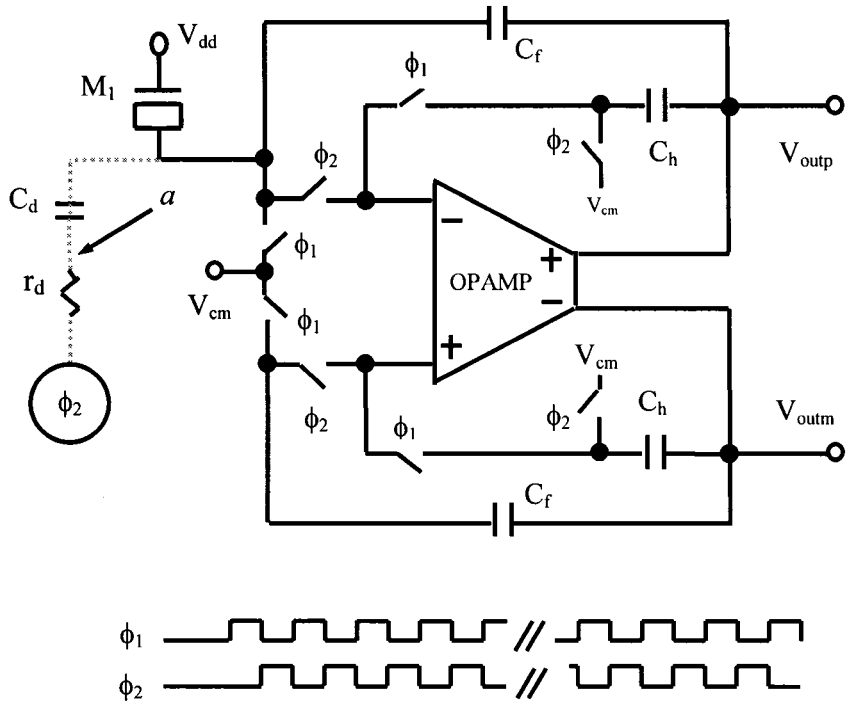


Figure 4-5: Substrate coupling voltage integrator circuit, a) schematic, b) clock waveforms

After N clock cycles, the differential voltage at the integrator output is

$$\Delta V_o[N] = \frac{C_d}{C_f}\sum_{k=1}^{N} V_{in}[k] + 2N\Delta - \frac{NC_d}{2C_f}\Delta + \sum_{k=1}^{N}\delta[k], \tag{4.4}$$

where $V_{in}[k]$ is the k_{th} sample voltage at node a during ϕ_1 and Δ is the integrator offset voltage. $\delta[N]$ is the lumped noise voltage at the output of the integrator.

The first term in (4-4) is the total substrate noise components after N clock injections. The remaining terms are noise components unrelated to substrate coupling. For every clock cycle, the voltage $V_{in}[k]$ is same and is equal to V_{noise}. At the end of the integration, the integrator output is equal to the reference voltage V_{ref}. The comparator output changes and both the counter and the integrator are stopped. The measured substrate coupling noise raw code is generated at the counter output. The substrate coupling noise per switching event can be obtained from the raw code by

$$V_{noise} = \frac{C_f}{C_d}\cdot\frac{V_{ref}}{N} + \frac{\Delta}{2} - 2\frac{C_f}{C_d}\cdot\Delta - \frac{C_f}{C_d}\cdot\frac{\sum_{k=1}^{N}\delta[k]}{N}, \tag{4.5}$$

Compare (4.2) and (4.5), the error exists in the measured data is

$$error = \frac{\Delta}{2} - 2\frac{C_f}{C_d}\cdot\Delta - \frac{C_f}{C_d}\cdot\frac{\sum_{k=1}^{N}\delta[k]}{N}, \tag{4.6}$$

4.3.2. Circuit Calibration

The coupling capacitor C_d is typically much smaller than the integrator feedback capacitor C_f. The third term in (4-4) is small, thereby making the second term dominant. For the circuit shown in Fig. 4-5, the amplifier offset voltage error and other noise sources in the measured substrate noise voltage [see (4-6)] can be removed by a calibration cycle. The operation of the calibration process proceeds as follow: by applying a power supply voltage at the input of the noise generator inverter during the whole calibration period and operating the circuit shown in Fig. 4-5. The input voltage $V_{in}[k]$ at the sensor input node a is zero. Run the test circuit, another digital code N_c is generated at the end of the calibration process. The new digital code is called the error (including the amplifier offset voltage error) calibration code. From (4-4), the total noise voltage is

$$\Delta V_o[N] = V_{ref} = 2N_c\Delta - \frac{N_c C_d}{2C_f}\Delta + \sum_{k=1}^{N_c}\delta[k], \tag{4.7}$$

From (4.5) and (4.7), the calibrated substrate coupling noise per switching event is

$$\Delta V_{noise} = \left(\frac{1}{N} - \frac{1}{N_c}\right)\cdot V_{ref} \quad , \tag{4.8}$$

and the corrected digital code is

$$N_{corrected} = \frac{V_{ref}}{\Delta V_{noise}} = \frac{N_c \cdot N}{N_c - N}. \tag{4.9}$$

In (4.8) and (4.9), N is the decimal value of the raw substrate coupling noise code, N_c is the decimal value of the calibration code, and V_{ref} is a DC reference voltage. The corrected noise code is given by (4.9). The noise in the reference voltage is the only source of error in the measured result. As in (4-4), the non-substrate related noise components of the measured results can be larger than the substrate noise voltage. The substrate noise cannot be measured without removing these non-substrate related noise components. With the use of an offset cancellation technique, the measured substrate noise is significantly more accurate and reliable. Furthermore, all of the noise acquisition processes including the A/D conversion are accomplished on-chip, therefore, complicated external test circuitry is not needed for this proposed substrate noise test circuit. The accuracy and error characteristics of this circuit are analyzed in the following section.

4.4. Accuracy and Error Analysis

Most of the offset voltage of an integrator is removed during the calibration process [see (4-4)-(4-9)]. However, due to the randomness of many noise sources such as power/ground noise, 1/f noise, and thermal noise at the integrator output,

the noise can only be completely removed if N and $N_c \rightarrow \infty$. The remaining error in the measured substrate noise voltage after the calibration process is

$$\Delta V_n = \sum_{k=0}^{N-1} \delta_k(t) - \frac{N}{N_c} \sum_{k=0}^{N_c-1} \zeta_k(t) \quad , \tag{4.10}$$

where δ_k is the noise voltage per clock cycle during sampling, and ς_k is the noise voltage per clock cycle generated during the calibration process. From (4.2), N and N_c are significant when a large reference voltage V_{ref} and feedback capacitor C_f is used.

Based on this analysis, a smaller measurement error is achieved if the reference voltage is large (large N). Since the substrate coupling voltage is usually small, in order to efficiently sense the substrate voltage (providing good sensitivity), the sensing capacitance cannot be excessively small. Increasing the size of the sensing transistor M_1 also reduces the error in C_d due to process variations which improves the linearity of C_d. An effective strategy to increase the measurement accuracy is to maintain a large reference voltage V_{ref} and feedback capacitor C_f.

4.5. OPAMP and Comparator

The OPAMP (operational amplifier) and comparator are the key components in the proposed substrate noise test circuit. Although the calibration process presented

in the previous section removes most of the OPAMP and comparator errors, a proper circuit architecture for the OPAMP and comparator is required in order to maximize circuit performance. The OPAMP circuit is described in section 4.6.1. The comparator design is presented in section 4.6.2.

4.5.1. OPAMP Circuit Design

The OPAMP used in the test circuit is required to have small offset and low noise. The fully differential architecture is selected for higher common-mode noise rejection and clock feedthrough noise reduction. The OPAMP circuit is shown in Fig. 4-6. The PMOS input differential pair stage is used to lower the OPAMP 1/f noise. The OPAMP is composed of two stages. The first stage is a folded-cascode PMOS gain stage and the second stage is a buffer stage. M11 supplies a DC bias current (the tail current) to the input differential pair, M1 and M2. M9 and M10 are matched to provide a DC bias current such that IM9 = IM11/2 + IM6. M5 and M6 are matched and carry the same DC currents. M7 and M8 are the cascode transistors for the differential-pair, M1 and M2. M3 and M4 are the cascode transistors of M5 and M6, respectively. M12 to M15 make up the second stage. The open-loop gain of the OPAMP is

$$A = g_{m1} \cdot g_{m13} \cdot (r_{ds12} // r_{ds13}) \cdot [(r_{ds1} // r_{ds10}) \cdot r_{ds8} \cdot g_{m8}] // (r_{ds4} \cdot r_{ds6} \cdot g_{m6}) \quad . \qquad (4-11)$$

A common-mode feedback circuit sets the OPAMP output common-mode voltage to a constant level (the reference DC voltage Vcm).

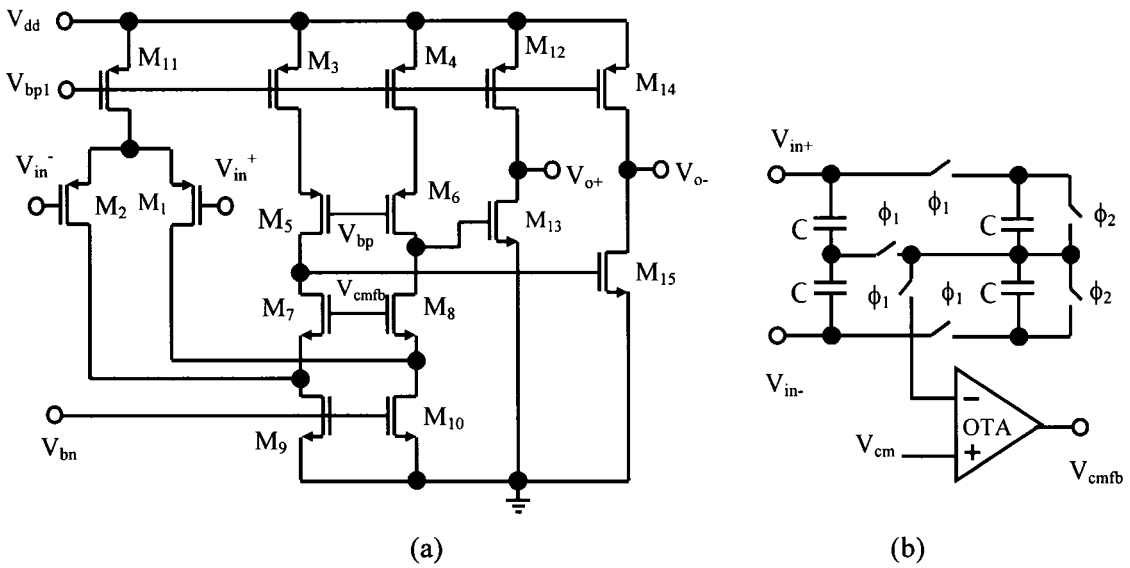
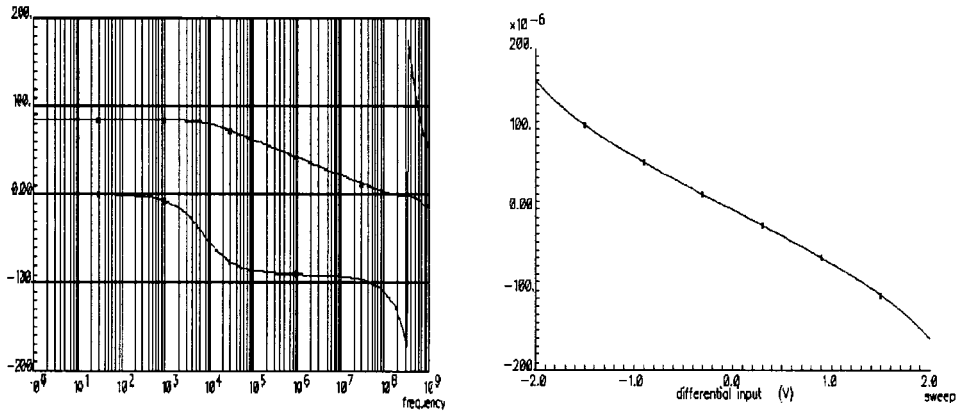


Figure 4-6: Low power folded-cascode OPAMP, a) schematic, b) common-mode feedback circuit

As shown in Fig. 4-6b, the common-mode control circuit has a switched-capacitor common-mode sensing circuit which generates an OPAMP output common-mode voltage every clock cycle and an OTA (operational transconductance amplifier). The sensed common-mode voltage is passed to an input of the open-loop OTA and the reference voltage V_{CM} is connected to another input of the OTA. The output voltage of the OTA V_{cmfb} controls the bias points of the main differential OPAMP as shown in Fig. 4-6a.

A simulation of the differential OPAMP illustrated in Fig. 4-6 is shown in Fig. 4-7. Results of SPICE simulation of the OPAMP are listed below where the following assumed parameter values, V_{dd} = 3.3 volts, T = 27 °C, and C_L = 0.7 pF.

Open Loop Gain:	76 db	Power Dissipation:	7 mW
Input Offset Voltage:	< 0.3 mV	Unity Gain Bandwidth:	140 MHz
Phase Margin:	> 65 °	Input Common Mode Range:	-2 to +2 V



(a) (b)

Figure 4-7: Simulation of OPAMP, a) open loop voltage gain and phase margin, b) output offset voltage

The large open-loop gain provides the OPAMP with a small offset voltage over a wide input range. This small offset voltage is required to reduce the error of the test circuit. A schematic of the common-mode voltage feedback circuit is illustrated

in Fig. 4-6b. The common-mode voltage generator determines the middle point of the two output voltages from the primary OPAMP and its output is compared with the reference voltage V_{cm}. A voltage V_{cmfb} is generated and applied to the gates of M_7 and M_8 as shown in Fig. 4-6a to set the common-mode voltage at the OPAMP outputs to the reference voltage V_{cm}.

4.5.2. Comparator Circuit Design

The performance of a comparator is important for processing low voltage signals. The input substrate coupling noise signal is small during the substrate coupling noise test. Due to the circuit calibration process described in section 4.4.2, the comparator offset is calibrated and removed from the measured data. Minimizing crosstalk between the input analog signal and the output digital signal of the comparator is therefore critical for maintaining the accuracy of the test result. The dynamic comparator with an input buffer to isolate the analog signal from the digital signals is described in this section. A schematic of a dynamic comparator is shown in Fig. 4-8.

M_1 to M_9 make up the latch amplifier where M_7 and M_8 supply the positive feedback. M_1 and M_2 make up the differential pair with M_5 supplying the tail current. The latch is composed of M_3, M_4, M_7, and M_8. Two source follower amplifiers, composed of transistors M_{14} and M_{16} and M_{15} and M_{17}, isolate the latch amplifier from the previous analog stage such that the noise in the previous stage does not affect the output of the comparator.

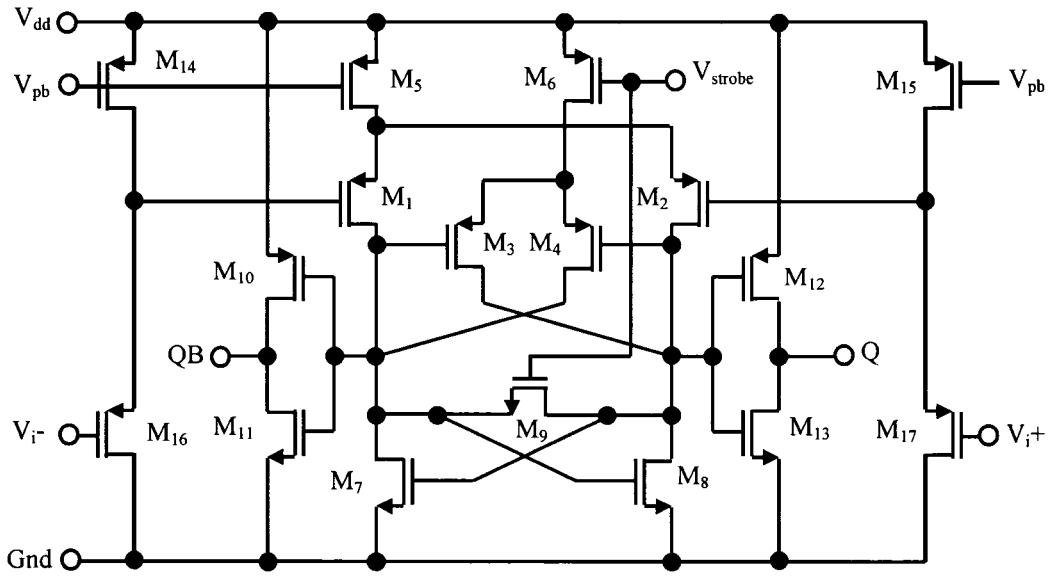


Figure 4-8: Schematic of the dynamic differential comparator

The operation of the comparator is as follow. When Vstrobe is high, the differential input is applied to the comparator, M3 and M4 are turned off, and M9 is turned on to force the latch to operate in the middle of the transition. The comparator is set to compare the input analog signals. When Vstrobe shifts to low, the positive feedback (or the latch) is enabled by turning on M6 and turning off M9. The latch outputs are generated rapidly based on the two input signals. The comparator output is thus valid during the phase when Vstrobe is low.

The switched-capacitor comparator block as shown in Fig. 4-3 is illustrated in Fig. 4-9. Four NOR gates at the comparator output hold the digital outputs when $\phi 2$ is high. The operation of the circuit shown in Fig. 4-9 is as follow. When $\phi 2$ is high

and $\phi 1$ is low, the input signals are sampled onto Cin. Voltages across the two capacitors are Vin+ - Vrefp and Vin- - Vrefp, respectively. In the next half clock cycle, $\phi 1$ changes to high and $\phi 2$ changes to low, and the input plates of capacitors Cin are connected to a DC voltage Vcm. Charge stored on Cin are redistributed to generate voltages at the comparator input nodes V+ and V-, as shown in Fig. 4-9. Application of the charge conservation law at the comparator high impedance input nodes permits the voltages at the two input nodes of the comparator to be determined.

$$V_+ = V_{cm} + V_{refp} - V_{in-} \quad , \tag{4.12}$$

$$V_- = V_{cm} + V_{refn} - V_{in+} \quad , \tag{4.13}$$

$$V_+ - V_- = (V_{refp} - V_{refn}) - (V_{in+} - V_{in-}) = \Delta V_{ref} - \Delta V_{in} \, . \tag{4.14}$$

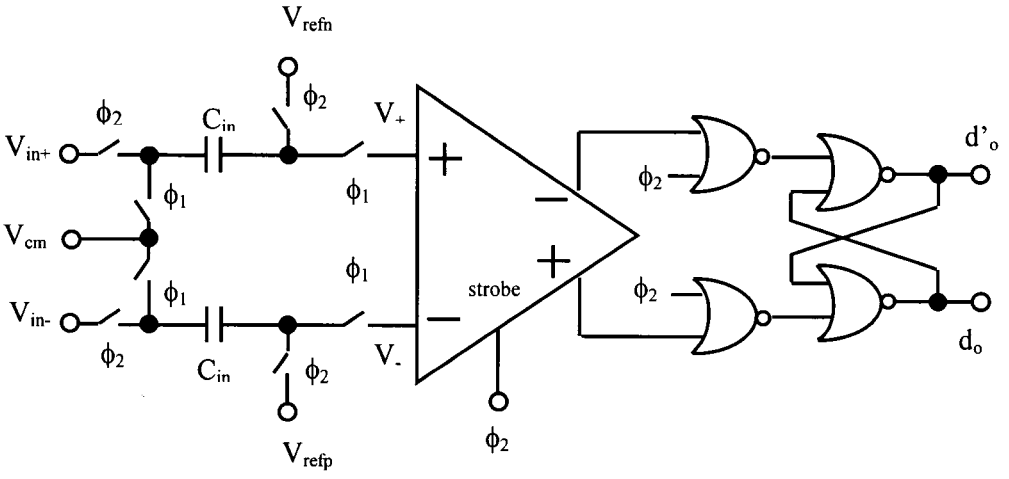


Figure 4-9: Switched-capacitor comparator block circuit

The input voltages, V+ and V-, as expressed in (4-12) and (4-13), are compared and the output digital signal is generated according to the input signals. If the differential input ΔVin is greater than the different reference voltage ΔVref, the output do is "1" and do' "0." Otherwise, do is "0" and do' "1." Due to the fully differential operation, clock feedthrough noise, power supply noise, and any other common-mode noises are greatly reduced. The comparator updates the digital output every clock by comparing the integrator outputs with the reference voltages.

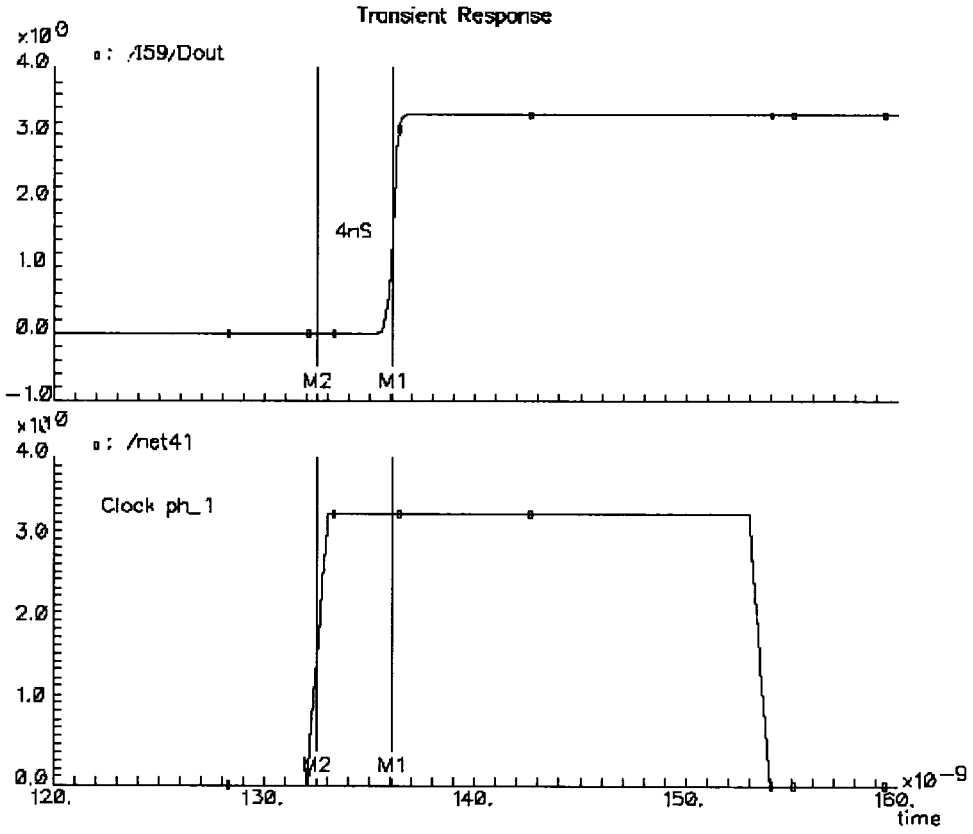


Figure 4-10: SPICE simulation of propagation delay of the comparator block

From (4.4), (4-12), (4-13), and (4.14), the outputs of the substrate noise test circuit are

$$V_+ - V_- = \left(V_{refp} - V_{refn}\right) - \frac{C_{cp}}{C_f}\sum_{k=0}^{N-1} V_{in}[k] - \frac{NC_{cp}}{2C_f}\Delta \quad , \tag{4.15}$$

$$V_{refp} - V_{refn} > \frac{C_{cp}}{C_f}\sum_{k=0}^{N-1} V_{in}[k] + \frac{NC_{cp}}{2C_f}\Delta, \quad d_o = 0 \quad , \tag{4.16}$$

$$V_{refp} - V_{refn} < \frac{C_{cp}}{C_f}\sum_{k=0}^{N-1} V_{in}[k] + \frac{NC_{cp}}{2C_f}\Delta, \quad d_o = 1 \quad . \tag{4.17}$$

The comparator output is reset to "0" at the beginning of each analysis. The comparator block compares the integrator outputs with the reference voltages for every clock cycle. Once the integrated substrate noise voltage is equal or greater than the differential reference voltage, a "1" appears at the comparator block output. The output "1" of the comparator block is applied to the counter "enable" input to stop the counting process. The comparator block shown in Fig. 4-9 has been analyzed and the resulting SPICE simulation is shown in Fig. 4-10. The circuit is simulated assuming a 3.3 volt power supply and a 24 MHz clock frequency. The 4 ns delay shown in Fig. 4-10 is caused by the two input source follower buffers (see Fig. 4-8). Removing the two source followers shown in Fig. 4-8 can reduce both the delay time and the power dissipation. The accuracy of the analysis, however, may also be reduced.

4.6. Simulation Results

The proposed substrate noise test circuit includes an integrator, a comparator block, a counter, and an on-chip timing circuit. The circuit has been simulated using SPICE. The sensing MOS capacitor has a width of 15 μm and a length of 1.8 μm. The total capacitance of C_d is about 89 fF. The reference voltage at the comparator input is 600 mV. The noise generator inverter is not included in the simulation. A voltage is assumed to be coupled to the input node of the sensing capacitor C_d. The voltage at the C_d input node is set to 30 mV and 0 mV in order to generate the raw and calibration codes, respectively.

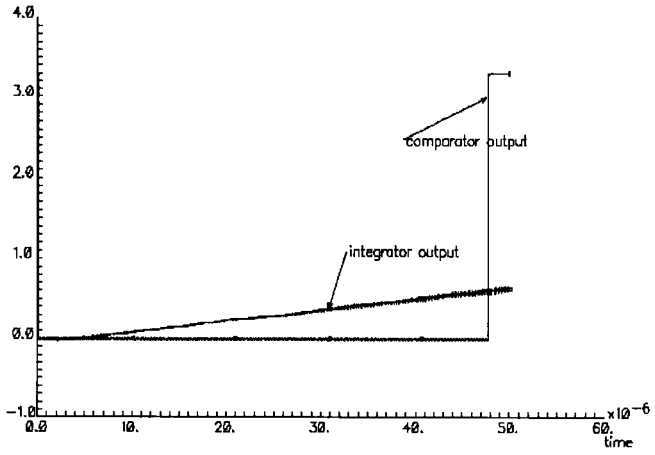


Figure 4-11: SPICE derived waveforms of the integrator and comparator outputs.

V_{ref} = 600 mV, f = 5 MHz, and the output is 235

Two codes, the raw code and the calibration code, are generated from SPICE. The SPICE simulation of the comparator output is shown in Fig. 4-11. As shown in

Fig. 4-11, the comparator output changes from 0 to 1 when the integrator output reaches 600 mV (the reference voltage V_{ref}). The calculated code from (4.2) is 178 and the simulated raw code is 235. A calibration code of 720 is obtained after the calibration process. From (4.9), the calibrated code is 177, which is quite close to the actual (calculated) code of 178.

The same procedures have been applied to various substrate noise voltages. These results are shown in Fig. 4-12. The raw simulation results are different as compared to the calculated (actual) values caused by the OPAMP offset and other noise components. The SPICE simulation produces a calibration code N_c of 720. From (4.8), the raw codes are calibrated and are depicted in Fig. 4-12. As shown in Fig. 4-12, the calibrated codes are close to the calculated codes. The difference between the calibrated code and the calculated (raw) code is less than 1%.

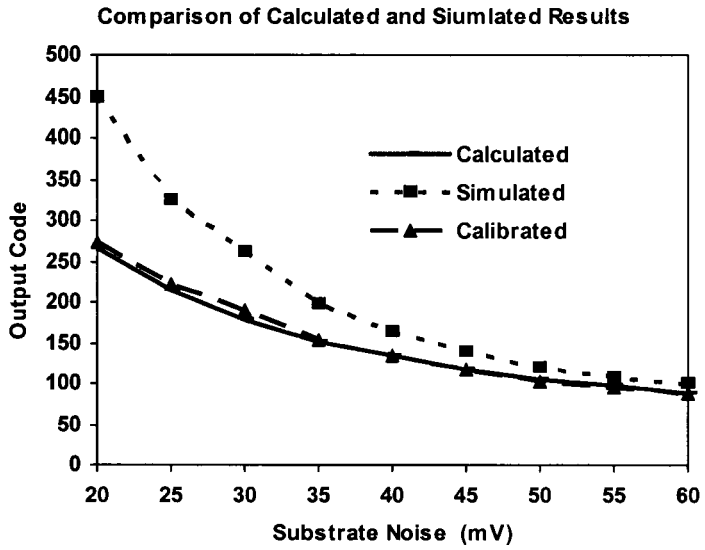


Figure 4-12: Comparison of calculated, simulated, and calibrated digital codes

4.7. Conclusions

The proposed test circuit can accurately measure substrate coupling noise. The measurement technique can be used to analyze different types of substrates. With this test circuit, different substrate coupling models can be evaluated.

The proposed substrate noise test circuit has an on-chip calibration function to remove extraneous noise sources from the test results. With this calibration step, only the substrate coupling noise is included in the digital output code. Less than 1% error from the actual value is achieved. This test circuit includes an efficient on-chip analog-to-digital converter so that the measured substrate coupling noise is in the form of a digital code. With this proposed circuit, the noise voltages from the pads, bounding wires, package frame, and external cables/fixture do not affect the accuracy of the measurement. The only noise source that can affect the accuracy of the measurement is from the reference voltage. In order to enhance the measurement accuracy, a low noise reference voltage is therefore preferable.

Chapter Five: A Circuit Technique for Accurately Measuring Coupling Capacitance

Complex, high speed digital circuits together with high performance analog circuits are commonly integrated on the same IC substrate. In such mixed-signal systems, fast switching transients produced within the digital circuits can couple into sensitive analog components, thereby limiting the analog precision. The coupling noise between the on-chip analog and digital circuits can corrupt low level analog signals, generating a significant error in the analog signal voltage. Coupling between analog signal lines also affects the performance of many analog circuits.

Unlike the digital circuit design and simulation process, an analog circuit requires significant information characterizing each individual component. To design and simulate mixed-signal ICs, accurate models are needed. Test data verifying these models is therefore increasingly important. In this paper, an accurate coupling capacitance test technique is presented.

Many coupling capacitor models have been developed during the past years [75]-[78]. The process of measuring coupling capacitance, however, has been based on simple two line test structures [38]-[41]. The output signals of these test circuits are weak analog voltages which are typically affected by other noise sources. The I/O pads, bonding wires, package frame, external circuits, and the cable also affect

the output analog signal, severely decreasing the accuracy of the measurement (see Fig. 5-1). Expensive equipment is typically required to test these circuits. In order to develop accurate test results and to simplify the measurement process, dedicated data sensing and analog-to-digital conversion circuits must also be included on-chip.

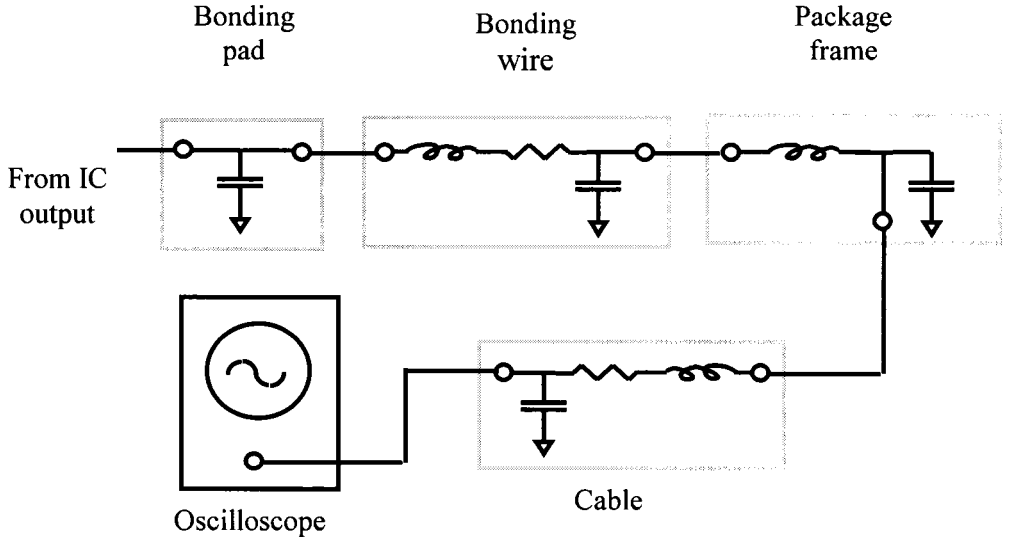


Figure 5-1: Parasitic impedances along an IC test path

A technique for accurately measuring coupling capacitance is presented in this chapter. The proposed on-chip test circuit can accurately and efficiently measure the line coupling capacitance and its noise voltage. A simple on-chip analog-to-digital converter converts the measured analog signal into a digital signal. Therefore, the I/O pads, bounding wires, package frame, external cables, and external test circuit do not affect the accuracy of the measurement. On-chip

calibration is also included to further extend the test accuracy. Less than 1% error as compared to SPICE is achieved with this circuit. The circuit provides an effective and accurate technique for evaluating a variety of existing capacitance coupling models. Simple test equipment is required for reading out the measured data.

This chapter is organized as follow. The near field or capacitance coupling effect is reviewed in Section 5-1. In Section 5-2, the principle of the on-chip test circuitry is described. Details of the design of the on-chip circuitry are presented in Section 5-3. The error of the capacitance coupling test circuit is analyzed in Section 5-4. Analytic and SPICE simulation results are presented and compared in Section 5-5. Finally, some conclusions are provided in Section 5-6.

5.1. On-Chip Coupling Between Lines

In mixed-signal ICs, coupling between signal lines is considered as near-field coupling. Near-field coupling has two components: electrical field coupling (capacitive coupling) and magnetic field coupling (inductive coupling). The inductive coupling is usually much smaller than the capacitive coupling for frequencies below a gigahertz. Only capacitive coupling is therefore considered in this chapter. In the latest submicrometer integrated circuits, both the line width and spacing are less than the line thickness and the separation between lines on multi-layer lines. As a result, the line-to-line capacitance on the same layer is often

dominant. When two or more lines are close to each other, some or all of these lines carry current, establishing an electric field. The signals on these wires interact through an electric field flux, which is represented by a coupling capacitance. Fig. 5-2 illustrates the near field electric coupling between two wires on the same layer. An electric field flux links the two wires when currents flow in the wires.

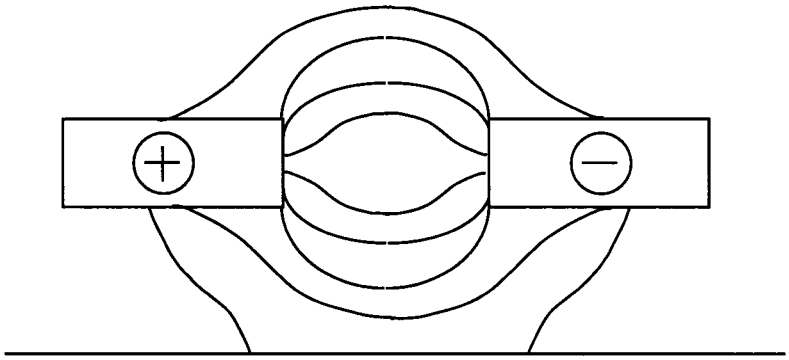


Figure 5-2: Electric Field Coupling Flux between Parallel Lines

The near field coupling strongly depends upon the distance between the two lines. One way to reduce the line-to-line coupling is to increase the spacing, thereby reducing the crosstalk capacitance between wires by altering the routing pattern such that the sensitive analog nodes are far from those circuits that switch most frequently.

Simple closed form expressions for coupling in arbitrary networks has been an open problem since the late 1960's [37]. Formulae characterizing coupling capacitance have been developed [75]-[78], for example, by Chang [75], Elmasry

[76], Sakurai [77], and Yuan [78]. Other relevant research in this area includes the work in [85]-[89]. However, most reports on measurement of coupling capacitance are based on simple two-line test structure [38]-[41]. The output signals of test chips are very weak analog voltages and are contaminated by other noises. The parasitic components of pads, bonding wires, package frame, external circuits and cable also affect the output analog signal and severely decrease the measurement accuracy.

Parasitic capacitors in a two line system are shown in Fig. 5-3 where C10 and C20 are the unit length capacitance of line 1 and 2 to substrate. C12 is the coupling capacitance between the two lines. Other capacitors are usually small as compared to C10, C20, and C12. A proposed circuit is presented to accurately test the coupling capacitance C12 between two lines. Other coupling capacitors can also be measured with this proposed circuit under different test configurations.

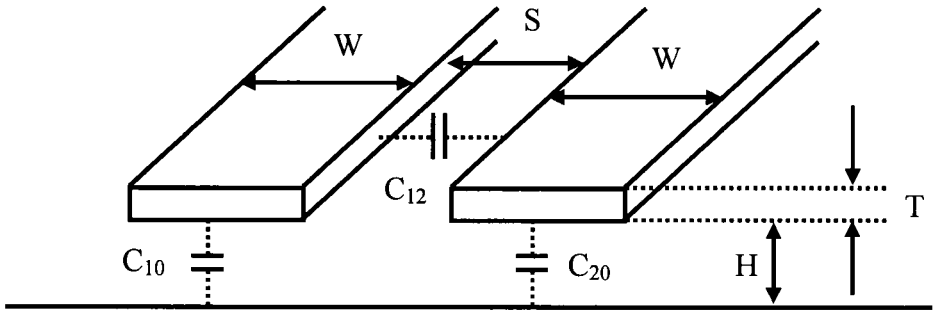


Figure 5-3: A two line system with parasitic capacitances

5.2. Circuit Principles

The proposed line coupling noise voltage testing circuit has a differential amplifier and consists of a two line coupling structure, an integrator, a comparator, a counter, and a digital control circuit, as shown in Fig. 5-4. The differential operation removes the common-mode noise from the power distribution network, thereby producing a more accurate capacitive coupling voltage.

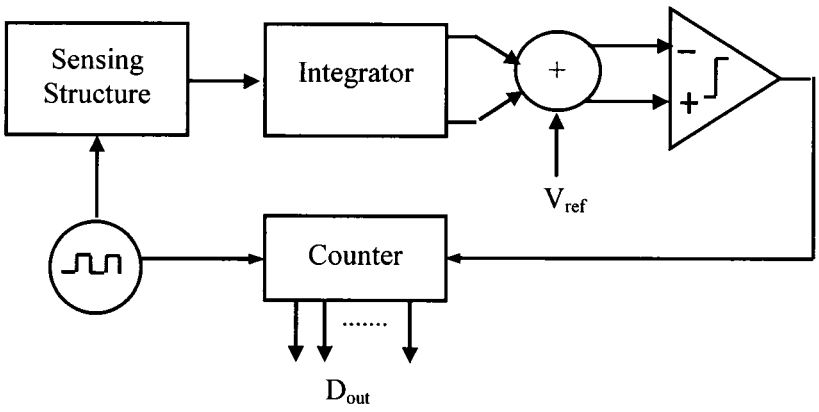


Figure 5-4: Capacitive coupling test circuit

The two line structure for sensing the capacitive coupling is shown in Fig. 5-5. Both lines have the same length L and width W, and are separated by a distance S. A digital clock is applied on one of the two lines. The other line is connected to the input of the integrator.

5.2.1. Operation of the Test Circuit

As shown in Fig. 5-5, a digital clock is applied to the fixed length digital line as a noise source to couple voltage to the integrator input. During each clock cycle, a

voltage is coupled to the integrator input through the coupling capacitor Ccp. This coupled voltage is integrated and compared to the reference voltage Vref every clock cycle (see Fig. 5-4). At the end of the ith clock, the voltage at the comparator input is

$$\Delta V_{comp\_in}[i] = V_{ref} - \Delta V_{noise}[i] \quad , \tag{5.1}$$

where ΔVnoise[i] is the differential output of the integrator at the end of the ith clock.

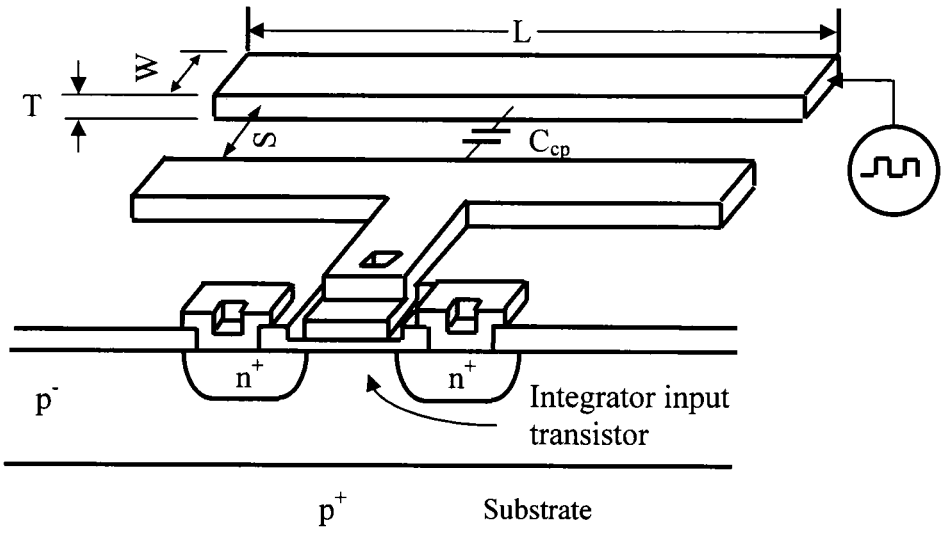


Figure 5-5: Structure for sensing capacitive coupling

At the end of the Nth clock cycle, the integrator produces an output voltage equal to the reference voltage Vref, changing the output state of the comparator.

The updated comparator output terminates the counter which sums the number of digital clock cycles that have been applied to the digital line before the counter is terminated. The output of the counter is stored in an output buffer register and passed to the external test circuit.

5.3. Detailed Circuit Characteristics

A schematic of the capacitive coupling noise integrating circuit is shown in Fig. 5-6. $\phi 1$ and $\phi 2$ are the two non-overlapped inverting clocks.

During the test, the amplifier-offset voltage and other noise sources are integrated by the test circuit, producing a large error in the measured results. In this paper, an on-chip calibration process is used to solve this problem. The integrator output after N clock cycles is

$$\Delta V_o[N] = \frac{C_{cp}}{C_f} V_{in}[N] + \Delta V_o[N-1] + 2\Delta - \frac{C_p}{2C_f}\Delta + \xi[N], \qquad (5.2)$$

where Vin[N] is the voltage on the digital line during $\phi 1$ (which is Vdd), and Δ is the integrator offset voltage which is generated by a combination of opamp offset, clock feedthrough effects, mismatches in the capacitors, common mode noises and process related errors. ξ[N] is the lumped noise voltage at the integrator output.

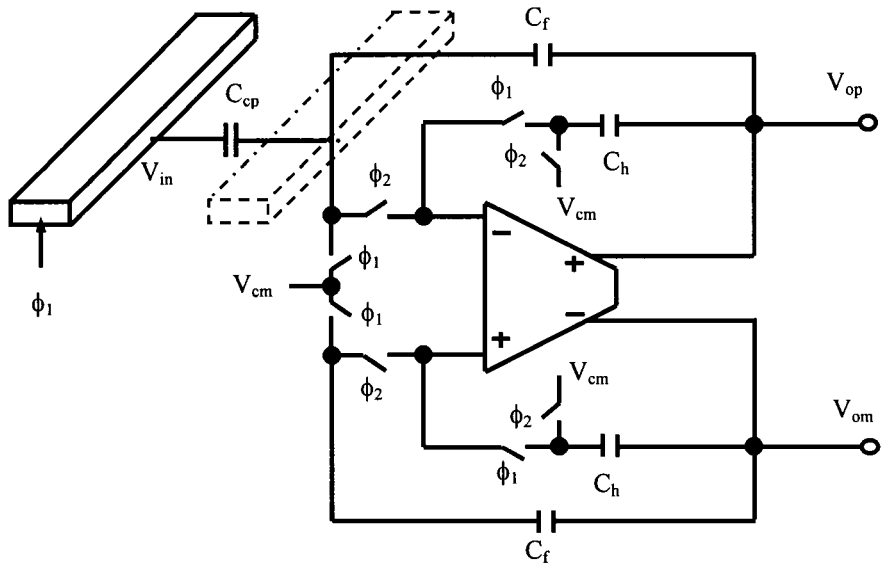


Figure 5-6: Switched capacitor voltage integrator circuit

When the number N is sufficiently large,

$$\xi[N] = \frac{C_{cp}}{C_f} \sum_{k=0}^{N-1} \delta[N-k] = 0 \quad , \tag{5.3}$$

where δ is the total output noise generated during each clock cycle.

At the end of the Nth clock cycle, the differential voltage at the integrator output is (Vin = Vdd, and assuming N is large)

$$\Delta V_o[N] = \frac{C_{cp}}{C_f} N V_{in} + 2N\Delta - \frac{NC_{cp}}{2C_f}\Delta \quad . \tag{5.4}$$

When the integrator output ΔVo[N] is equal to the reference voltage Vref (see Fig. 5-3), the output of the comparator changes, terminating the counter. The counter output N and Vref have the following relationship,

$$V_{ref} = \frac{C_{cp}}{C_f} N V_{dd} + 2N\Delta - \frac{NC_{cp}}{2C_f}\Delta, \tag{5.5}$$

where Vdd is the power supply voltage, Cf is the integrator feedback capacitance, and Δ is the integrator offset voltage. The capacitance Ccp in (5-5) is the measured line coupling capacitance. During the measurement, capacitor C10 (shown in Fig. 5-3) is driven by a voltage source and C20 has a constant voltage Vcm across it. The measured capacitance Ccp is C12 , as shown in Fig.5-3.

5.4.1. Circuit Calibration Process

In order to measure the line coupling capacitance Ccp, the second and third terms in (5-5) must be made negligible. Removing the second and the third term in (5-5) is accomplished by operating the test circuit with the digital noise source line grounded, essentially calibrating the circuit. The digital code NC, generated from the calibration process, is called the error reference code. When Vin[n] is zero, the total error from (5-4) is

$$\Delta V_n[N_C] = 2N_c\Delta - \frac{N_C C_{cp}}{2C_f}\Delta = V_{ref}\,. \tag{5.6}$$

From (5-5) and (5-6), the coupling capacitance C_{cp} is

$$C_{cp} = C_f \cdot \frac{N_c N}{N_c - N} \cdot \frac{V_{ref}}{V_{dd}} \quad , \tag{5.7}$$

where N and N_C are decimal values of the digital codes at the circuit output.

5.4. Accuracy and Error Analysis

Most of the noise voltage at the output of the integrator can be removed by a calibration technique [see (5-4)-(5-6)]. However, due to the random nature of many noise sources, such as power/ground noise, 1/f noise and thermal noise at the integrator output, the total noise can only be completely removed when N and Nc $\rightarrow \infty$. The final expression for the measured coupling capacitance Ccp is

$$C_{cp} = \frac{N_c N}{N_c + N} \cdot \frac{V_{ref}}{V_{dd}} \cdot \frac{C_f}{1 + \frac{1}{V_{dd} \cdot N}\sum_{k=0}^{N-1}\delta_k(t) - \frac{1}{V_{dd} \cdot N_c}\sum_{k=0}^{N_c-1}\eta_k(t)}, \tag{5.8}$$

where δk is the total noise voltage at the integrator output per clock cycle during a sampling period, and ηk is the total noise voltage per clock cycle generated during

the calibration process. Comparing (5-7) with (5-8), the total error after the calibration process is

$$\Delta C_{cp} = C_f \cdot \frac{N_c N}{N_c + N} \cdot \frac{V_{ref}}{V_{dd}} \cdot \frac{\frac{1}{N}\sum_{k=0}^{N-1}\delta_k(t) - \frac{1}{N_c}\sum_{k=0}^{N_c-1}\eta_k(t)}{V_{dd} + \frac{1}{N}\sum_{k=0}^{N-1}\delta_k(t) - \frac{1}{N_c}\sum_{k=0}^{N_c-1}\eta_k(t)}. \tag{5.9}$$

Based on this analysis, a small measurement error is produced if a large reference voltage (larger N and Nc) is selected. In order to make C12 (see Fig. 5-3) dominant, long but narrow parallel lines in the test structure (see Fig. 5-4) are utilized. For the same reference voltage Vref, however, test structures having a large coupling capacitance should have smaller N and Nc numbers. The measurement error, as analyzed above, increases with larger capacitance Ccp. As long as the OPAMP operates within the linear range, a larger reference voltage is preferable to enhance the accuracy of the measurement.

5.5. Simulation Results

The test circuit has been simulated at the transistor level. SPICE simulation results are shown in Figs. 5-7 and 5-8, and the analytic results are compared to SPICE in Fig. 5-9. In Fig. 5-7, the differential waveforms of the integrator outputs and comparator output are displayed. In order to produce accurate simulation results, the signal on the digital line begins at 2.5 uS to ensure the system has settled sufficiently. The power supply is 3.3 volts, the differential reference voltage

is 1 volt, and the common mode reference voltage Vcm is 1.65 volts. The integrator feedback capacitor Cf is 800 fF and the coupling capacitance Ccp is 2 fF. As shown in Fig. 5-7, the output of the integrator increases as additional samples are summed. Because the coupling voltage per switching event is same, the integrator output has a linear relationship with the number of samples. When the integrator output is equal to the reference voltage, the test is completed.

The waveforms shown in Fig. 5-8 are the integrator differential output for a coupling capacitance of 2 fF, 4 fF, and 6 fF. As indicated by (5-4), the slope of the integrator output is a constant,

$$\frac{d(\Delta V_o[N])}{d(N)} \approx \frac{C_{cp}}{C_f} V_{dd} \quad . \tag{5.10}$$

Increasing Ccp increases the slope of the integrator output waveform. As shown in Fig. 5-8, the SPICE waveforms agree with the analytic solutions from (5.10).

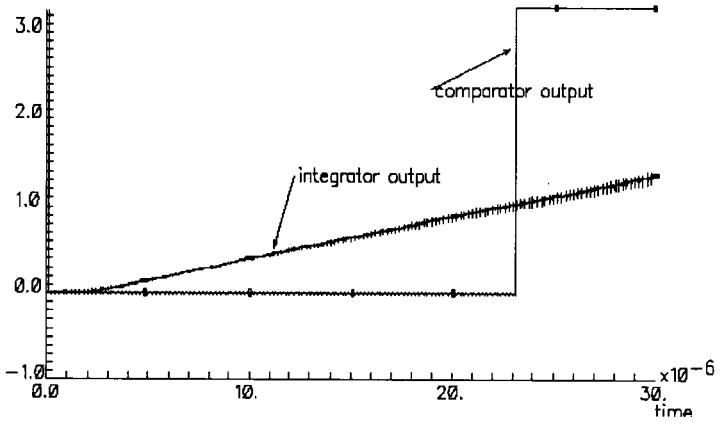


Figure 5-7: SPICE simulation of the integrator differential and comparator outputs

The simulated raw output code N is 102 and the calculated value is 91. A calibration code Nc of 680 is obtained. From (5-7), the calculated coupling capacitance Ccp is 2.02 fF (a Ccp of 2 fF is used in the simulation). The difference between the calculated and simulated Ccp values is about 1%.

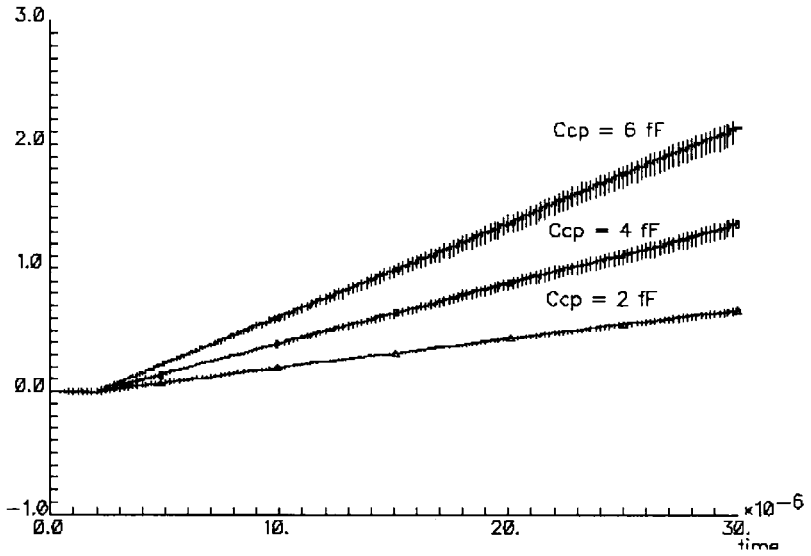


Figure 5-8: comparator output with V_{dd} = 3.3 volts, V_{ref} = 1 volt, C_f = 800 fF

The calculated, measured, and calibrated codes for different values of the coupling capacitance Ccp are displayed and compared in Fig. 5-9. According to Fig. 5-9, the measurement accuracy of the proposed circuit has an error of less than 1% for a coupling capacitance between 2 fF and 5.5 fF. The effective range of the measurement (producing an error of less than 1%) of the capacitance Ccp is wider with a larger reference voltage Vref. The error of this circuit, as analyzed in (5-10),

depends upon the values of N and Nc. In order to average the random noise at the integrator output, a large number of integration cycles is desired.

Errors incurred with high coupling capacitances (see Fig. 5-9) are due to an inadequate number of integration cycles. The noise at the integrator output, therefore, is not completely removed. For small coupling capacitance (see Fig. 5-9), the parasitic coupling capacitance in the two line system seriously degrades the measured results. Large errors, therefore, exist for low values of Ccp. Increasing the reference voltage can extend the accuracy of the measurement range toward high values of Ccp. The lower end of the measurement range cannot be improved by increasing Vref. Short parallel lines in the sensing structure (see Fig. 5-5) of the test circuit should, therefore, be avoided.

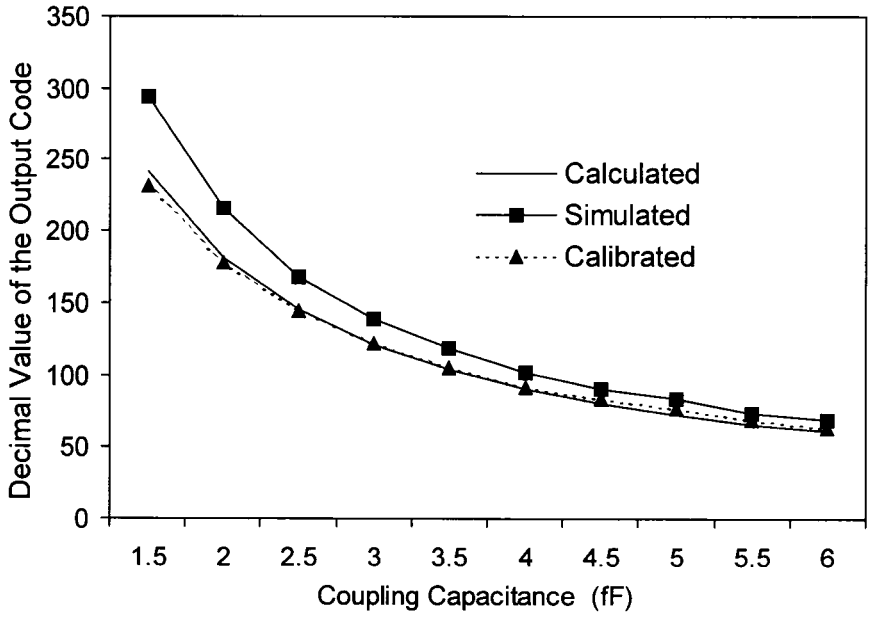


Figure 5-9: Comparison of calculated, simulated, and calibrated digital codes

5.6. Conclusions

An accurate line coupling capacitance test circuit is proposed in this chapter. The circuit can be applied to accurately measure the coupling capacitance between any conductive layers. With this line capacitive coupling technique, different capacitance coupling models can be evaluated. With on-chip calibration, only the coupling noise is included in the digital output code. Less than a 1% error is achieved when comparing the calculated coupling capacitance with SPICE simulation. The noise voltages from the I/O pads, bounding wires, package frame, external cables, and test circuit do not affect the accuracy of the measurement. The only noise sources that could produce errors originate from the power supply and the reference voltage. In order to enhance the measurement accuracy, low noise power supply voltage and reference voltages are recommended.

Chapter Six: Clock Feedthrough in CMOS Analog Transmission Gate Switches

An analysis of clock feedthrough in CMOS analog transmission gate (TG) switches is presented in this chapter in details. A clock feedthrough mechanism and a related model of a transmission gate switch are established in the current-voltage domain. An analog switch is a basic component in integrated circuits (ICs). The on/off behavior of an analog switch is controlled by the gate voltages that govern the presence of charge in the inversion channel underneath the gates. A CMOS transmission gate switch is shown in Fig. 6-1.

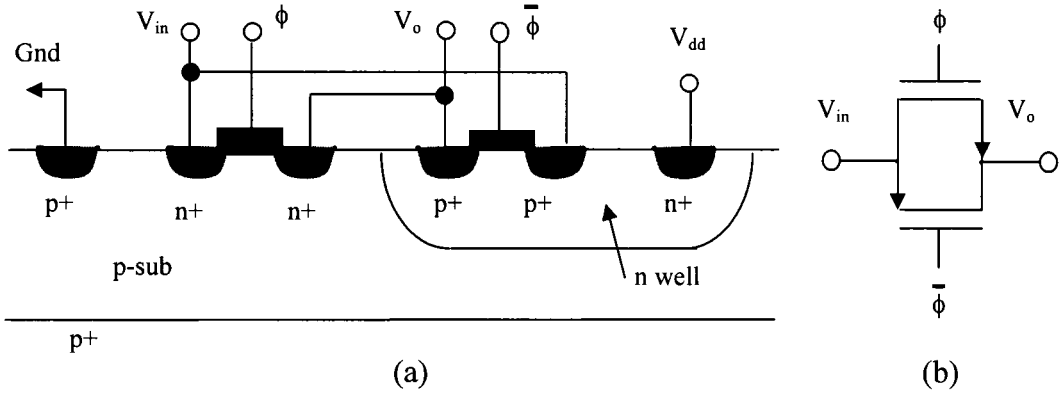


Figure 6-1: CMOS TG analog switch: (a) device cross section, (b) circuit symbol

With process scaling and the increasing demand for portable systems, a lower power supply voltage has become common. In order to pass a large analog signal,

single MOSFET switches are replaced by transmission gate switches in many analog circuits. A TG switch has an approximately uniform on-resistance, and can pass wide analog signal swings.

Clock feedthrough is a fundamental problem in analog ICs. The most commonly accepted clock feedthrough mechanism (in the charge domain) occurs when the switch is turned off, dispersing the charge in the inversion channel, forcing current to flow either into the substrate or the load capacitor at the MOSFET drain or source. This mechanism produces an error voltage on the load capacitor. This flow of electrons was first called charge feedthrough by Stafford et al. [84]. Sheu and Hu [85], and Shieh et al. [86] published analytical models of strong inversion channel injection and gate-to-drain overlap capacitive coupling in NMOS switches. Wegmann used the continuity equation to model clock feedthrough for a single MOSFET switch [87]. More recently, Gu and Chen described a charge injection model that includes weak inversion injection [88]. All of these papers, however, only consider a single NMOS switch. In this chapter, clock feedthrough in a TG switch is modeled as coupling from the transistor gate and overlap capacitors. A clock feedthrough mechanism for an analog TG switch is also presented in the current-voltage domain. This clock feedthrough mechanism is applicable for both TG switches and for single PMOS or NMOS analog switches.

In section 6-1, the mechanism of clock feedthrough in TG switches is discussed. Clock feedthrough in the full conduction region is considered in section 6-2. Clock

feedthrough noise generated in the half conduction region is analyzed for a TG switch in section 6-3. Clock feedthrough in the subthreshold/cutoff region is described in section 6-4. A discussion of these results is presented in section 6-5. Some conclusions are provided in section 6-6.

6.1. Mechanism of Clock Feedthrough in TG Switches

Three currents flow in a MOSFET at the time the switch is turned off (see Fig. 6-2). These currents are the MOSFET drain current ID, the coupling current Igd through the overlap capacitor Cgd, and the coupling current Icox through the gate capacitor Cox.

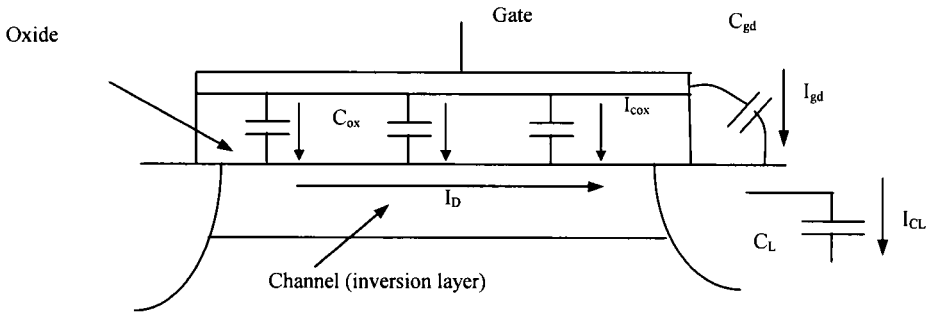


Figure 6-2: Current flow in a MOSFET

Clock feedthrough error is due to capacitive coupling from the overlap capacitor Cgd and the gate capacitor Cox to the sample and hold (S/H) capacitor CL. The MOSFET drain current ID supplies charge to compensate for the error voltage (generated from the coupling) until the MOSFETs are completely cut-off. The clock feedthrough error voltage ΔVerror on an S/H capacitor CL is determined by

the difference between the coupled charge and the charge injected by the transistor current. A slower gate voltage signal provides the MOSFET drain current with additional time to compensate for the coupling error.

$$\Delta V_{error} = \frac{\Delta Q}{C_L} = \frac{1}{C_L} \cdot \left(\Delta Q_{coupling} - \int_0^t I_D(t) dt \right). \tag{6.1}$$

6.1.1. Clock Feedthrough in TG Switches

The circuit depicted in Fig. 6-3 is a CMOS TG switch. An input voltage Vin is sampled onto the S/H capacitor CL by applying a low voltage at the gate of the PMOS transistor and a high voltage at the gate of the NMOS transistor. Due to coupling from capacitors Cox and Cgd, an error voltage is generated on CL when the switch is turned off (called switch-off). Switch-off in this paper is defined as the time period when the gate voltage on an NMOS transistor changes from Vdd to 0 and the gate voltage on a PMOS transistor changes from 0 to Vdd.

Three pairs of current flow in a TG switch during the period of switch off. These current pairs are divided into noise generating pairs and noise reducing pairs. As shown in Fig. 6-3, the first noise generating current pair, In and Ip, couples currents from the gates to the load capacitor through the MOSFETs gate-to-drain overlap capacitors. The second noise generating pair is Icoxn and Icoxp. Currents in the noise generating pairs flow in opposite direction and compensate each other. For

perfectly matched current pairs, noise generated from these pairs is zero when both transistors conduct (the full conduction region as discussed later). The noise reducing current pair, IDN and IDP, are currents supplied by the MOSFETs in the TG switch.

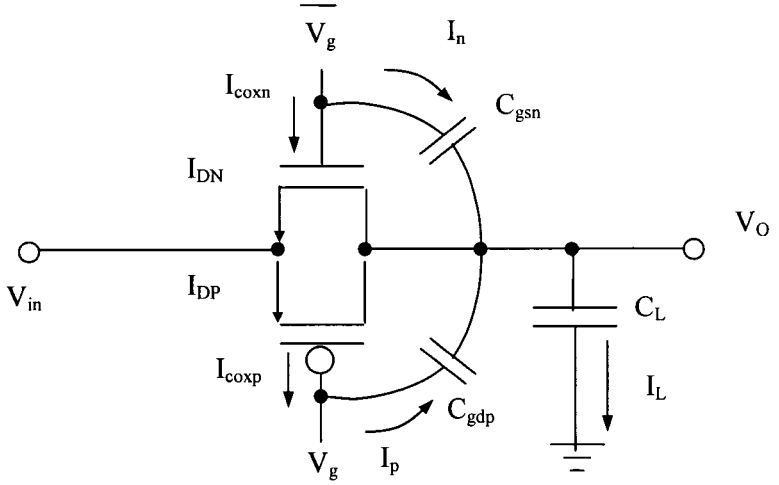


Figure 6-3: An analog TG switch with an S/H capacitor, C_L

6.1.2. Modeling Clock Feedthrough in TG Switches

The transmission gate switching process is modeled in this subsection and shown in Fig. 6-4. The MOSFETs are modeled as voltage controlled resistors. Coupling from the gate capacitors and the gate-to-drain overlap capacitors are represented by currents Icoxn, Icoxp, Igdn and Igdp. The MOSFETs are assumed to operate in the linear region and produce the MOSFET currents, I_{DN} and I_{DP}.

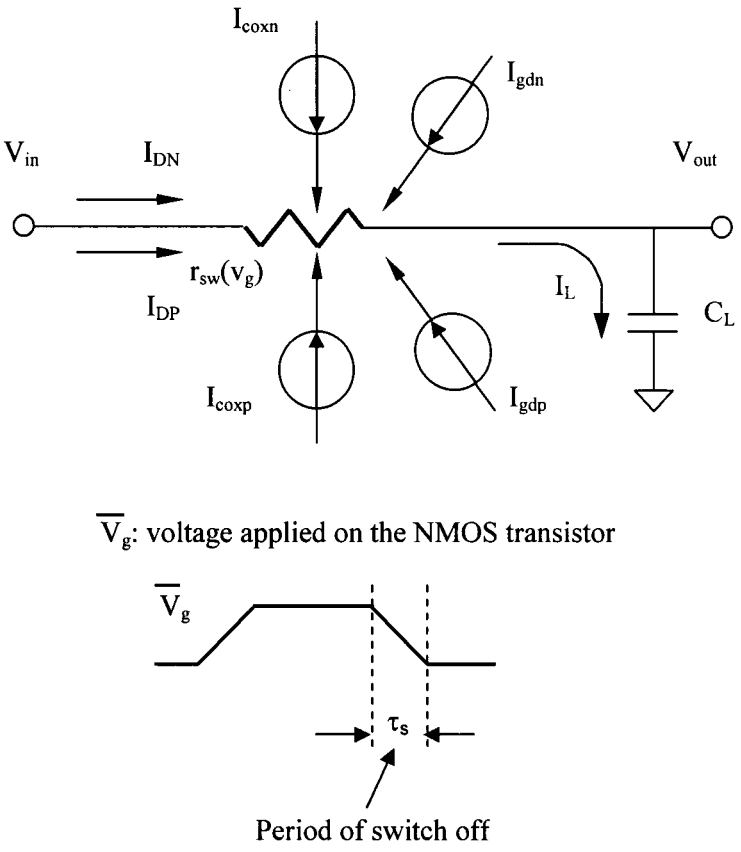


Figure 6-4: Model of an analog TG switch during switched off

Current and voltage differential equations can be established from the circuit shown in Fig. 6-4. These equations are solved in sections 6.3, 6.4, and 6.5, permitting the clock feedthrough noise voltage generated within each region to be determined.

6.1.3. Region Map

The voltages applied at the gates of the PMOS and NMOS transistors are modeled as a ramp signal as shown in Fig. 6-5. The operation of the TG switch

during switch-off is divided into three regions based on the states of the two transistors. When the ramp input voltage Vg is applied at the gate of the PMOS transistor and (Vg)' is applied at the gate of the NMOS transistor, the TG operates in one of three regions: full conduction, half conduction, and subthreshold/cutoff. During full conduction, both of the PMOS and NMOS transistors conduct. The half conduction region occurs when only one of the two transistors conducts current and the other transistor is off. The subthreshold/cutoff region occurs when both of the PMOS and NMOS transistors are off. The voltages applied on the gates of the transistors are

$$V_g = V_{dd} \cdot t/\tau_s, \tag{6.2}$$

$$\overline{V_g} = (1 - t/\tau_s) \cdot V_{dd}. \tag{6.3}$$

The times t_a and t_b, shown in Fig. 6-5 are, respectively,

$$t_a = \tau_s \cdot (V_{in} - |V_{TP}|)/V_{dd}, \tag{6.4}$$

$$t_b = \tau_s \cdot (V_{dd} - V_{in} - V_{TN})/V_{dd}. \tag{6.5}$$

The absolute value of the clock feedthrough in each region is directly proportional to the length of time the TG switch remains in that region. For example, as shown in Fig. 6-5, for an input voltage Vin (the sampled voltage), the length of time the switch operates in the full conduction region is ta, tb - ta in the half conduction region, and τs - tb in the subthreshold/cutoff region. The relationship between the region map and clock feedthrough noise is used to explain the results presented in the following sections. The region map shown in Fig. 6-5 is generated from a symmetric TG switch. The region map shown in Fig. 6-5, however, is general and is applicable for both symmetric and non-symmetric TG switches.

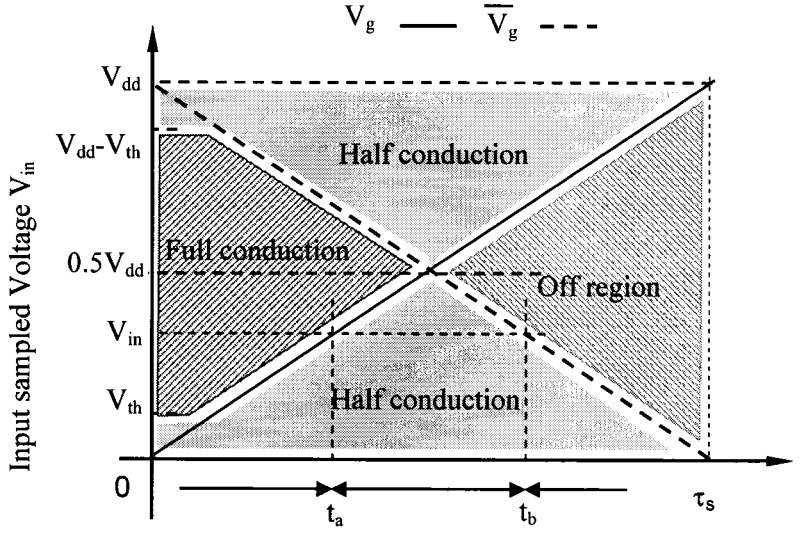


Figure 6-5: Region map when turning off the TG switch ($W_n = W_p$, and $L_n = L_p$, and $V_{TN} = |V_{TP}| = V_{th}$)

6.2. Clock Feedthrough in the Full Conduction Region

As shown in Fig. 6-4, seven currents flow in a TG switch during the switch off process. IL is the current sourcing or sinking capacitor CL, IDN and IDP are the NMOS and PMOS drain currents, respectively, and In and Ip are the coupling currents flowing through the MOS transistor gate-to-drain overlap capacitors. Icoxp and Icoxn are the coupling currents flowing through the gate capacitors. During the full conduction region, all seven currents exist. From the current conservation law applied at the output node of Fig. 6-4, a system equation is obtained,

$$I_L = I_n + I_p - (I_{DN} - I_{coxn}) + (I_{DP} - I_{coxp}), \tag{6.6}$$

$$C_{Leff}\frac{dV_e}{dt} = -\frac{V_e}{R_{sw}} - \left(C_{gdn} - C_{gdp} + \frac{C_{oxn} + C_{oxp}}{2}\right)\cdot\frac{V_{dd}}{\tau_s} \quad , \tag{6.7}$$

where R_{sw} is the TG switch "on" resistance.

$$\frac{1}{R_{sw}} = \frac{1}{R_N} + \frac{1}{R_P} = k_n \cdot \left(V_G - V_{in} - V_{TN}\right) - \left|k_p\right| \cdot \left(V_{in} - \left|V_{TP}\right| - V_G\right) \quad , \tag{6.8}$$

$$C_{Leff} = C_L + C_{gdn} + C_{gdp} \quad , \tag{6.9}$$

$$A_1 = \frac{k_n V_{dd} - \left(k_n + \left|k_p\right|\right) \cdot V_{in} - k_n V_{TN} + \left|k_p\right| \cdot \left|V_{TP}\right|}{k_n - \left|k_p\right|} \quad , \tag{6.10}$$

$$k_n = \mu_n C_{oxN} \left(W/L\right)_N \quad , \tag{6.11}$$

$$\left|k_p\right| = \mu_p C_{oxP} \left(W/L\right)_P \quad , \tag{6.12}$$

where kn, kp, V_{TN}, V_{TP}, $(W/L)_N$, and $(W/L)_P$ are the current factor, threshold voltage, and the width/length ratio of the NMOS and PMOS transistors, respectively.

An expression for the error voltage on the hold capacitor CL during the full conduction region is solved from the differential equation characterized by (6.7) and is

$$V_{el}(t) = -\sqrt{\frac{\pi V_{dd} C_{Leff}}{2\tau_s (k_n - \left|k_p\right|)}} \cdot \left(\frac{2C_{gdn} - 2C_{gdp} + C_{oxN} - C_{oxP}}{2C_{Leff}} \right) \cdot \exp\left\{ \frac{(k_n - \left|k_p\right|)V_{dd}}{2\tau_s C_{Leff}} \left(t - \frac{A_1 \tau_s}{V_{dd}} \right)^2 \right\}$$

$$\cdot \left\{ erf\left[\sqrt{\frac{\tau_s (k_n - \left|k_p\right|)}{2V_{dd} C_{Leff}}} \cdot A_1 \right] - erf\left[\sqrt{\frac{\tau_s (k_n - \left|k_p\right|)}{2V_{dd} C_{Leff}}} \cdot \left(A_1 - \frac{V_{dd}}{\tau_s} \cdot t \right) \right] \right\} \quad . \tag{6.13}$$

The error voltage generated during the full conduction region as shown in (6.13) is a function of the input voltage, gate voltage transition time, S/H capacitance, and the size of the MOSFET transistors. The resulting clock feedthrough error is graphically depicted in Fig. 6-6. The error voltage generated by clock feedthrough within the TG switch during the full conduction region is due to coupling of the gate voltages through Coxn, Coxp, Cgdn, and Cgdp. Coupling from the gate capacitors of the NMOS and PMOS transistors has opposite polarity which compensate each other. The same phenomenon occurs in coupling from the overlap capacitor. Equation (6.13) also shows that clock feedthrough in the full conduction region is zero if Coxn equals Coxp and Cgdn equals Cgdp. Due to current cancellation in the two noise generating pairs, clock feedthrough during the full conduction region is small. Clock feedthrough in the full conduction region is determined from (6.13). These results are illustrated in Fig. 6-6. The three-dimensional characteristics of clock feedthrough in the full conduction region can be explained based on the region map described in the previous section.

When the input voltage is below Vth, the PMOS transistor is off. Full conduction does not occur (the TG switch is in the half conduction region) and the error voltage in full conduction is zero as shown in Fig. 6-6.

Once Vin exceeds the NMOS threshold voltage Vth, the TG switch enters the full conduction region. Increasing the input voltage, the TG switch resistance RSW increases, and less MOS current is supplied to compensate the coupling error

voltage. Because the MOSFETs are equally sized, the coupling currents from the gate capacitors are completely canceled. Only coupling through the gate-to-drain overlap capacitors generate noise. Capacitive coupling between Cgd and CL is larger due to a smaller gate voltage at the end of the full conduction region. The error, therefore, increases with higher input voltage. As shown in the region map, when the input voltage increases above Vth, the length of time in the full conduction region becomes wider. The clock feedthrough noise generated in this region therefore increases (clock feedthrough noise in any region is proportional to the length of time the switch remains in that region) [see Fig. 6-5, (6.4), and (6.5)].

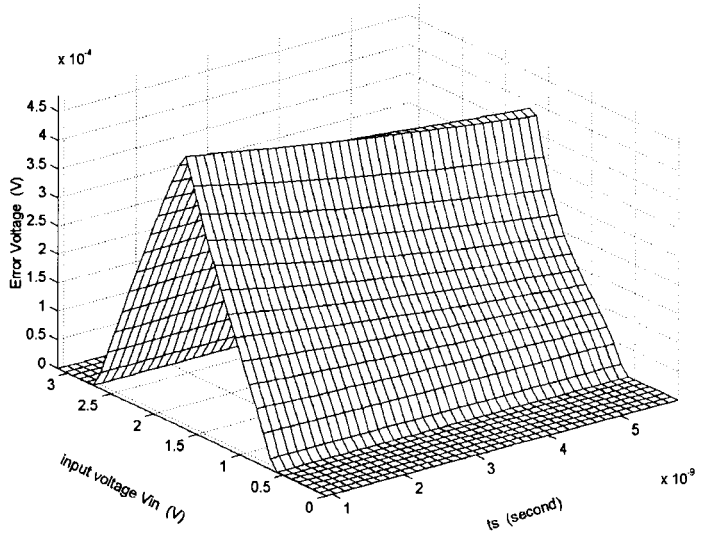


Figure 6-6: Clock feedthrough error of an analog TG switch generated during the full conduction region ($W_n = W_p = 10$ μm, $L_n = L_p = 0.35$ μm, $k_n = 40$ mA/V^2, $|k_P| = 10$ mA/V^2, $C_L = 1$ pF, and $C_{OXN} = C_{OXP} = 3$ fF/μm^2)

When the input voltage is approximately half the power supply voltage (assuming $V_{TN} = |V_{TP}|$ and kn = kp), the switch resistance RSW is greatest, the full conduction region is widest (Fig. 6-5), and the error voltage on the capacitor CL reaches a maximum. The region map shows that the length of time the TG switch is in this region reaches a maximum when the input voltage is at half of the power supply voltage. As described by the region map, the noise generated in the full conduction region is maximum.

As shown in Fig. 6-5, the width of the full conduction region decreases as the input signal increases toward Vdd from half of the power supply voltage. The error voltage, therefore, decreases with increasing input voltage due to weaker capacitive coupling and a larger MOSFET current flowing through the switch. A slower gate ramp voltage (larger τs in Fig. 5) permits the transistor to source current for a longer time, thereby compensating the error on the load capacitor CL, resulting in a smaller error voltage. The region map shows the decreasing length of the full conduction region. The clock feedthrough noise decreases. The TG switch exits the full conduction region when the input voltage passes Vdd – Vth (the NMOS transistor is off) and the clock feedthrough noise returns to zero.

6.3. Half Conduction

In the half conduction region, one transistor operates in the linear region while the other transistor is off. The duration of the half conduction region is $|tb - ta|$, as

shown in Fig. 6-5. The clock feedthrough noise generated during the half conduction region is directly proportional to the time within the region $|tb - ta|$. Clock feedthrough in this region is due to coupling through the gate capacitor of the conducting MOSFET and coupling from the overlap capacitors of both of the MOSFETs. As in the full conduction region, the drain current of the conducting MOSFET compensates the coupling error. The current in the off transistor is much smaller and is therefore ignored. In the half conduction region, one noise generating current in the gate current pair is zero so that current compensation in this current pair does not exist. The noise generated in this region is therefore higher. The other current pair generating noise is due to the overlap capacitors of both of the NMOS and PMOS transistors which contribute to the error voltage.

Two cases can exist during the half conduction region. With one case, the NMOS transistor conducts and the PMOS transistor is off. In the other case, the PMOS transistor conducts and the NMOS transistor is off. The first case shown in the region map is defined as zone A of the half conduction region, and the second case is defined as zone B of the half conduction region. Depending upon the input sampled voltage level, the TG switch operates in one of the two zones during the half conduction region. The clock feedthrough noise voltage generated in Zone A is negative, and is positive in zone B. The PMOS transistor is off within zone A.

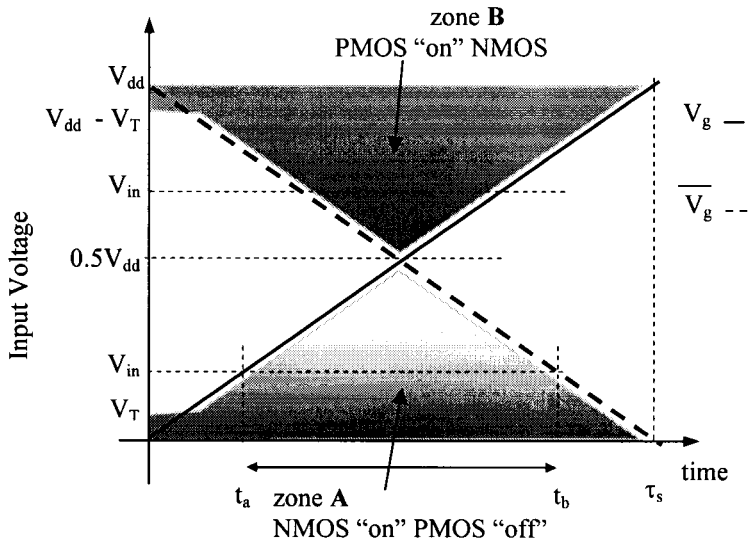


Figure 6-7: Zones in the half conduction region for a symmetric TG switch (V_{TN} = $|V_{TP}| = V_{th}$, $W_n = W_p$, and $L_n = L_p$)

The PMOS drain current I_{DP} and coupling current I_{coxp} shown in Fig. 6-4 are zero. The error voltage in the half conduction region is obtained by solving the differential equations, (6.7) and (6.8). The clock feedthrough noise in zone A is

$$V_{e2}(t) = -\beta_N \cdot f_N(t) + V_{e1}(t_a) \quad , \quad t_a < t < t_b \quad , \tag{6.14}$$

where Ve1(ta) is the error voltage generated during the full conduction region and determined from (6.13),

$$\beta_N = \sqrt{\frac{\pi V_{dd} C_{Leff}}{2\tau_s k_n}} \cdot \left(C_{gdn} - C_{gdp} + \frac{C_{oxN}}{2} \right) \Big/ C_{Leff} , \tag{6.15}$$

and

$$f_N(t) = \exp\left\{\frac{k_n \cdot V_{dd}}{2\tau_s C_{Leff}}\left(t - t_a - \frac{V_{dd} - V_{in} - V_{TN}}{V_{dd}} \cdot \tau_s\right)^2\right\} \cdot \left\{erf\left[\sqrt{\frac{k_n \cdot \tau_s}{2V_{dd}C_{Leff}}} \cdot \left(V_{dd} - V_{in} - V_{TN}\right)\right]\right.$$

$$\left. - erf\left[\sqrt{\frac{k_n \cdot \tau_s}{2V_{dd}C_{Leff}}} \cdot \left(V_{dd} - V_{in} - V_{TN} - \frac{V_{dd}}{\tau_s}t\right)\right]\right\} \quad . \tag{6.16}$$

For those input voltage levels that maintain the TG switch within zone B during the half conduction region, the NMOS transistor is off so that kn and Coxn can be removed from the system equation, (6.7). Solving (6.7) and (6.8), the clock feedthrough noise generated in zone B is

$$V_{e2}(t) = -\beta_P \cdot f_P(t) + V_{e1}(t_b) \quad , \quad t_a < t < t_b \, , \tag{6.17}$$

$$\beta_P = -\sqrt{\frac{\pi V_{dd} C_{Leff}}{2\tau_s |k_p|}} \cdot \left(C_{gdn} - C_{gdp} + \frac{C_{oxP}}{2}\right) \Big/ C_{Leff} \quad , \tag{6.18}$$

and

$$f_P(t) = \exp\left\{\frac{|k_p| \cdot V_{dd}}{2\tau_s C_{Leff}}\left(t - t_b - \frac{V_{in} - |V_{TP}|}{V_{dd}} \cdot \tau_s\right)^2\right\} \cdot \left\{erf\left[\sqrt{\frac{|k_p| \cdot \tau_s}{2V_{dd}C_{Leff}}} \cdot \left(V_{in} - |V_{TP}|\right)\right]\right.$$

$$\left. - erf\left[\sqrt{\frac{|k_p| \cdot \tau_s}{2V_{dd}C_{Leff}}} \cdot \left(V_{in} - |V_{TP}| - \frac{V_{dd}}{\tau_s}t\right)\right]\right\} \quad . \tag{6.19}$$

The clock feedthrough error generated during zones A and B are determined from (6.14) and (6.17) [without the term $V_{el}(t_a)$] and illustrated in Fig. 6-8. The error waveform illustrated in Fig. 8 can be explained from the zone map shown in Fig. 6-7. When the input signal voltage ranges from 0 to V_{th}, the TG switch operates in the half conduction zone A. Due to coupling between the NMOS gate capacitor and the S/H capacitor, the total clock feedthrough error is negative (see Fig. 8). The length of time $(t_b - t_a)$ is a maximum.

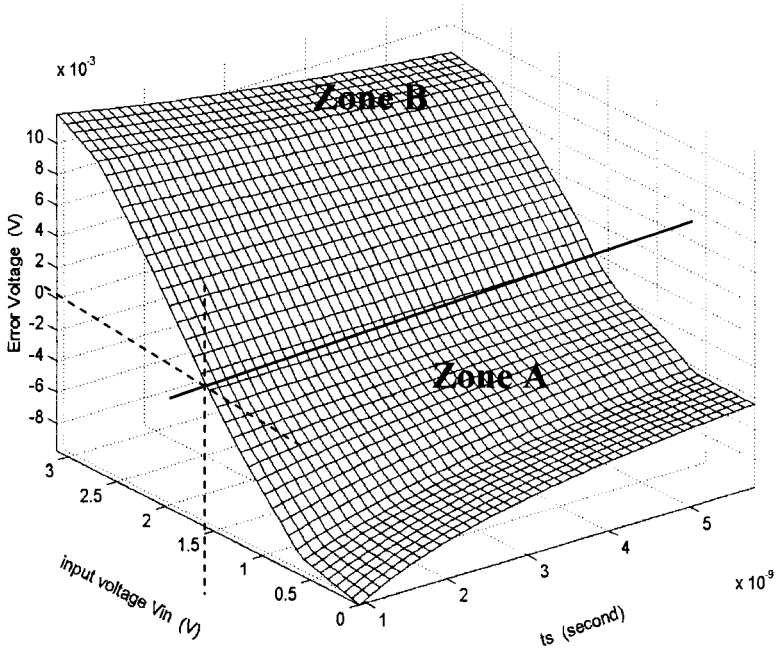


Figure 6-8: Clock feedthrough error of a TG switch during the half conduction region (V_{dd} = 3.3 volts, $W_n = W_p$, and $L_n = L_p$)

Increasing the input voltage from $V_{DD}/2$, assuming $V_{TN} = V_{TP}$, the TG switches into zone B. Clock feedthrough is primarily caused by coupling of the gate voltage between the PMOS transistor gate capacitor C_{OXP} and the S/H capacitor C_L. The clock feedthrough voltage becomes positive (see Fig. 6-7). A larger input voltage makes the TG switch remain in zone B longer (see Fig. 6-7). The error voltage, therefore, increases with a larger input signal when the input voltage is greater than $V_{DD}/2$, as shown in Fig. 6-8.

When the input voltage level reaches $V_{dd} - V_{th}$, the length of time $t_b - t_a$ increases at half the speed as compared to when the input voltage is between $V_{dd}/2$ and $V_{dd}/2 - V_{th}$. The clock feedthrough noise voltage increases slowly with increasing input voltage.

Increasing the ramp constant τ_s provides a longer time for the MOS transistor drain current to compensate the coupling error voltage on C_L. The error is smaller for larger τ_s. Comparing Fig. 6-8 with Fig. 6-6, the clock feedthrough noise generated in the half conduction region is much larger than the clock feedthrough noise generated in the full conduction region. Ensuring that the TG switch operates in the half conduction region for a short amount of time is important for reducing the clock feedthrough noise voltage. Level shifting the input voltage to approximately half of the power supply voltage will therefore minimize clock feedthrough noise in a TG switch.

6.4. Subthreshold/Cutoff Region

The error voltage generated in the subthreshold/cutoff region is due to coupling of the gate voltage through the gate-to-drain overlap capacitors C_{gd} of the two transistors to the S/H (load) capacitor C_L. Because both of the NMOS and PMOS transistors are off, there is no channel generated under the gates.

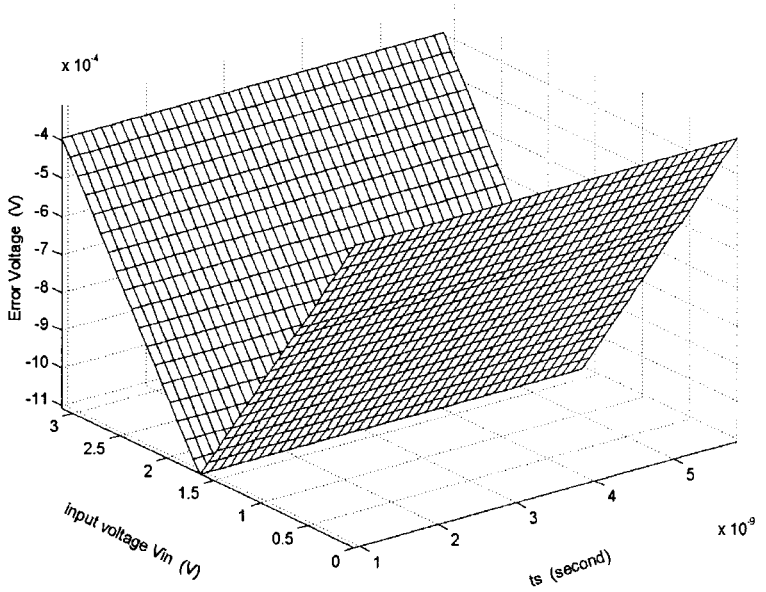


Figure 6-9: Clock feedthrough error of a TG switch during the subthreshold/cutoff region (V_{dd} = 3.3 volts, $W_n = W_p$, and $L_n = L_p$)

The channel resistance in the proposed clock feedthrough model is very large, therefore, the noise generating current pair, the gate capacitor coupling currents I_{coxn} and I_{coxp}, can be ignored. The subthreshold currents in the NMOS and PMOS

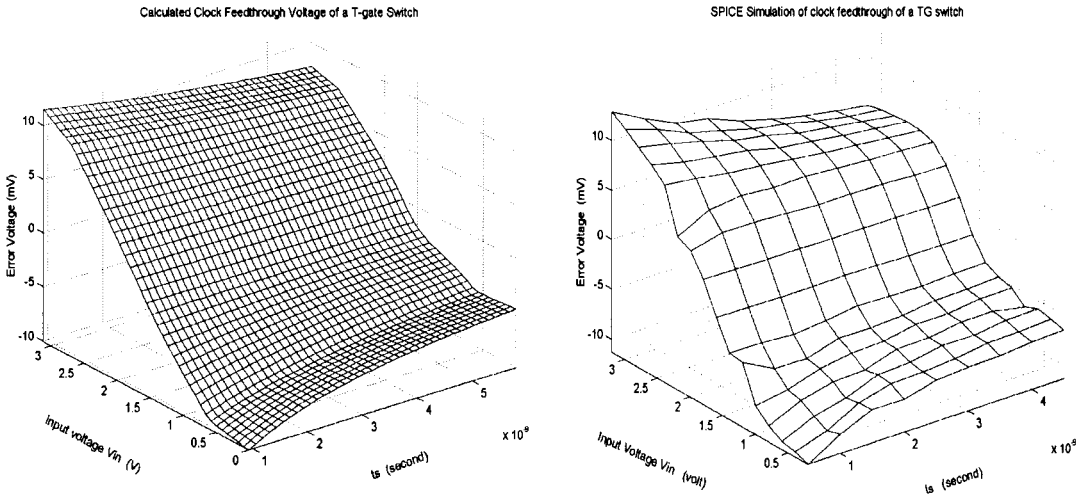
transistors are on the order of 10^{-15} to 10^{-17} A/μm and are therefore ignored. Due to the low charge density as compared to the charge density of the induced channel, currents from discharging the PMOS and NMOS transistor depletion layers can also be ignored. The clock feedthrough noise generated in the subthreshold/cutoff region (for symmetric TG switches) is therefore negligible.

The clock feedthrough voltage generated during the subthreshold/cutoff region is shown in Fig. 6-9. The three-dimensional curve can also be explained by the region map. As shown in Fig. 6-9, clock feedthrough during the subthreshold/cutoff region is small as compared to the clock feedthrough noise generated in the half conduction region. The region map shown in Fig. 6-5 describes, for a symmetric TG switch, the shape of the subthreshold/cutoff region which is symmetric to the full conduction region. The clock feedthrough noise voltage generated in the subthreshold/cutoff region is therefore a mirror image of the clock feedthrough noise generated in the full conduction region, as shown in Figs. 6-6 and 6-9, except during the time when the sampled input voltages are near the ground and power supply voltages.

6.5. Simulation Results

Based on the physical mechanisms described in the previous sections, clock feedthrough in a TG switch is shown in Fig. 6-10 to be a function of the transistor size, load capacitor, input voltage, and the gate voltage time constant τ_s. The total

clock feedthrough is the sum of the error voltage generated in the three regions during the time required to turn off the transistors. From an analysis of clock feedthrough for a symmetric TG switch (the NMOS and PMOS transistors have the same geometric dimensions and threshold voltages), the clock feedthrough error generated in the half conduction region is shown to be dominant. A SPICE simulation of clock feedthrough within the same TG switch is illustrated in Fig. 6-10b.



(a) (b)

Figure 6-10: Clock feedthrough voltage of a TG switch a) analytically determined, b) SPICE simulation (V_{dd} = 3.3 volts, $V_{TN} = |V_{TP}| = 0.6$ volts, $W_n = W_p = 10$ μm, $L_N = L_P = 0.35$ μm, $k_n = 40$ mA/V^2, $|k_P| = 10$ mA/V^2, $C_L = 1$ pF, and $C_{OXN} = C_{OXP} = 3$ fF/μm^2)

As shown in Figs. 10a and 10b, results from the proposed model and SPICE simulation are in close agreement. The error from the proposed model is less than 3% for most of the sampled voltages as compared to SPICE simulations, and the error is less than about 9% when the sampled input voltage is near the power supply voltage.

6.6. Conclusions

Clock feedthrough in a TG switch is due to coupling of the gate voltage between the MOSFET overlap capacitors Cgd and the gate capacitors COX and the S/H capacitor CL. The MOSFETs in a TG switch supply currents that compensate the coupling error on an S/H load capacitor. A region map of the TG switch during switch off can be used to efficiently estimate the clock feedthrough noise. For a specific input voltage, the polarity and relative magnitude of the clock feedthrough noise can also be determined. For a symmetric TG switch, the input sampled voltage is chosen to be around half of the power supply in order to minimize clock feedthrough noise. This choice of bias condition can significantly reduce clock feedthrough noise. The input sampled voltages can also be shifted to make the clock feedthrough noise always positive or negative which is preferable to other noise reduction techniques. In a TG switch, clock feedthrough generated during the half conduction region causes most of the error on the S/H capacitor. Clock feedthrough during the subthreshold/cutoff region is small and can be ignored. A

slower gate input voltage signal provides a longer time for the MOSFET currents to compensate the coupling voltage, thereby reducing the clock feedthrough voltage error. An error of less than 3% is noted in the analytic expressions as compared to SPICE simulations.

Chapter Seven: Charge Sharing Effect (CSE) in CMOS Switched Capacitor Sample-and-Hold Circuits

CMOS switched capacitor circuits are widely used in analog signal processing, data conversion, signal filtering, speech recognition, and many analog and mixed-signal integrated circuits [84], [89], [90]. As analog ICs continue to improve in speed and resolution, increasing demands are placed on the performance of high speed S/H circuits. In many applications, such as data acquisition and conversion, the throughput and accuracy are often limited by the speed and precision at which the input can be sampled and held.

Noise in switched capacitor (SC) circuits is a major problem in many practical applications. Many papers have reported on CMOS switched capacitor circuit noise issues [64], [91]-[94], [95]-[98]. Most of these papers concentrate on common noise sources such as interconnect coupling [92], clock feed-through noise [93], [94], power supply/substrate coupling [64], and process related noise [95]-[97]. However, charge-sharing effect (CSE) noise in switched-capacitor S/H circuits has to date not been reported. CSE noise in certain applications is large and can be a dominant noise source. CSE noise results in gain error and introduces nonlinearities

that distort the circuit output. Charge-share-effect noise in SC sample-and-hold circuits will be discussed in this chapter. It is demonstrated here that the charge-share effect depends on the circuit implementation and is input signal dependent. Since the charge-sharing effect is input signal related, it is difficult to compensate for this error using self-calibration techniques such as correlated double sampling.

The charge sharing effect in switched capacitor S/H (sample-and-hold) circuits is discussed in the following sections. Based on the analysis, the charge sharing effect introduces an input signal dependent error at the S/H circuit output. Depending upon the S/H circuit architecture and application, CSE can be the primary noise source in switched capacitor S/H circuits. The charge sharing effect in S/H circuits greatly affects the proper selection of the circuit architecture and optimization of the system performance. In section 7-1, various sample-and-hold architectures are reviewed. The charge-share effect concept and mechanism are described in section 7-2. CSE noise in S/H circuits is analyzed in section 7-3. An analysis of CSE noise is presented in section 7-4. Some conclusions are provided in section 7-5.

7.1. Sample-and-Hold Circuit Design

Two basic circuit configurations are commonly used to implement monolithic S/H circuits, open loop and closed loop topologies, as shown in Figs. 7-1 and 7-2, respectively. The open loop architecture offers potentially the fastest

implementation of the sampling function [99], [100]. Two open loop S/H circuits are shown in Fig. 7-1. In the simplest form (see Fig. 7-1a), an open loop sample-and-hold circuit consists of a switch, a capacitor Csh, and a high input impedance unity-gain amplifier. Capacitor Cp, as shown in Figs. 7-1a and 7-1b, is the parasitic capacitor at the amplifier input. During the sampling phase, switch S1 is closed and the input voltage is sampled onto the S/H capacitor Csh. In many practical applications, the S/H capacitor Csh is separated from the buffering section by a switch S2 such that the amplifier noise can be compensated (or other operations can be accomplished while the input is being sampled). One such circuit is illustrated in Fig. 7-1b.

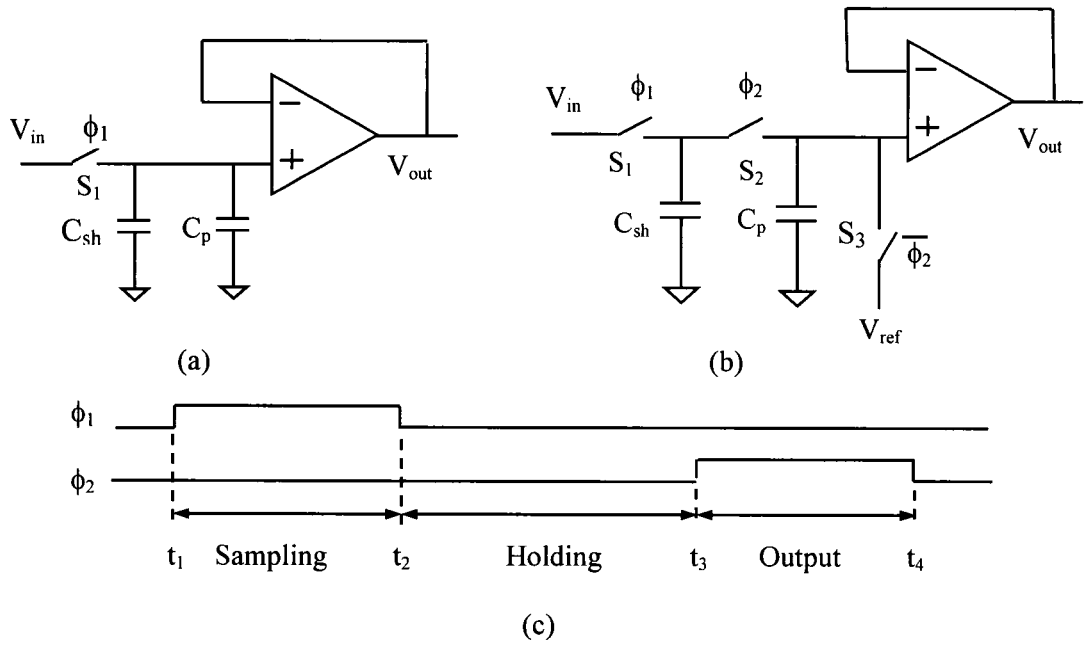


Figure 7-1: S/H circuit, a) an open loop architecture, b) a different open loop architecture with amplifier offset compensation, c) typical timing of a S/H circuit

During the sampling phase, switches S1 and S3 are closed and S2 is open. The analog input signal is sampled onto the S/H capacitor Csh while the amplifier output is set equal to Vref + Δ where Δ is the lumped amplifier error voltage including the offset voltage. The sampled/held signal is available only between t3 and t4, as shown in Fig. 7-1c.

Closed-loop architectures avoid charge injection or clock feedthrough during turn-off of the sampling switch S_1 [99]. One such configuration is shown in Fig. 7-2. In this circuit, the sampling switch is always at virtual ground during the sampling phase. This connection ensures that the charge injection is independent of the input signal so that the error due to the clock feedthrough from S_1 can be easily removed. The disadvantages of the closed loop sample-and-hold architectures typically include lower speed, limited bandwidth, and increased design complexity. The charge sharing effect in closed-loop sample-and-hold circuits is not further discussed in this chapter.

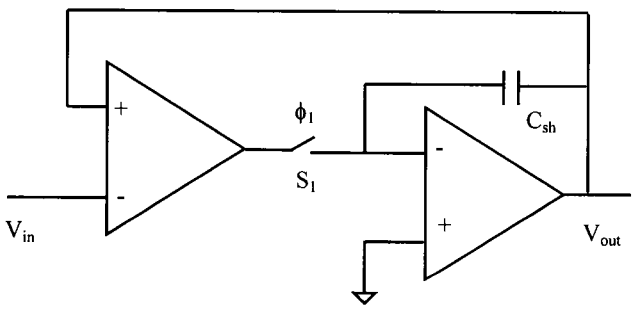


Figure 7-2: Closed-loop sample-and-hold circuit architecture

7.2. Charge Sharing Effect (CSE)

The concept of charge redistribution [109] (or the charge conservation principle) is commonly used in CMOS switched capacitor circuit design and analysis. Due to parasitic capacitors, an error voltage is generated after the charge is redistributed. The charge sharing effect is a phenomenon where charge is placed on the parasitic capacitors when a capacitor network with parasitic capacitors is reconnected to the OPAMP. When the network is reconnected to the OPAMP, the capacitor network does not have any source to charge pump in or out such that the total amount of charge in the network is conserved.

As shown in Fig. 7-1b, a S/H circuit consists of the S/H capacitor Csh, the lumped parasitic capacitor Cp, and the amplifier input capacitors. Each of these capacitors holds a different amount of charge after the sampling phase is completed. Once the output phase starts, the charge is redistributed onto these capacitors, causing an error voltage to be produced at the S/H circuit output due to the parasitic capacitors. The total charge in the sample/hold capacitor network remains unchanged after the charge redistribution is completed. A general open loop S/H circuit with parasitic components which is used for analyzing the charge sharing effect is shown in Fig. 7-3. In Fig. 7-3, Ci is the input capacitor of the amplifier, Vref is a DC reference voltage, and ri is the OPAMP input resistance. The charge sharing effect occurs when the circuit changes from the hold phase to

the output phase. The charge in the sampling phase (t = t2, see Fig. 7-1) and the output phase (t = t3) is

$$Q[t_2] = (v_{in}[t_2] - V_{ref}) \cdot C_{sh} + v_{i+}[t_2] \cdot C_p + (v_{i+}[t_2] - v_{i-}[t_2]) \cdot C_i, \qquad (7.1)$$

$$Q[t_3] = (v_x[t_3] - V_{ref}) \cdot C_{sh} + v_x[t_3] \cdot C_p + (v_x[t_3] - v_{i-}[t_3]) \cdot C_i. \qquad (7.2)$$

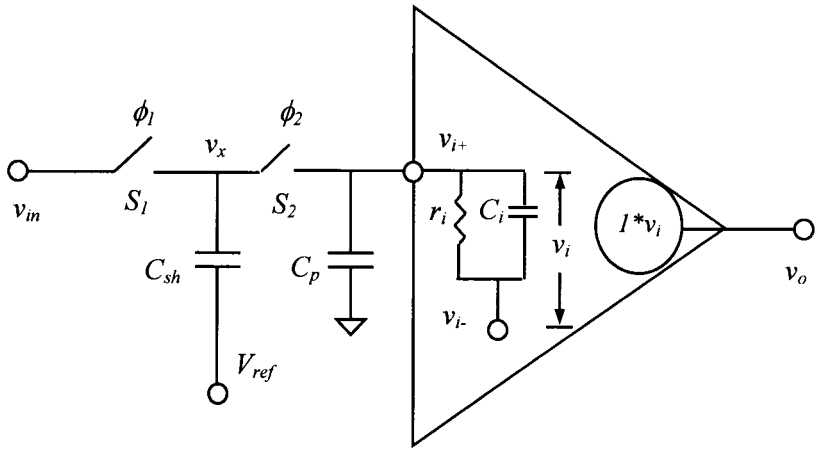


Figure 7-3: A general open-loop CMOS switched capacitor S/H circuit

No additional charge is added to the capacitor network, therefore, Q[t2] is equal to Q[t3]. The S/H circuit output voltage during the output phase can be obtained from (7.1) and (7.2),

$$v_x[t_3] = v_{in}[t_2] + \frac{(C_p + C_i) \cdot v_{i+}[t_2] + C_i \cdot (v_{i-}[t_3] - v_{i-}[t_2]) - (C_p + C_i) \cdot v_{in}[t_2]}{C_{sh} + C_p + C_i}. \qquad (7.3)$$

The second term in (7-3) is the error voltage due to the charge sharing effect. Equation (7-3) shows that, for an open loop S/H circuit, the charge sharing effect noise voltage is a function of the sampled input signal voltage vin, the S/H capacitor Csh, the parasitic capacitor Cp, and the voltage change across the OPAMP input capacitance Ci. Generally, charge sharing effect noise is inversely proportional to the S/H capacitance Csh. Increasing Csh is an effective way to reduce the charge sharing noise.

7.3. Charge-Sharing Noise in CMOS Switched Capacitor S/H Circuits

CMOS OPAMPs have a high input impedance and good linearity. Therefore, these circuits are usually used as a buffer in switched capacitor S/H circuits. The CMOS OPAMP, however, has a nonzero input capacitance such that the charge sharing effect affects the performance of the CMOS S/H circuits. The charge-share effect in CMOS S/H circuits in which the OPAMP input and parasitic capacitances are considered is discussed in the following sub-sections.

In many CMOS open loop S/H circuits, the OPAMP has a unity gain configuration (see Fig. 7-1). The output voltage during the output phase equals the sampled input voltage and the offset voltage,

$$v_o[t_3] = v_{in}[t_2] + V_{offset} \quad . \tag{7.4}$$

The operation of a S/H circuit as shown in Fig. 7-1b is as follow. The input signal is first sampled onto capacitor Csh by closing switches S1 and S3 while leaving switch S2 open during the sampling phase. After the sampling phase, S1 and S2 are open and S3 remains closed. The S/H circuit output is held to the reference voltage Vref. During the output phase, switch S2 is closed and switches S1 and S3 are open. To accurately analyze the charge sharing effect, the buffer input capacitance, as shown in Fig. 7-1b, should also be considered. A portion of a typical CMOS OPAMP input stage is shown in Fig. 7-4. M1 and M2 make up the input differential pair, M5 supplies the bias current Io, and M3 and M4 are the active loads of M1 and M2, respectively. All of the transistors operate in the saturation region.

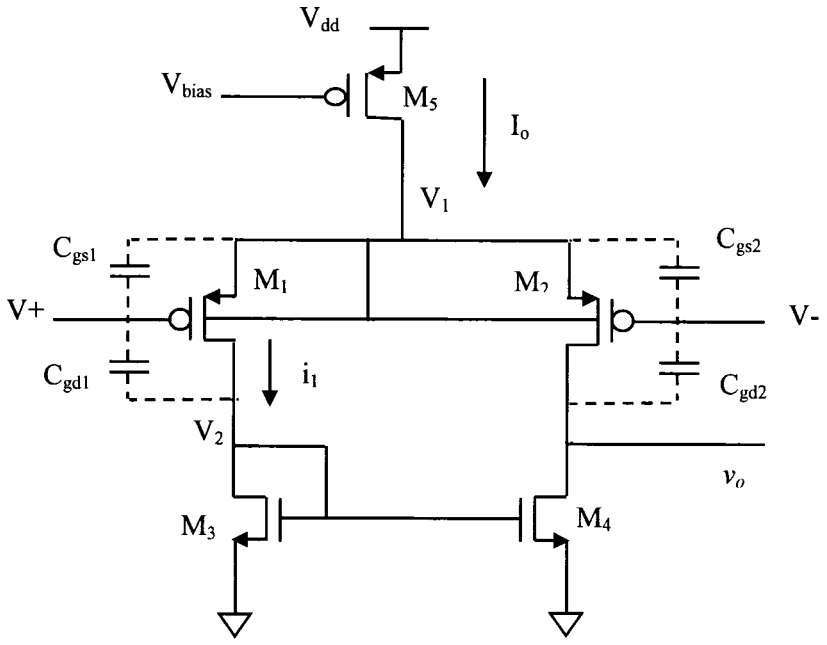


Figure 7-4: A typicalinput stage of a CMOS OPAMP

When used as a buffer in an open loop S/H circuit, the input capacitors of the amplifier are part of the charge redistribution process,

$$C_{gd1} = C_{GD1} \quad , \tag{7.5}$$

$$C_{gs1} \approx C_{GD1} + \frac{2}{3} C_{OX1} \quad . \tag{7.6}$$

Ignoring clock feedthrough and the leakage current, the total charge stored by capacitors Csh, Cp, C_{DG}, and C_{ox1} at the end of the sampling phase (t = t_2) is conserved during the output phase. The total charge in the S/H circuit shown in Fig. 7-1b during the sampling phase and the output phase is equal and can be expressed as

$$Q(t_2) = V_{in}[t_2] \cdot C_{sh} + V_{ref} \cdot C_p + \left(V_{ref} - V_2[t_2]\right) \cdot C_{GD1} + \left(V_{ref} - V_1[t_2]\right) \cdot \left(\frac{2}{3} \cdot C_{ox1} + C_{GD1}\right), \tag{7.7}$$

$$Q(t_3) = V_o[t_3] \cdot C_{sh} + V_o[t_3] \cdot C_p + \left(V_o[t_3] - V_2[t_3]\right) \cdot C_{GD1} + \left(V_o[t_3] - V_1[t_3]\right) \cdot \left(\frac{2}{3} \cdot C_{ox1} + C_{GD1}\right), \tag{7.8}$$

where V1[t] and V2[t] are the node voltages at the amplifier input stage, as shown in Fig. 7-4. From (7.7) and (7.8), the output voltage of the S/H circuit shown in Fig. 7-1b is

$$V_o(t_3) = V_{in}[t_2] + \beta_1 \cdot \left(V_{ref} - V_{in}[t_2]\right) + \beta_2 \cdot \Delta V_1 + \beta_3 \cdot \Delta V_2 \quad , \tag{7.9}$$

where C_T = Csh + Cp + $2C_{GD}1$ + 0.66Cox1, $\beta 1$ = Csh + $2C_{GD}1$ + 0.66Cox1)/C_T, $\beta 2$ = (C_{GD1} + 0.66Cox1)/C_T, and $\beta 3$ = $C_{GD}1/C_T$.

$$\Delta V_1 \approx V_o[t_3] - V_{ref} - \sqrt{\left(V_{ref} + |V_{tp}|\right)^2 + I_o / K_1} + \sqrt{\left(V_o[t_3] + |V_{tp}|\right)^2 + I_o / K_1} \quad , \qquad (7.10)$$

$$\Delta V_2 \approx 0 \quad , \qquad (7.11)$$

where Vref is the reference voltage, Io is the OPAMP bias current, and K1 and Vtp are the current factor and threshold voltage of transistor M1 (see Fig. 7-4), respectively.

For CMOS S/H circuits, $\beta 3$ is much smaller than $\beta 1$ and $\beta 2$. The internal node voltage V2 of the OPAMP shown in Fig. 7-4 changes little with the input voltages. The fourth term on the right side of (7-9) can, therefore, be ignored. Note in (7-9) that the noise voltage due to the charge sharing effect in the circuit shown in Fig. 7-1b is

$$V_{Error} \approx \frac{C_{sh} + 2C_{GD1} + 0.66C_{OX1}}{C_{sh} + C_p + 2C_{GD1} + 0.66C_{OX1}} \cdot \left(V_{ref} - V_{in}[t_2]\right) + \frac{C_{GD1} + 0.66C_{OX1}}{C_{sh} + C_p + 2C_{GD1} + 0.66C_{OX1}} \cdot \Delta V_1 . \qquad (7.12)$$

This analysis shows that the output error voltage of the S/H circuit shown in Fig. 7-1b due to the charge sharing effect is dependent on the sampled input signal. Charge sharing noise due to the parasitic capacitance of the amplifier cannot be ignored in amplifiers with a large input stage.

7.4. Results and Comparison with SPICE

An open loop S/H circuit, as shown in Fig. 7-3, is simulated with various parasitic capacitances connected to the buffer amplifier input. These simulated results are compared in the following subsections to the analytic results derived from (7-12). The comparisons are presented in subsection 7.5.1. Some charge sharing effect noise reduction techniques are suggested in subsection 7.5.2.

7.4.1. Comparison of the Analytic Results with SPICE

An analytic estimate of the charge sharing effect error voltages determined from (7-12) is compared with SPICE. These SPICE results and the analytic results from (7-12) are displayed in Fig. 7-5. Note that the SPICE simulation results are more input signal dependent than the analytic results. The errors range from 2.4% for a Cp of 320 fF to 18% for zero Cp. This difference is due to clock feedthrough from the switches shown in Fig. 7-1b.

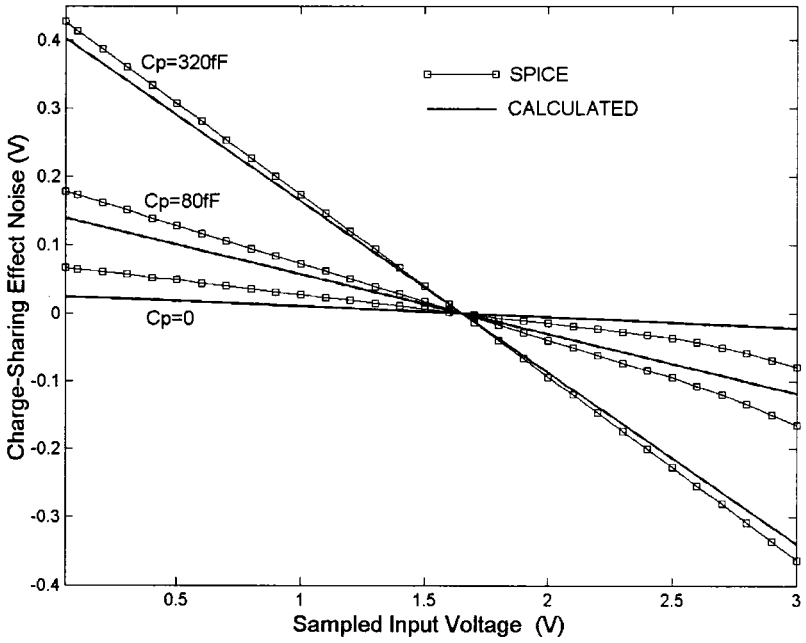


Figure 7-5: Charge share effect in a S/H circuit shown in Fig. 6-1b (C_{sh} = 1 pF, V_{ref} = 1.65 volts, V_{dd} = 3.3 volts, W_1/L_1 = 80 μm/0.4 μm, and I_O = 100 μA for the amplifier input stage)

As shown in Fig. 7-5, the difference between the simulated and analytic results increases as the parasitic capacitance Cp decreases. Based on the model established in Chapter 6, clock feedthrough injects charge onto the capacitor. Clock feedthrough is input signal dependent and is inversely proportional to the capacitance. For the same amount of injected charge, a smaller voltage change is generated across a larger capacitor. In Fig. 7-1b, clock feedthrough injects charges onto all of the capacitors during charge redistribution. A larger parasitic

capacitance Cp decreases the clock feedthrough error. The analytic results from (7-12) are, therefore, close to SPICE simulation results for the case of a large parasitic capacitance (an error of 2.4% for a large Cp and an error of 18% for zero Cp). As illustrated in Fig. 7-5, charge sharing effect noise is input voltage dependent. Due to this characteristic, removing or reducing charge-sharing effect noise is difficult. It is also shown in Fig. 7-5 that charge sharing effect noise can be as large as hundreds of millivolts for improperly designed S/H circuits. Such a large error voltage is not acceptable in most applications

7.4.2. Reduction of Charge Sharing Effect Noise

Depending on the S/H architecture, the charge sharing effect can generate an input signal dependent error at the S/H circuit output. In general, the most effective way to reduce this type of error is to increase the Csh/Cp ratio. The parasitic capacitance at the high impedance input of the amplifier, however, is large in certain applications. It is therefore often too costly to use a large Csh to reduce the charge sharing effect. For these applications, there are several ways to reduce the charge sharing effect.

A. Use a closed-loop S/H circuit architecture. The disadvantages are slower speed and higher design complexity.

B. Use the Miller effect to effectively increase the sample-and-hold capacitance. Such circuits are used in [101], [102], and [103] to reduce clock feedthrough and are discussed in Chapter 8. The disadvantage is greater design complexity

C. Pin the amplifier input node to a constant voltage. One such circuit is shown in Fig. 7-6.

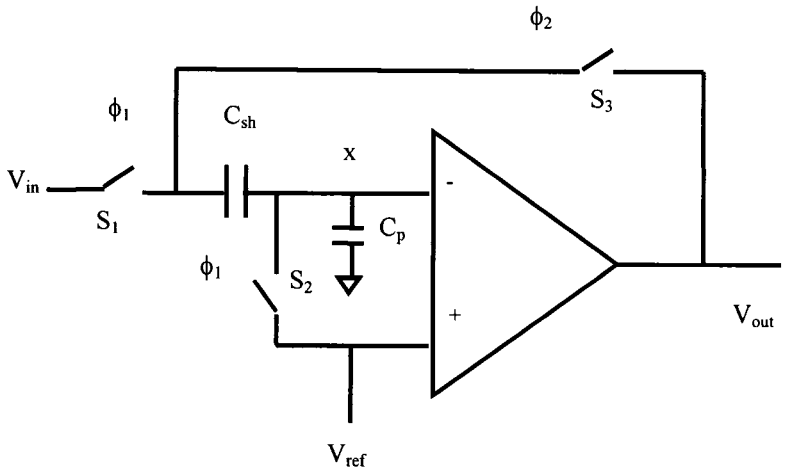


Figure 7-6: A fixed amplifier input voltage S/H circuit to reduce the charge sharing effect noise

7.5. Conclusions

The charge sharing effect (CSE) in switched capacitor S/H circuits has been introduced and discussed in this chapter. The charge sharing effect introduces an input signal dependent error voltage at the S/H circuit output which is difficult to compensate. Depending upon the architecture and application, the charge sharing

effect can generate as high as a few hundred millivolts of noise at the S/H output. Based on the results described in this chapter, charge sharing effect noise is analytically determined and compared with SPICE simulation results. Good agreement is found ranging from 2.4% error when the parasitic capacitance is large to 18% error when there is no parasitic capacitance. It is found that an increase in the Csh/Cp ratio is an effective technique to reduce charge sharing effect noise. Depending on the application, different techniques can be considered to minimize charge sharing effect noise. These techniques include a closed-loop type of S/H circuit architecture, the use of the Miller effect to increase the S/H capacitance, and pinning the amplifier input. The charge sharing effect should be evaluated during the S/H circuit design process so as to determine the circuit architecture and optimize system performance.

Chapter Eight: A CMOS Miller Hold Capacitance Sample-and-Hold Circuit to Reduce Charge Sharing Effect and Clock Feedthrough

A technique using Miller capacitance in the S/H (sample-and-hold) circuit is introduced in this chapter to reduce the charge sharing effect (CSE) due to the parasitic capacitance and clock feedthrough from a sampling switch. A compact cascode amplifier is used in the Miller feedback circuit. A ten times reduction in CSE and clock feedthrough is achieved. The S/H capacitor is split into two, Csh1 and Csh2, in the circuit. One of these S/H capacitors effectively reduces the CSE while the other capacitor reduces clock feedthrough.

CMOS switched capacitor S/H circuits are widely used in analog signal processing, data conversion, signal filtering, speech recognition, and many other analog and mixed-signal IC circuits [83], [105] and [106]. As analog ICs continue to improve in speed and resolution, increasing demands are placed on the performance of high speed S/H circuits. In many applications, such as data acquisition and conversion, the throughput and accuracy is often limited by the speed and precision at which the input is sampled and held.

Many noise sources [91], such as interconnect coupling [92], clock feedthrough [85] [87], power supply/substrate coupling [36] [107], charge sharing effects

(CSE), and process related noise exist in CMOS switched capacitor circuits. The CSE and switching noise result in gain error that introduces nonlinearities which distort the circuit output. Since the charge sharing effect and clock feedthrough are input signal related, it is difficult to compensate by using self-calibration techniques such as correlated double sampling (CDS). A Miller hold capacitor circuit is used in [99]-[102] to decrease switching noise. In this paper, a technique is presented that uses the Miller effect to effectively reduce the charge sharing effect and clock feedthrough in S/H circuits.

This chapter is organized as follow. In Section 8-1, the concept of the Miller effect and the charge share effect are briefly reviewed. The proposed Miller hold capacitor S/H circuit with reduced CSE noise is described in Section 8-2. Analytic results are discussed in Section 8-3. A comparison of these results with SPICE is presented in Section 8-4. Finally, some conclusions are provided in Section 8-5.

8.1. Miller Effect and Charge Sharing Effect

The Miller effect and the Charging Sharing effect are common effects in analog ICs. A brief review of these effects is presented in the following subsections.

8.1.1. Miller Effect

The Miller effect provides a mean for dealing with voltages at both ends of a capacitor changing at the same time, either independently or dependently. In certain

circuits, a larger capacitor can be used to represent the behavior at the terminal voltages. A general illustration of the Miller effect is shown in Fig. 8-1. The charge on capacitor C is,

$$\begin{aligned} Q &= C \cdot (V_+ - V_-) = C \cdot (\alpha_+ - \alpha_-) \cdot V_s(t) \\ &= C_M \cdot V_s(t) \quad , \end{aligned} \tag{8.1}$$

where CM is the Miller capacitance, Vs is the signal voltage, and α+(t) and α-(t) are the voltage gain at the two terminals of capacitor C, respectively.

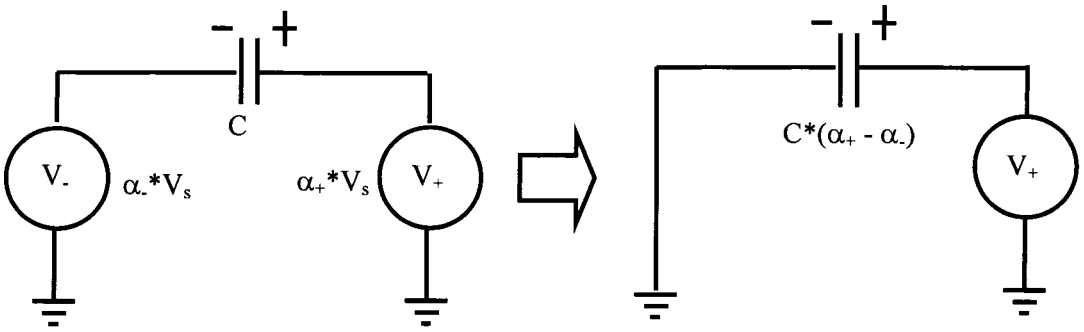


Figure 8-1: Diagram of principle describing Miller effect

In most applications, the coefficient α+(t) and α-(t) are constants, where α+(t) - α-(t) is much larger than one. A typical configuration of the Miller capacitance is shown in Fig. 8-2.

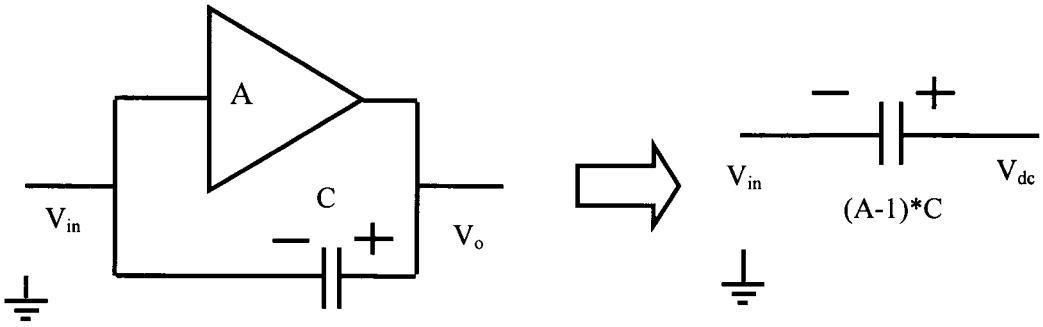


Figure 8-2: A typical Miller capacitor configuration

8.1.2. The Charge Sharing Effect

The charge sharing effect occurs when a capacitor network is reconnected. The charges are redistributed among the capacitors with the total charge conserved.

A capacitor network in a S/H circuit consists of a S/H capacitor Csh, a lumped parasitic capacitor Cp, and the amplifier input capacitors (see Fig. 7-3). Each of these capacitors stores a different amount of charge after the sampling phase. Once the output phase begins, these charges are redistributed within the capacitor network, causing a voltage error at the output of the S/H circuit. The voltage at the output of the S/H capacitor Csh during the output phase is

$$v_x[t_{out}] = v_{in}[t_{hold}] + \frac{C_p \cdot (v_{i+}[t_{hold}] - v_{in}[t_{hold}])}{C_{sh} + C_p + C_i} + \frac{C_i \cdot (v_{i+}[t_{hold}] + v_{i-}[t_{out}] - v_{i-}[t_{hold}] - v_{in}[t_{hold}])}{C_{sh} + C_p + C_i}. \quad (8.2)$$

The second and third terms in (8.2) represent the error voltage due to the charge sharing effect. For different circuit configurations the CSE noise has a different

expression. In general, the CSE is input signal dependent and inversely proportional to the S/H capacitance Csh. Increasing Csh is an effective way to reduce the charge sharing noise.

8.2. A Miller Hold Capacitor Circuit for Reducing CSE Reduction and Clock Feedthrough

In the presence of a parasitic capacitance Cp, a high gain Miller feedback amplifier is required to effectively reduce the charge sharing effect noise. A large gain of the Miller feedback amplifier is also desirable for reducing the dependence of clock feedthrough on the input signal. A typical open-loop S/H circuit is used as an example and shown in Fig. 7-1b.

In [102], a simple inverter (see Fig. 8-3b) is used as the Miller feedback amplifier to improve the switching noise. The large size inverter, however, has a large input capacitance CI that decreases the reduction in CSE and clock feedthrough. In the proposed Miller hold capacitor S/H circuit, a cascode inverter amplifier (Fig. 8-3c) is used to minimize the amplifier input capacitance CI and increase the gain.

For the cascode inverting amplifier shown in Fig. 8-3c, the input transistors M5, and M6 are designed with small width and minimum length. The gain is achieved by the large size of the cascode transistors M5a, and M6a. The gain of the simple

and cascode inverting amplifiers are characterized by (8-3) and (8-4). The simulation results are illustrated and compared in Fig. 8-3a.

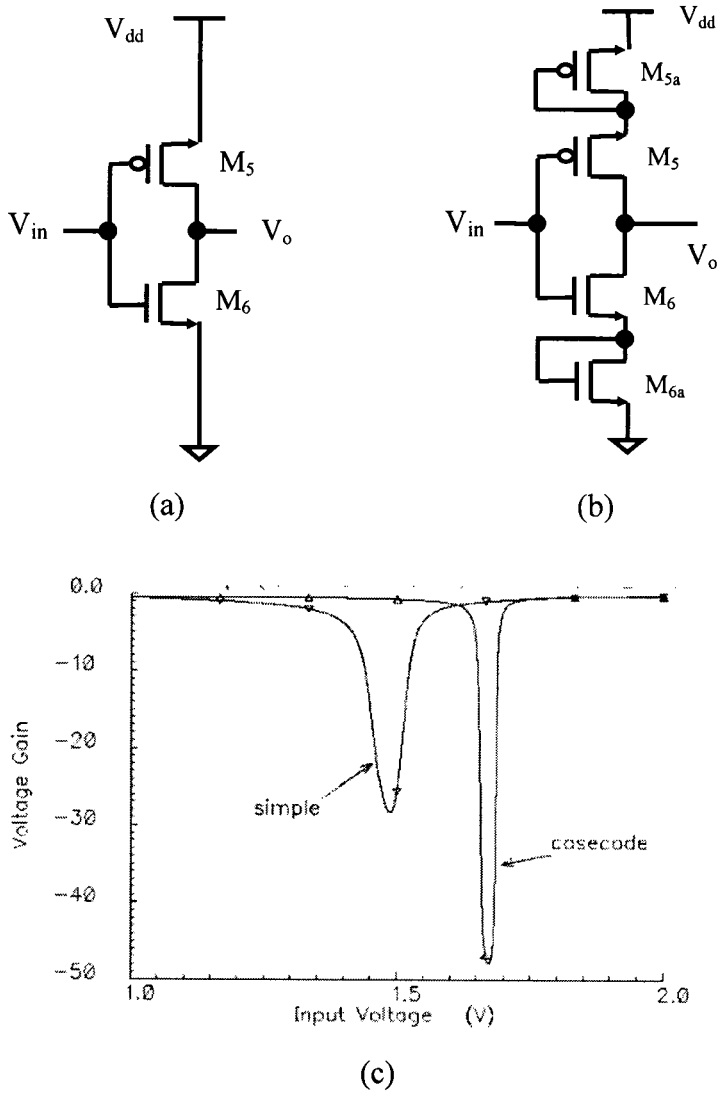


Figure 8-3: Gain and circuit of two compact amplifiers, a) voltage gain, b) simple inverter amplifier, c) cascode inverter amplifier

$$A_{simple} \approx -\frac{2}{\lambda_n + \lambda_p} \frac{\sqrt{\beta_5} + \sqrt{\beta_6}}{\sqrt{I_o}} \quad , \tag{8.3}$$

$$A_{cascode} \approx -\frac{4\sqrt{\beta_{5a}} \cdot \sqrt{\beta_{6a}}}{\sqrt{\beta_{6a}}\lambda_n + \sqrt{\beta_{5a}}\lambda_p} \cdot \left(\sqrt{\beta_5} + \sqrt{\beta_6}\right) \quad , \tag{8.4}$$

where λn and λp are the process related transistor channel modulation factors for the NMOS and PMOS transistors, respectively, and β5, β5a, β6 and β6a are the current factor of the transistor M5, M5a, M6, and M6a, respectively. Io is the current when the inverter is biased at the threshold point.

The proposed Miller hold capacitor S/H circuit is shown in Fig. 8-4. It consists of a sampling MOS switch M1, a Miller feedback circuit, two isolation MOS switches M2 and M4, and a high input-impedance unity gain buffer. Cp is a parasitic capacitance. The Miller hold capacitance is formed by the capacitors Csh1 and Csh2, a MOS pass transistor M7, and a CMOS cascode inverting amplifier. CI and Cp2 are the parasitic capacitances at the input and output of the inverting amplifier, respectively.

When the S/H circuit is in the sampling phase (ϕ1 is high), the input signal is sampled onto the S/H capacitance composed of Csh1 and Csh2 in parallel. The parasitic capacitor Cp is charged to a reference voltage Vref. During the transition from the sample phase to the hold/output phase, charge is redistributed among

Csh1, Csh2, CP, and CI, producing a charge sharing effect error. Meanwhile, the rapid turn-off of transistors M1 and M7, and the turn-on of transistor M2 results in charge injection onto nodes x and y.

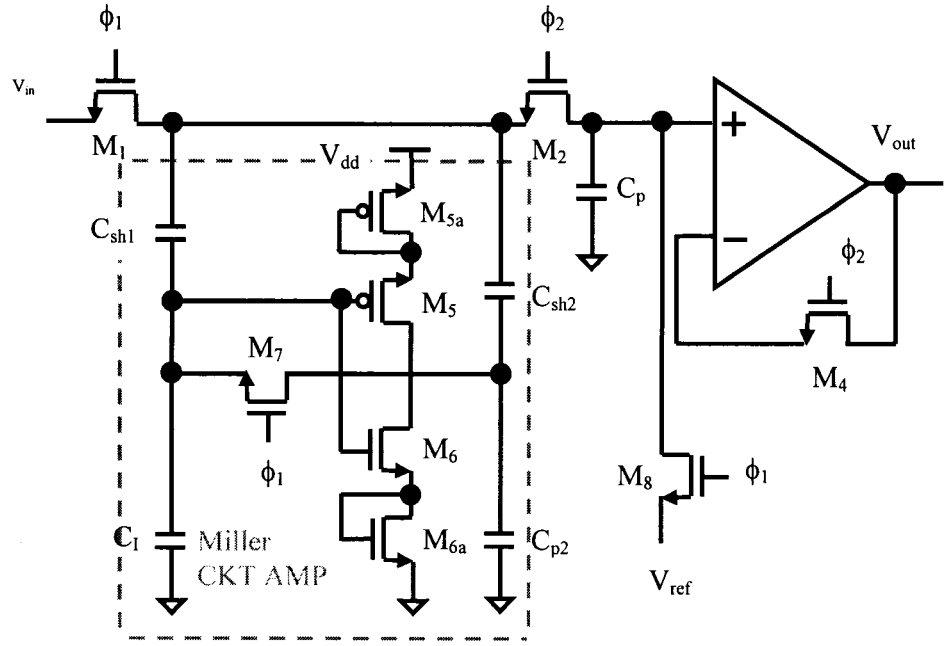


Figure 8-4: The proposed Miller hold capacitor S/H circuit

Increasing capacitance Csh reduces the dependence of the input signal on the CSE noise and clock feedthrough. ΔQy is the charge injected onto node y and ΔQx is the charge injected onto node x during the transition. Applying the charge conservation principle to nodes y and x,

$$-v_x[t_{hold}]\cdot C_{sh1} = v_y[t_{out}]\cdot C_I - \Delta Q_y + \left(v_y[t_{out}] - v_x[t_{out}]\right)\cdot C_{sh1}, \qquad (8.5)$$

$$v_x[t_{hold}]\cdot(C_{sh1}+C_{sh1}) = -\Delta Q_x + (v_x[t_{out}]-v_y[t_{out}])\cdot C_{sh1}$$
$$+(v_x[t_{out}]-V_{ref})\cdot C_p + (v_x[t_{out}]+Av_y[t_{out}])\cdot C_{sh2}\,, \qquad (8.6)$$

$$v_x[t_{hold}] = V_{in}\,, \qquad v_x[t_{out}] = V_0 \qquad (8.7)$$

Solving (8-5) - (8-7), the S/H circuit output voltage is:

$$V_o \approx V_{in} - \frac{(C_{sh1}+C_l)\cdot C_p\cdot(V_{ref}-V_{in})}{AC_{sh1}C_{sh2}+(C_{sh1}+C_{sh2}+C_p)\cdot(C_{sh1}+C_l)}$$
$$+\frac{(C_{sh1}+C_l)\cdot\Delta Q_x - AC_{sh2}\Delta Q_y}{AC_{sh1}C_{sh2}+(C_{sh1}+C_{sh2}+C_p)\cdot(C_{sh1}+C_l)}\,. \qquad (8.8)$$

The error voltage due to the charge sharing effect and clock feedthrough are represented by the second and third term in the right side of (8-8), respectively.

8.3. Results and Discussion

The charge sharing effect and clock feedthrough noises in the S/H circuit without a Miller capacitor (see Fig. 7-1b) is

$$V_o(error) = -\frac{C_p\cdot(V_{ref}-V_{in})+\Delta Q_x}{C_{sh1}+C_{sh2}+C_p}. \qquad (8.9)$$

For the proposed S/H circuit shown in Fig. 8-4, the noise caused by the charge sharing effect can be reduced to -(Vref – Vin)*Cp/ACsh2 for A >> 1. The S/H capacitance Csh2 is amplified by the gain A via the action of the Miller feedback circuit. As compared to the output error described by (8-9) in circuit shown in Fig. 7-1b, the CSE is greatly reduced. If A is large, the clock feedthrough error is reduced to ΔQy/Csh1. Because the voltage at node y in Fig. 8-4 is fixed, the clock feedthrough injected charge ΔQy is a constant, making the clock feedthrough error independent of the input signal.

Comparing (8-9) and (8-8), the CSE noise is reduced and the clock feedthrough error is no longer input signal dependent with the use of Miller feedback circuit. This analysis shows that with a Miller feedback circuit, the S/H capacitors Csh1 and Csh2 reduce the CSE and clock feedthrough errors. For CSE error reduction, a large S/H capacitance Csh2 is desired, and a large Csh1 is required to decrease the clock feedthrough. In practical applications where the parasitic capacitance Cp is large, the capacitance Csh2 should also be large.

8.4. Simulation Results

Both the S/H circuits with and without the Miller feedback circuit (see Figs. 7-1b and 8-4) have been investigated. SPICE simulation results are presented in Figs. 8-5 and 8-6. In the simulations, the total S/H capacitance (Csh1 + Chs2) is 1 pF, and the parasitic capacitance Cp is 0, 80 fF, and 320 fF.

The error voltage of the proposed S/H circuit is shown in Fig. 8-5 to be almost flat when the parasitic capacitance Cp is small (0 and 80 fF). The CSE noise is greatly reduced when compared to the S/H circuit without Miller capacitor, and the clock feedthrough error is no longer input independent. For the case of a large parasitic capacitance Cp (320 fF), the output error is a much weaker function of the input signal as compared to the S/H circuit without a Miller capacitor (see Fig. 7-1b).

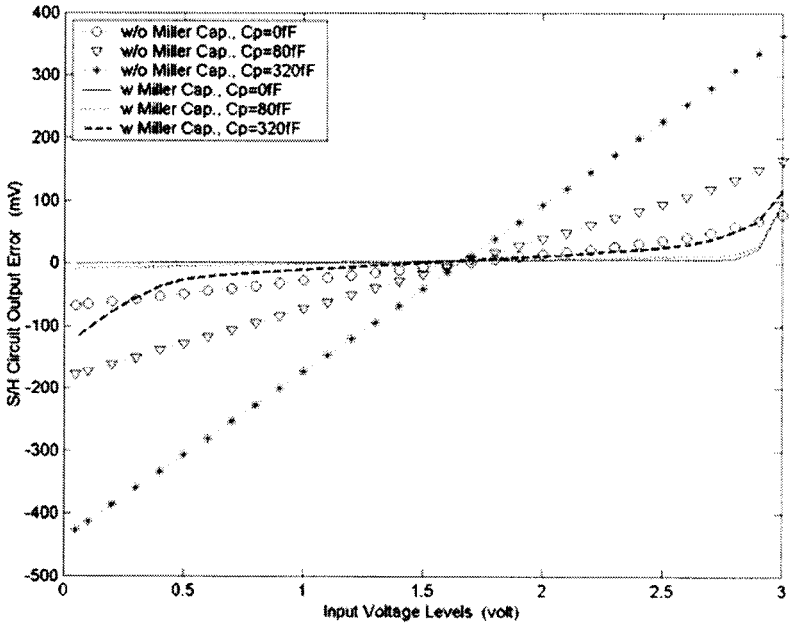


Figure 8-5: Output error of circuits with and without the Miller feedback circuit

For the case of Cp = 80 fF, the slope of the curve (the error gain) is reduced from 0.11 to 0.01 when the Miller capacitance is used. A reduction in the error

voltage of ten times is therefore achieved with the proposed S/H circuit. The nonlinear shape of the slope occurs when the input signal is near the power supply and ground, and is due to the nonlinear voltage gain A of the Miller feedback amplifier (see Fig. 8-3a). A larger Cp generates a higher error voltage [see (8-8)] and shifts the Miller feedback amplifier farther from the threshold voltage

As discussed in the previous section, the S/H capacitors Csh1 and Csh2 have a different effect on reducing the CSE and switching error. Simulations characterizing two combinations of Csh1 and Csh2 for the S/H circuit shown in Fig. 8-4 are illustrated in Fig. 8-6. For Csh1 = 300 fF and Csh2 = 700 fF, the slope of the error voltage curve is about 0.03 while in the second case (Csh1 = 700 fF and Csh2 = 300 fF), the slope is 0.13. The simulations agree with prediction that the CSE error in the S/H circuit is inversely proportional to the value of Csh2.

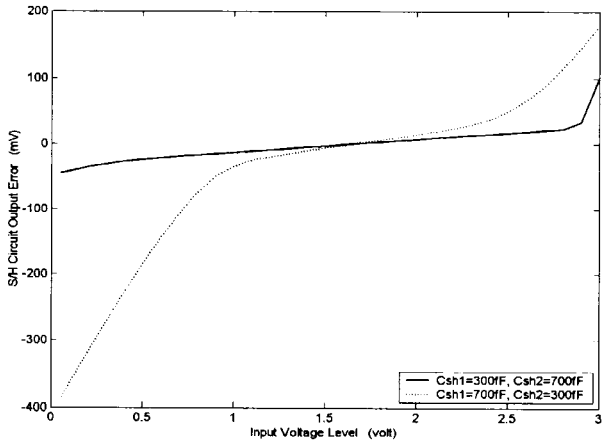


Figure 8-6: Simulated output error of the proposed circuit with different S/H capacitance ratios

The reduction in CSE noise and clock feedthrough due to the Miller feedback amplifier using a cascode inverter is compared to the reduction from using a simple inverter. These results are shown in Fig. 8-7. The proposed S/H circuit using a cascode Miller feedback amplifier has a lower error and a smaller slope due to the higher gain and smaller CI. The linearity of the curve when the input signal is near the power supply voltage and ground, however, is worse as compared to the S/H circuit with a simple amplifier in the Miller feedback circuit.

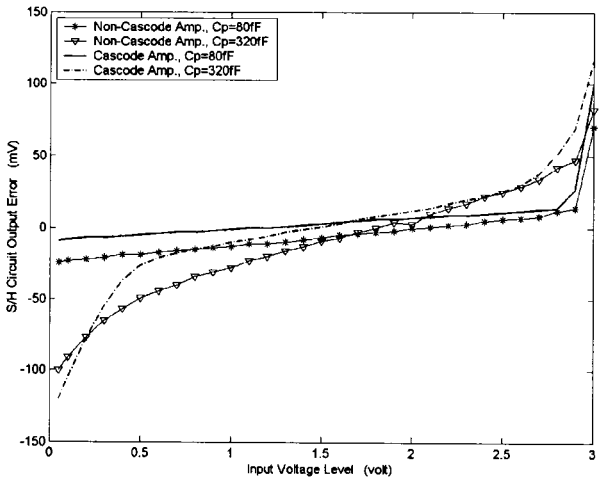


Figure 8-7: Output error of a Miller capacitance S/H circuit with a simple inverting amplifier and cascode inverting amplifier

8.5. Conclusions

The switched capacitor Miller hold capacitance S/H circuit with a cascode inverting amplifier effectively reduces the charge sharing effect and clock

feedthrough. A 10X reduction in charge sharing effect and clock feedthrough error is achieved. Depending upon the architecture and application, the size of the two S/H capacitors Csh1 and Csh2 can be efficiently designed to reduce the noise. The reduction in CSE depends upon the value of the capacitor Csh2 and in the clock feedthrough on Csh1.

Chapter Nine: Random Transistor Mismatch in CMOS Differential Pairs

The operational amplifier (OPAMP) is a fundamental and widely used block in many analog circuits such as gain circuits, sample/hold (S/H) circuits, integrators, A/D and D/A converters, and filters. The application frequency for OPAMPs ranges from DC to high frequency RF. For those applications where high output signal accuracy is required such as A/D converters, small OPAMP offset and CMRR (common mode rejection ratio) variations are necessary. In certain applications (such as RF), a large signal-to-noise ratio (or a small CMRR) is needed when the signals are extremely weak. In almost all OPAMPs, the differential pair is used as the input stage due to the inherently good common mode voltage rejection ratio of a differential pair.

Transistor mismatch in operational amplifiers affects the performance of CMOS differential pair amplifiers by adding error to the amplifier parameters. Generally, transistor mismatches originates from two sources: systematic and random mismatches. In this chapter, random transistor mismatch, which is difficult to reduce by layout techniques, is discussed. An analysis of the effect of random transistor mismatch on the differential amplifier input offset voltage and common-mode rejection ratio (CMRR) is presented in this chapter. The analysis shows in

this chapter that a typical CMOS differential amplifier has a minimum offset voltage of about one to two mV (higher for a PMOS differential pair). A minimum variation of 5% in the CMRR in an NMOS differential pair amplifier is expected. Increasing the transistor size in a differential pair is shown to be an effective way to reduce these random errors.

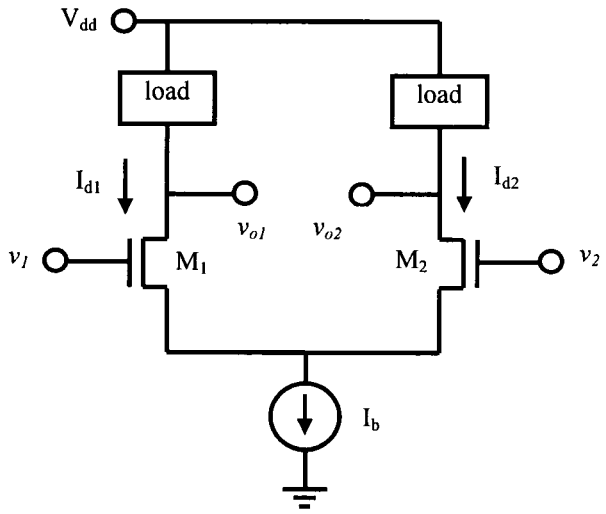


Figure 9-1: An N type CMOS differential pair stage

The differential pair is composed of two same type and same size transistors with the source of each transistor connected to the same high AC impedance node (usually a current source) as shown in Fig. 9-1. The differential pair stage supplies high common-mode rejection. Together with the second buffer stage, the OPAMP produces a small input offset voltage. Practically, however, the two transistors in a differential pair are not precisely the same due to transistor mismatch. Transistor

mismatch should therefore be considered during the OPAMP design and layout process in order to avoid high offset voltage, low common-mode voltage rejection ratio, and low yield.

In this chapter, the effects of random MOS transistor mismatch on differential pairs are discussed. Methods that optimize differential pair matching are proposed. Component mismatch is not a new topic. Many papers on IC component matching have been published during the past several years [44], [45], [47], [59], and [108]-[114], such as on the topics of capacitor mismatch [44], [45], [59], transistor mismatch [47], [111], [113], [114], and the effects of component mismatch on current sources [45], [47], [111], [113] and [114], D/A converters [45], [109]-[111], and bandgap reference generators [47]. In this chapter, the effects of random transistor mismatch on MOS operational amplifiers are evaluated based on widely used component mismatch models as reported in [47], [111].

The chapter is organized as follow. In Section 9-1, MOS transistor mismatch is reviewed and discussed. The MOS differential pair and related errors such as offset-voltage and common-mode noise rejection are analyzed in Section 9-2. Finally, some conclusions are presented in Section 9-3.

9.1. MOS Transistor Random Mismatch

Device mismatch is the difference in parameters of two identical components. In general, there are two types of variations in integrated circuits: global variations

which account for the total variation of a parameter over a wafer, and local variations or mismatches which reflect the variation in a parameter within a local region. MOS transistors in a differential pair are typically placed physically close to each other, making local variations the dominant source of component mismatch. Local variations, therefore, are the focus of this chapter.

MOS transistor mismatch originates from two sources: systematic error, which affects adjacent elements with similar geometry [45], [59], and random variations of transistor parameters which differ from element to element. Systematic mismatch can be greatly reduced with layout techniques [47], [109], [114]. The random nature of transistor mismatch, however, cannot be corrected or improved by layout techniques. Circuit errors due to random component mismatch can be minimized by applying certain circuit design techniques. Transistor mismatch is a combination of variations in the threshold voltage, gate capacitance, channel length and width, and carrier mobility. These variations are reviewed in the following subsections.

9.1.1. Variations in MOS Threshold Voltage

The MOS threshold voltage V_T changes with variations in process and bias conditions. The dependence of the threshold voltage on the process and the source-to-body voltage V_{SB} is

$$\left|V_T\right| = \left|V_{T0}\right| + \gamma\left(\sqrt{\left|2\phi_p\right| + \left|v_{SB}\right|} - \sqrt{\left|2\phi_p\right|}\right) \quad , \tag{9.1}$$

$$\left|V_{T0}\right| = \phi_{GB} - 2\phi_F - \left(\sqrt{2qN\varepsilon_{si} - 2\left|\phi_p\right|} + Q_{ss}\right)\Big/ C_{OX} \, , \tag{9.2}$$

where γ is the body effect coefficient.

The standard deviation of V_T and γ is

$$\sigma^2(V_T) = \frac{A_{VT}^2}{WL} + S_{VT}^2 D^2 \tag{9.3}$$

$$\sigma^2(\gamma) = \frac{A_\gamma^2}{WL} + S_\gamma^2 D^2 \quad , \tag{9.4}$$

where A_{VT}, S_{VT}, A_γ, and S_γ are process dependent parameters, D is the distance between two transistors, and W and L are the transistor width and length, respectively.

9.1.2. Variations in the MOS Transistor Current Factor

Most MOS transistors in analog ICs operate in the saturation region. A first order I-V model of the saturation region is most frequently used to approximate the transistor behavior in analog circuits.

$$I_D = \frac{C_{OX}\mu_n}{2}\left(\frac{W}{L}\right)\cdot(V_{GS}-V_{TN})^2 = K(V_{GS}-V_{TN})^2, \tag{9.5}$$

where K is the MOS transistor current factor, Cox is the gate oxide capacitance, μn is the carrier mobility, and V_{TN} is the N-channel threshold voltage. By examining the mutually independent components, W, L, μ, and Cox, the matching properties of the current factor K are [47]

$$\frac{\sigma^2(k)}{k^2} = \frac{A_W^2}{W^2} + \frac{A_L^2}{L^2} + \frac{A_{Cox}^2}{C_{OX}^2} + \frac{A_\mu^2}{\mu_n^2} + S_K^2 \cdot D^2. \tag{9.6}$$

The parameters A_W, A_L, A_{Cox}, A_μ, D, and S_k are process dependent. Examples of these parameters for two different technology generations [47], [109] are listed in Table 9-1.

Table 9-1 Matching Parameters of a 2.5 μm and a 0.6 μm CMOS Process

Parameter	NMOS		PMOS		Unit
	2.5 μm	0.6 μm	2.5 μm	0.6 μm	
A_{VT}	30	13	35	22	mVμm
A_γ	16x10-3		12x10-3		$V^{0.5}$μm
A_k	2.3	1.9	3.2	2.8	%μm
S_{VT}	4		4		μV/μm
S_γ	4		4		$10^{-6}V^{0.5}$/μm
Sk	2		2		10^{-6}/μm

Mismatches in μ and Cox have a similar relationship with W and L as described by (9-3) and (9-4). As analyzed by Pelgrom in [47], the standard deviation of L and W are $\sigma^2(L) \propto 1/W$ and $\sigma^2(W) \propto L$. Equation (8-6) can be further simplified to

$$\frac{\sigma^2(k)}{k^2} \approx \frac{A_K^2}{WL} + S_k^2 D^2 \quad . \tag{9.7}$$

9.1.3. Drain Current Mismatch

Highly accurate match in the current is required in most basic analog integrated circuits such as current mirrors, differential pair amplifier stages, reference voltage generators, and current mode circuits. In this section, current mismatch in MOS transistors is discussed.

Mismatch in the MOS transistor drain current originates primarily from two sources: threshold voltage V_T and current factor K mismatch. The relationship between the drain current mismatch and mismatches in V_T and K is established in [47] for transistors operating in the saturation region.

$$\frac{\sigma^2(\Delta I)}{I^2} = \frac{\sigma^2(\Delta K)}{K^2} + 4\frac{\sigma^2(\Delta V_T)}{\left(V_{GS} - V_T\right)^2}. \tag{9.8}$$

Variations in the mismatch between equal area MOS transistors, which have been observed in V_T and K, are demonstrated by the mismatch in drain current I_D through the relationship shown in (9-8). Although (9-8) is intended for the linear region, the measured data described in [47] notes that transistors operating partly in the saturation region could also be accurately predicted by (9-8). The measured data described in [111] indicate that equal size transistors with short channel lengths and wide channel widths are more poorly matched than transistors with long channel lengths and narrow channel widths. Similar to mismatch in the threshold voltage V_T and current factor K, transistors with a small W/L ratio produce a higher drain current matching than transistors with a large W/L ratio.

9.1.4. Gate-to-Source Voltage (V_{GS}) Mismatch

In differential pairs, the drain current I_D in transistors M1 and M2 (see Fig.9-1) is designed to be the same magnitude. The random error exists in the transistor voltage V_{GS}, which causes a random error in the input offset voltage of the amplifier. The variance of the transistor gate-to-source voltage is [117]

$$\Delta V_{GS} = \frac{\Delta I_D}{g_{m0}} \quad , \tag{9.9}$$

$$\sigma^2(V_{GS}) = \frac{\sigma^2(I_D)}{g_{m0}^2} . \tag{9.10}$$

From (9-8),

$$\sigma^2(V_{GS}) = \sigma^2(\Delta V_T) + \frac{(V_{GS} - V_T)^2}{4} \cdot \sigma^2\left(\frac{\Delta K}{K}\right). \tag{9.11}$$

9.2. MOS Differential Pair

In the previous section, random variations in individual MOS transistor are discussed. Based on the expressions developed in the previous section, the effects of random transistor mismatch on CMOS differential pairs are analyzed in the following subsections.

9.2.1. Offset Voltage Due to Random Transistor Mismatch in MOS Differential Pairs

An NMOS differential pair is shown in Fig. 9-2. M1 and M2 form a differential pair. Mb supplies the DC tail current for M1 and M2. M3 and M4 are the active loads for the differential pair. M1, M2, M3, and M4 are all the same size. The mismatch due to the geometric variations in W and L can be reduced with layout techniques such as the common-centroid layout [49], which can cancel the effects of long range variations as long as these variations are linear functions of distance. In such a layout as shown in Fig. 9-3, transistors M1 and M2 are divided into segments or fingers. The simplest types of arrays involve the placement of multiple devices structured as fingers in parallel, as shown in Fig. 9-3. Dummy unit

transistors are typically placed around the array for improved matching of any coupling within the array.

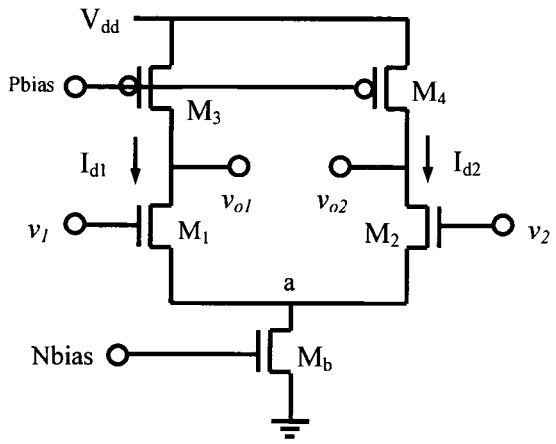


Figure 9-2: A standard CMOS differential pair amplifier stage

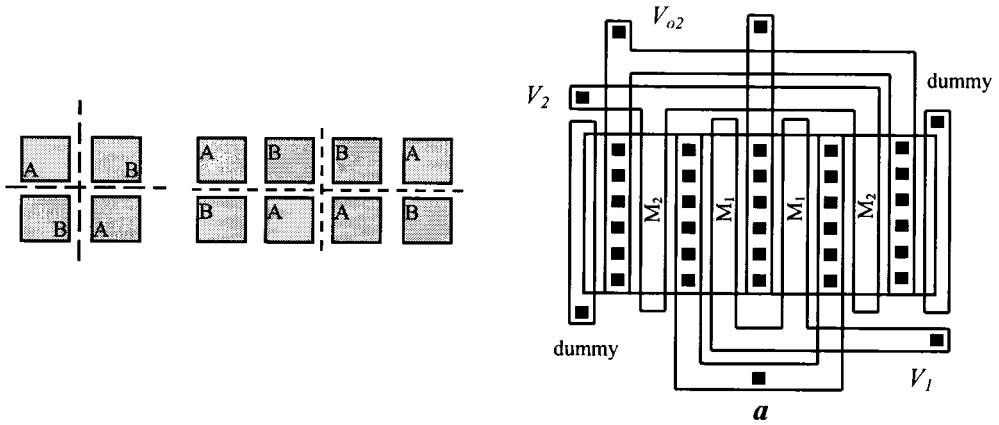


Figure 9-3: The common-centroid layout technique for improving component matching, a) examples for matching components A and B, b) application to layout of M1 and M2 of a MOS differential pair

When a DC voltage V_A is applied to both inputs of a differential amplifier, currents Id1 and Id2 flow in transistor M1 and M2, respectively. The sum of Id1 and Id2 equals the tail current supplied by transistor Mb. Ideally, the two outputs produce the same voltage. The two outputs, however, can produce a different voltage due to mismatches in M1 and M2. This voltage difference is the offset voltage of the amplifier. The offset voltage of a differential pair caused by random transistor mismatch is discussed below.

An important characteristic of a differential amplifier is the minimum detectable differential voltage. The presence of component mismatch produces differential voltages at the amplifier output that are indistinguishable from the signal being amplified.

In many analog systems, this type of error is the fundamental limitation on the system resolution. The effects of mismatch on the DC performance of an amplifier are most conveniently represented by the input offset voltage [115], [116]. When one input of a differential pair has a DC voltage Va, a voltage Va ± V_{OS} is applied on the second input to drive the differential amplifier output to zero. This additional voltage V_{OS} is called the amplifier input offset voltage.

$$V_{OS} - V_{GS1} + V_{GS2} = 0 \quad . \tag{9.12}$$

From (9-3), (9-4), (9-7), and (9-11), the standard deviation of V_{OS} is

$$\sigma^2(V_{OS}) = 2 \cdot \sigma^2(V_{GS}) = \frac{2}{WL} \cdot \left(A_{VT}^2 + \frac{(V_{GS} - V_T)^2}{4} \cdot A_k^2 \right) \quad . \qquad (9.13)$$

As listed in Table 9-1, the deviation constant A_{VT} of the threshold voltage is much greater than A_K, the deviation in the MOS transistor current factor K. The mismatch in the threshold voltage dominates the differential amplifier random error in the input offset voltage. As shown by (9-13), the larger transistor size and smaller V_{GS} - V_T yield a smaller error in the offset voltage. Also, the transistor drain current is proportional to $(V_{GS}$ - $V_T)2$. The input offset voltage of the differential amplifier is therefore proportional to the bias current in the transistors M1 and M2. However, A_{VT} is much larger than A_K such that the input offset voltage of the differential amplifier is almost independent of the bias current if the transistors are sufficiently large.

Assuming the systematic error between the size of the transistors M_1 and M_2 is zero, the relationship between the MOS transistor size and the input offset voltage of the MOS differential amplifier is due to random mismatch in the transistors. This behavior is described by (9-13) and shown in Fig. 9-4.

As shown in Fig. 9-4, a large deviation in the input offset voltage caused by random mismatch in M1 and M2 exists in a MOS differential amplifier if the transistors in the differential pair are small. A larger offset voltage mismatch occurs in a PMOS differential pair than in an NMOS differential pair due to the larger A_{VT} and A_K in a PMOS transistor. This mismatch in the input offset voltage is random

in nature and difficult to remove. Offset compensation techniques can be used to reduce the effects of random mismatch in the input offset voltage. As shown in Fig. 9-4, a minimum standard deviation of offset voltage of about 1 mV occurs in a NMOS differential pair even if the transistor sizes are large. In standard CMOS operational amplifiers, the transistor width of the input differential pair ranges between 10 μm and 100 μm for channel lengths between 0.8 μm and 1 μm. From Fig. 9-4, the CMOS operational amplifier has a standard deviation of offset voltage ranging from 1 mV to 3 mV independent of the physical layout. For a PMOS differential pair, A_{VT} is more than twice that of an NMOS transistor. A much larger transistor size is therefore required to reduce the mismatch in the input offset voltage due to random mismatch in a PMOS transistor.

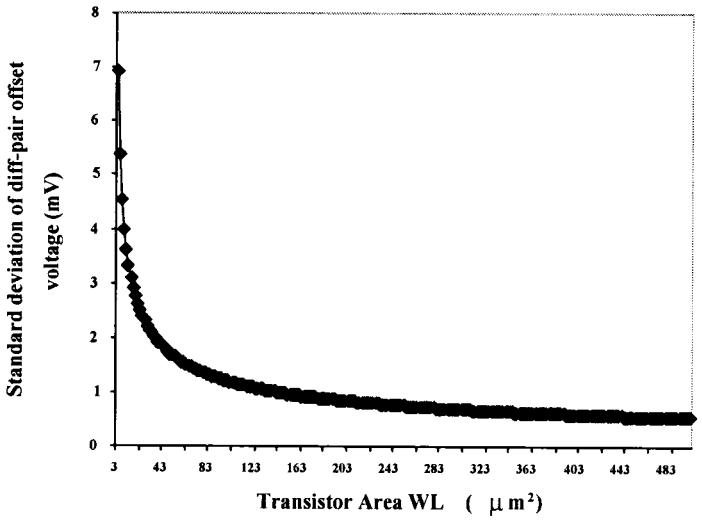


Figure 9-4: Mismatch of input offset voltage of an NMOS differential amplifier (pair) for different transistor sizes for a 0.5 μm CMOS process (A_{VT} = 12 mV*μm, and A_K = 1.5% μm)

9.2.2. Common-Mode Rejection Ratio (CMRR) of a CMOS Differential Pair

Any signals applied to the two inputs of a differential pair can be separated into the differential-mode voltage and the common-mode voltage.

$$V_{in\_c} = \frac{v_1 + v_2}{2} \quad , \tag{9.14}$$

$$V_{in\_d} = v_1 - v_2 \quad . \tag{9.15}$$

The CMRR is defined as

$$CMRR = 20\log\left(\frac{A_D}{A_C}\right) \quad , \tag{9.16}$$

where AD and AC are the differential-mode voltage gain and common-mode voltage gain of a differential pair stage, respectively. For the circuit shown in Fig. 9-2, the MOS differential pair amplifier has a common-mode rejection ratio CMRR,

$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right| = 1 + 2\frac{g_{m3} + 1/r_3}{g_b + 1/r_b} \cdot \frac{g_{m1} + 1/r_1}{g_{m3} + 1/r_1} . \tag{9.17}$$

Normally, 1/rb << gb, 1/r3 << gm3, 1/r1 << gm1, and gb << gm1, the CMRR can be approximated as

$$CMRR \approx \frac{2 \cdot g_{m1}}{g_b}. \tag{9.18}$$

From (9.3), (9.4), (9.7), and (9.8),

$$\begin{aligned} \frac{\sigma(\Delta CMRR)}{CMRR} &\approx \left(\frac{\sigma^2(\Delta k)}{k^2} + \frac{\sigma^2(\Delta I_{D1})}{I_{D1}^2} \right)^{1/4} \\ &\approx \left(2\frac{A_k^2}{WL} + 4\frac{A_{VT}^2}{WL} \cdot \frac{1}{\left(V_{GS}/V_T - 1\right)^2} \right)^{1/4}. \end{aligned} \tag{9.19}$$

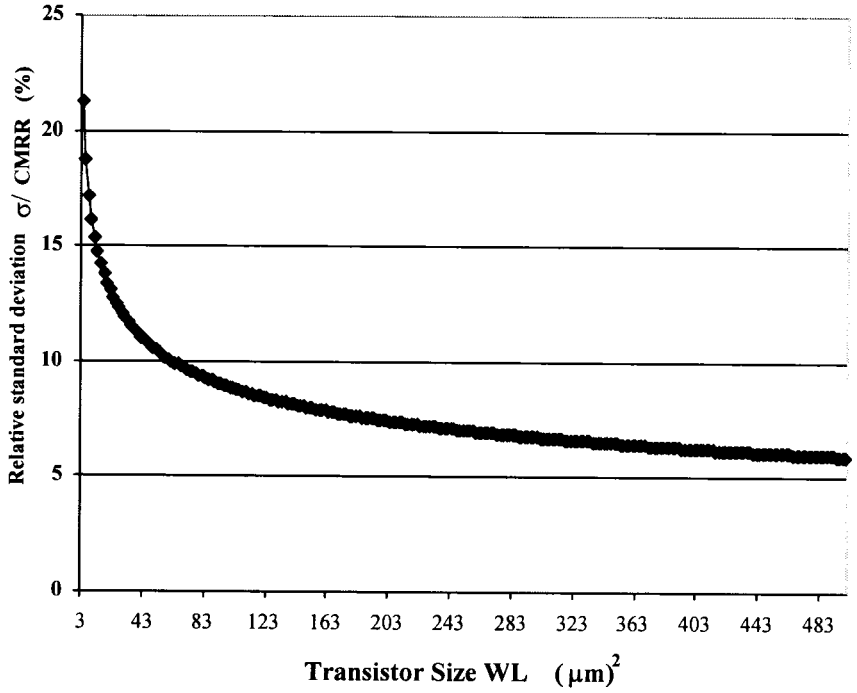


Figure 9-5: Variation of CMRR for an NMOS differential pair amplifier for a 0.5 μm CMOS process.

For a 0.5 μm CMOS process under the condition of V_{GS}/V_T = 1.3, A_{VT} = 12 mV*μm, and A_K = 1.5% μm, the random variation (or mismatch) of the common-mode voltage rejection as a function of the transistor size WL is shown in Fig. 9-5. A minimum 5% variation in the relative standard deviation of CMRR is due to random transistor mismatch. A random mismatch in the transistor threshold voltage is the primary source of the variation in CMRR. An effective technique for reducing this random mismatch in CMRR is the use of large transistor sizes in the differential pair. In specific applications where high accuracy is required such as A/D converters, variations in CMRR could affect product yield. A large transistor size should therefore be used in differential pair transistors in these applications.

9.3. Conclusions

An analysis of the mismatch of the input offset voltage and common-mode rejection ratio of a differential pair amplifier is discussed in this chapter. The analysis shows that a typical CMOS differential pair amplifier has a minimum standard deviation of offset voltage rangung from 1 to 2 mV (higher for a PMOS differential pair). A minimum variation (or mismatch) of 5% in relative standard deviation of CMRR is shown to occur in NMOS differential pair amplifiers. These errors are due to random transistor mismatch and cannot be removed or reduced by layout techniques. The use of large transistors in the differential pair is the primary method used to reduce these random errors. A larger transistor size is required for a

pair of PMOS transistors in order to reduce the input offset voltage and to improve the CMRR due to higher random mismatch in PMOS transistors. From the point of view of random errors, NMOS transistors are therefore preferable in CMOS operational amplifiers.

Chapter Ten: Experiment Data

An on-chip circuit has been developed that can directly measure substrate and line-to-line coupling noise. This test circuit has been manufactured in a 0.35 μm double-well double polysilicon CMOS process and consists of noise generators and switched-capacitor signal processing circuitry. On-chip analog-to-digital conversion and calibration are used to eliminate off-chip noise and to extend the measurement accuracy by removing system noise. A scan circuit is described that enables the noise waveform to be reconstructed. On-chip generators ranging in area from 1 μm^2 to 6 μm^2 produce noise at the receiver decreasing from 3.14 mV/μm to 0.73 mV/μm. Open and closed guard rings reduce the noise by 20% and 85%, respectively. The difference between experimental and an analytic model of the line-to-line coupling capacitance ranges from 8.5% to 17.7% for different metal layers.

Complex high speed digital circuits together with high performance analog circuits are commonly integrated onto the same substrate. In such mixed-signal systems, fast switching transients produced by digital circuits can couple into sensitive analog components through both the substrate and line-to-line capacitances, thereby limiting the achievable analog precision. Furthermore, performance degradation caused by substrate and capacitive coupling noise is

difficult to control and even more difficult to predict. The requirement for highly accurate noise measurement to identify and manage on-chip noise has therefore become increasingly evident.

In order to evaluate substrate noise, on-chip test circuits are required to accurately and efficiently measure the substrate current [64], [68]-[72]. These measurements, however, are based on simple single MOS transistor test structures [71], [34], voltage comparator structures [69], [70], or single stage MOS differential amplifier structures [72]. Due to the analog output signals, a common problem in these measurements is the difficulty of acquiring output signals without other noise signals becoming mixed in the measured signal. The external circuitry and parasitic impedances affect the analog output signal, severely decreasing the measurement accuracy. The accuracy of these test structures is therefore usually quite poor.

Four different test circuits have been fabricated: two substrate coupling noise test circuits and two capacitive coupling noise test circuits. Substrate coupling noise test circuit I measures the substrate coupling noise generated from a substrate noise generator array where each individual substrate noise generator is of different size and distance to the noise receiver. Substrate noise test circuit II evaluates the reduction in substrate coupling noise due to guard rings. Noise generators are placed outside each guard ring so that the effect of the reduction in substrate noise due to each guard ring can be measured and evaluated. The capacitive coupling test

circuits measure the line-to-line capacitive coupling noise and capacitance. A microphotograph of the substrate and line-to-line capacitive coupling noise test circuits is shown in Fig. 10-1.

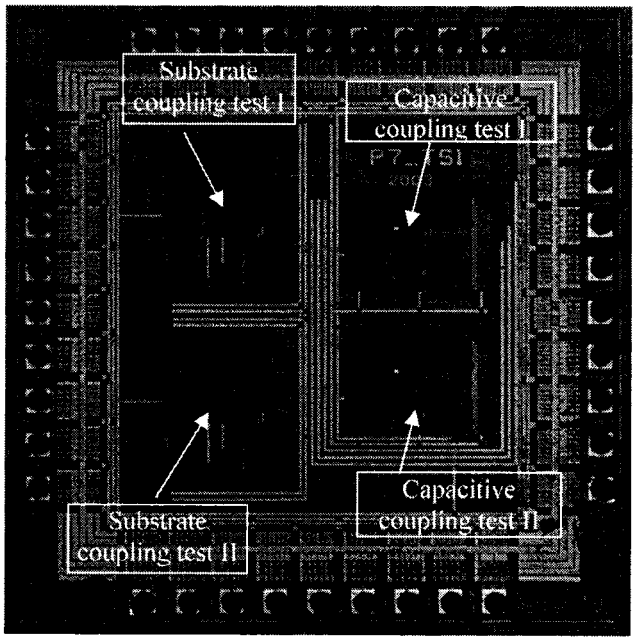


Figure 10-1: Microphotograph of the substrate and capacitive coupling test circuits

The substrate noise measurement technique is described in section 10.1. In section 10.2, experimental data from the substrate coupling noise test circuitry is presented and discussed. The test results describing the reduction in substrate noise due to the guard lines and rings are evaluated in section 10.3. The on-chip line-to-line capacitive coupling test technique and related test results are presented and

compared to an analytic model of line-to-line coupling capacitance in section 10.4. Finally, some conclusions are provided in section 10.5.

10.1. On-Chip Substrate Coupling Noise Test Technique

A specialized on-chip test circuit has been developed to directly measure substrate coupling noise. The test circuit utilizes differential switched-capacitor circuits with digital outputs. The test circuit has an input pin to enable on-chip system calibration to remove existing system noise. The circuit consists of a noise generator array, an analog signal processing (ASP)/analog-to-digital converter (ADC) block, a clock delay array, and a timing circuit, as shown in Fig. 10-2. The clock delay array generates 32 different delayed clocks to operate the ASP/ADC block such that the noise waveform can be reconstructed from 32 points that make up a substrate noise waveform. The delay time is set from 0 to 32 ns with a 1 ns step size.

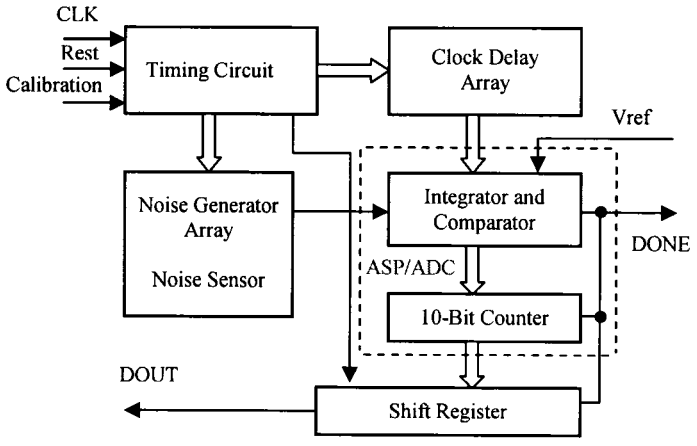


Figure 10-2: Block diagram of the noise coupling test circuit

The substrate noise is generated by an array of noise generators, each of different size and placed at different distances from each noise receiver. A decoder is used to control the noise generator array such that only one noise generator switches at any one time. The operation of the test circuit is as follow. The substrate coupling noise is sensed by the receiver and passed to the input of the integrator where the sensed noise voltage is amplified and integrated. The integrated coupling noise is converted to digital signals by an on-chip A/D converter consisting of a 1-bit differential comparator and a 10-bit counter. The integrated coupling noise is applied to the inputs of the comparator and compared to the reference voltages at each clock cycle as shown in Fig. 10-3.

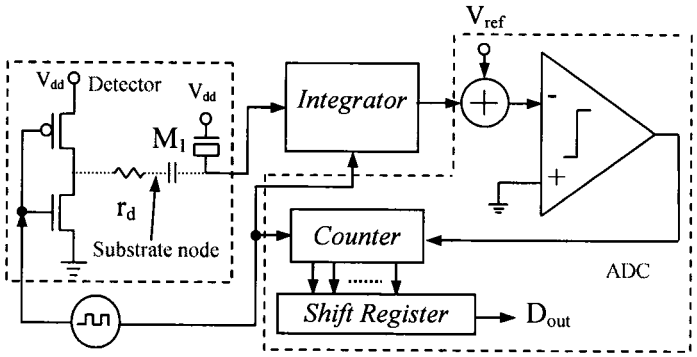


Figure 10-3: On-chip noise generator/receiver and analog-to-digital converter

Once the integrated coupling noise reaches the reference voltage, the comparator output flags the output pin (DONE shown in Figs. 10-2 and 10-4) to indicate the completion of the measurement process, terminating the counter and integrator. The

counter numerates the number of clock cycles during the integration period and the system uses the counted value as raw test data. At the end of each measurement, the value stored in the 10-bit counter is moved in parallel to a shift register from where the test data is shifted out (through the "DOUT" pin shown in Fig. 10-4).

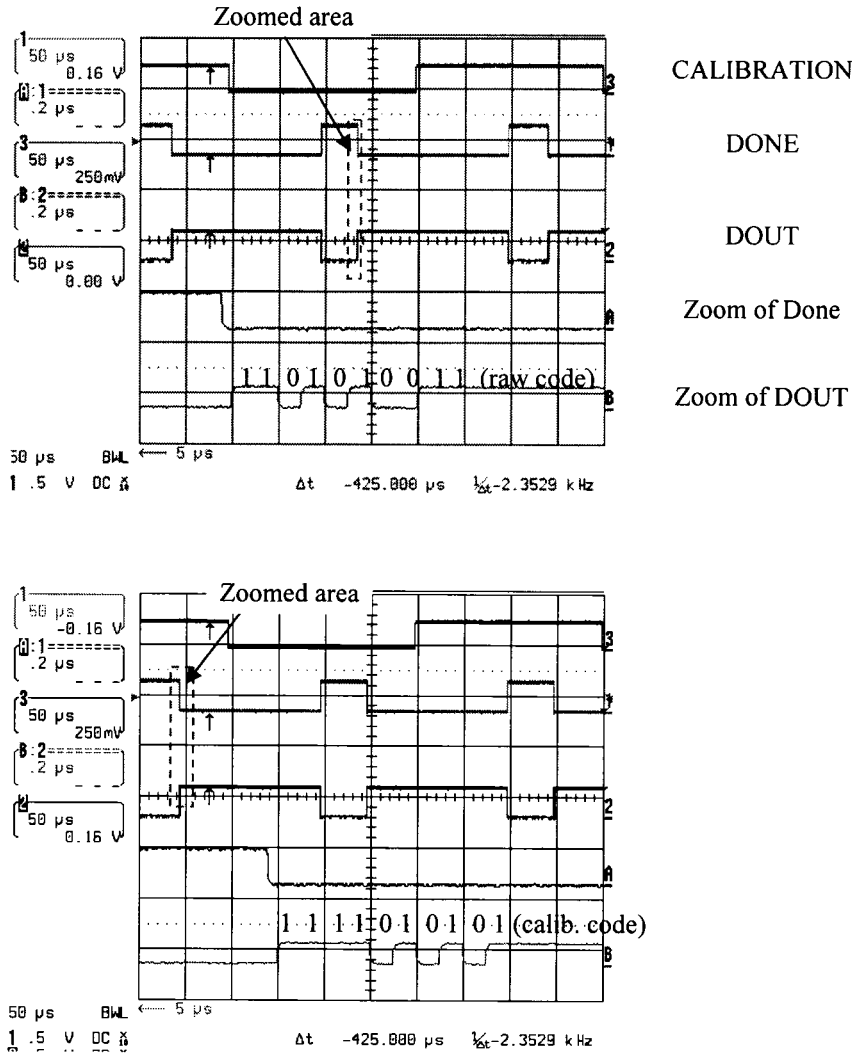


Figure 10-4: Measured output waveforms of the substrate coupling noise test circuit

The system noise in the measured data is removed by an on-chip calibration process. During the calibration process, the noise generators are maintained inactive such that only the system noise is integrated and compared to the reference voltages. A digital code is generated at the end of the calibration process and used to calibrate the raw test data. Each measurement generates two 10-bit digital codes, the raw data code and the calibration code. The peak-to-peak substrate noise voltage is determined from the integrator gain, reference voltages, and the decimal value of the two digital codes. One pair of the measured substrate raw and calibration codes is imported from the digital oscilloscope and is shown in Fig. 10-4. The waveforms on the top of Fig. 10-4 depict the raw data measurement and the waveforms on the bottom of Fig. 10-4 display the calibration test data. Five waveforms are shown in each imported screen. The upper waveform depicts the input calibration waveform, indicating whether the calibration test is "High." Below the calibration waveform is the single bit output indicating the completion of the measurement when the signal changes from "High" to "Low." Below the DONE waveform is the digital output signal DOUT. Greater resolution of the test results, the zoomed areas of waveform "DOUT," is shown at the bottom of Fig. 10-4.

A microphotograph of the substrate coupling noise test circuit is shown in Fig. 10-5, where the primary blocks in the test circuit are individually labeled. A five-bit decoder is placed around the noise generators in the noise generator array block, as

shown in Fig. 10-5. Two identical mirrored noise generator arrays, with an opposite clock phase, are placed next to each other to support the differential operation. A six-bit decoder is laid out around the delay array. Drivers are placed in front of the decoder inputs to drive the long buses. The power supply and ground buses of the analog and digital circuit are physically separate.

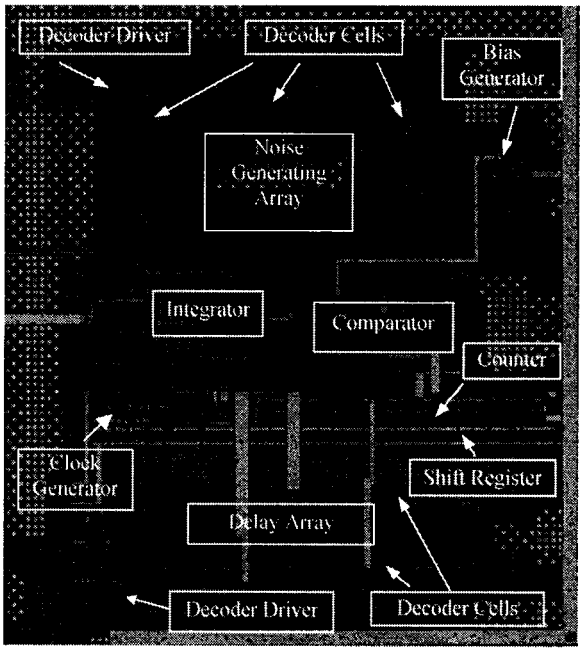


Figure 10-5: Microphotograph of the substrate coupling noise test circuit I

The noise receiver is an MOS gate capacitor formed by applying the power supply voltage V_{dd} on the gate of an NMOS transistor and connecting the source/drain (S/D) of the transistor as the input to the integrator circuit. The noise generator is an N^+ region, similar to the S/D of an NMOS transistor, with a specific size and distance from the receiver. A current is injected into the substrate from this

N^+ region when a clock signal is applied. The principle of the substrate coupling noise generator/receiver pair is illustrated in Fig. 10-6. Microphotographs of the noise generator/sensor are shown in Figs. 10-7 and 10-8. The noise generator size ranges from 0.5 μm^2 to 2 μm^2 and the distance to the noise receiver ranges from 1 μm to 20 μm.

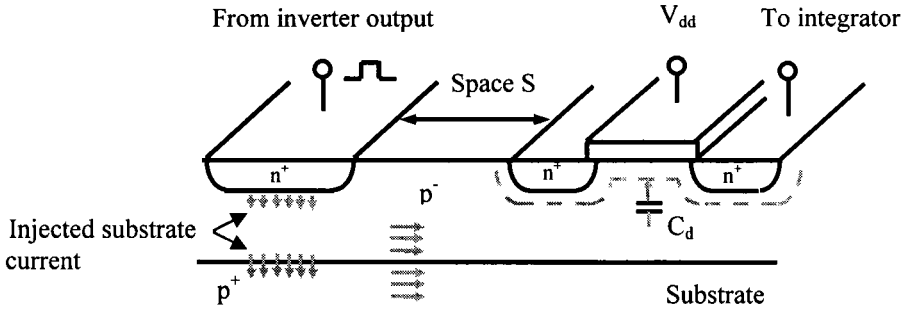


Figure 10-6: Operation of the substrate coupling noise generator/receiver pair

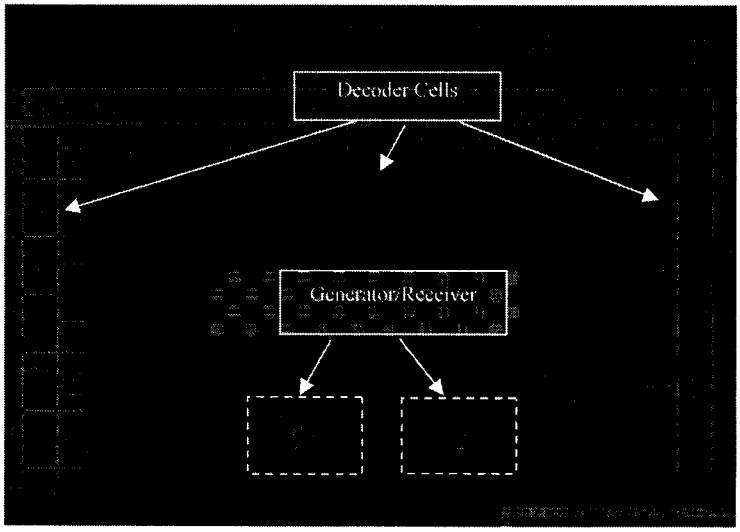


Figure 10-7: Microphotograph of the substrate coupling noise generator array

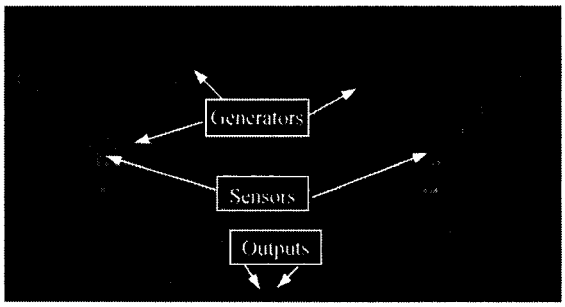


Figure 10-8: A closer look at the noise generator array

10.2. Experimental Data from the Substrate Coupling Noise Test Circuit

Each of the 21 noise generators on the substrate noise test circuit I have been evaluated, producing 32 different points on the substrate coupling noise waveforms for each noise generator. The substrate coupling noise voltage waveforms are reconstructed from these test data points. The test results of each of the 21 noise generators in the substrate noise generator array are summarized in Figs. 10-10 and 10-11. The results show that the substrate coupling voltage is proportional (but not linear) to the size of the noise generator. At 2.5 μm from the noise generators, the measured substrate coupling noise voltages are 18.2 mV, 23.45 mV, and 27.89 mV for noise generators of size 1 μm^2, 2 μm^2, and 4 μm^2, respectively. The injected substrate current from a larger noise generator can travel farther within the substrate. The measurement data also show that the substrate coupling noise voltages decrease exponentially as the signal propagates within the substrate. The noise signal, however, attenuates at a different rate for different noise generator

sizes. The substrate coupling noise voltage generated from large noise generators attenuates slowly as compared to smaller size noise generators, partially due to the effect of feedback on the voltage of the substrate current injecting PN junction [121]. The injected current produces a voltage drop between the injection node and ground due to the substrate resistance. This voltage drop due to the substrate resistance reduces the voltage across the PN junction, causing an increase in the PN junction capacitance as shown in Fig. 10-9. Additional current is therefore injected into the substrate due to this feedback effect, causing the noise signal to attenuate more slowly.

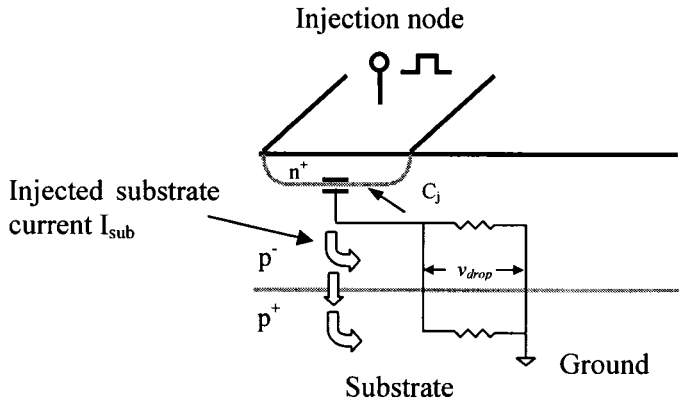


Figure 10-9: The effect of feedback on the PN junction capacitance due to the voltage drop caused by the substrate resistance

For noise generators of size 1 μm^2, 2 μm^2, 4 μm^2, and 6 μm^2, the peak-to-peak substrate noise voltage decreases as a function of distance and, for this substrate, is

3.14 mV/μm, 3.08 mV/μm, 1.98 mV/μm, and 0.73 mV/μm, respectively (see Fig. 10-10).

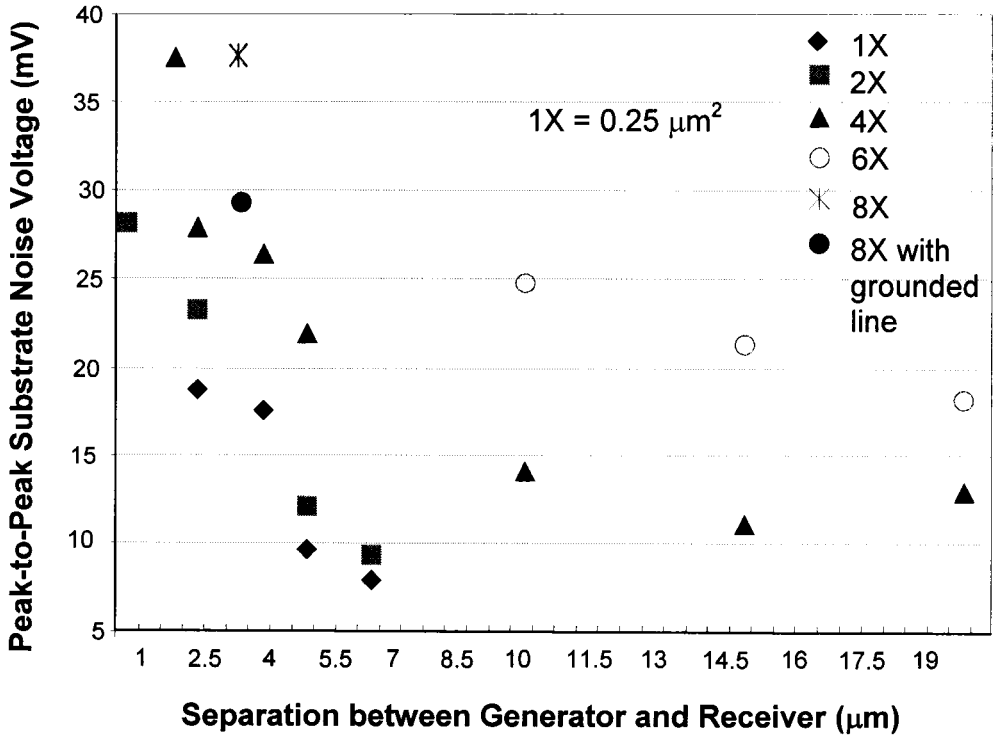


Figure 10-10: Measured substrate coupling noise voltage as a function of the noise generator size and distance from the noise receiver

A substrate coupling noise waveform reconstructed from the 32 point measurement is shown in Fig. 10.11. The substrate noise generator requires an area of 1 x 1 μm^2 and is placed 5 μm from the receiver. The test results illustrate the peak-to-peak substrate coupling noise voltage produced by the noise generator,

approximately 15 mV for this 0.35 μm CMOS p^-/p^+ substrate process. The epi-layer is 5.5 μm thick and has a resistivity ρ of 20 Ω·cm. The heavily doped p^+ substrate has a thickness of 120 μm and a resistivity of 0.03 Ω·cm. Note that the substrate coupling noise waveform attenuates quickly and diminishes in about 20 ns.

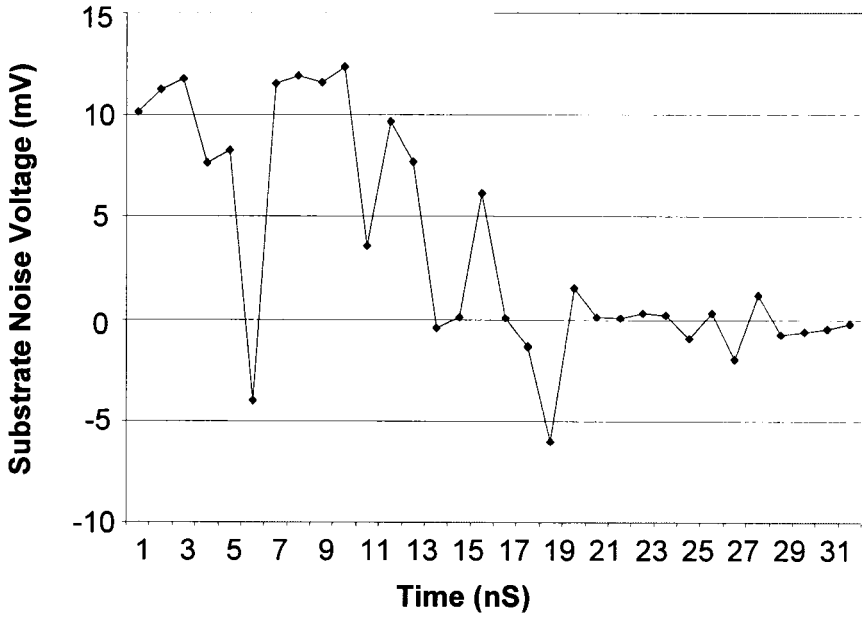


Figure 10-11: Reconstructed substrate noise waveform determined from 32 test points

10.3. Substrate Coupling Noise Reduction Due to Guard Lines and Rings

The noise generator array also includes a noise generator with an N^+ grounded line (also called a guard band) to separate the noise source from the noise receiver. The test results demonstrate that the guard line has only a limited effect on

reducing the substrate noise. As compared to the noise generator without a guard line, less than a 20% reduction in noise is measured for this N^+ grounded line test structure.

Eight structures for evaluating the reduction in substrate noise caused by the guard rings are evaluated. These guard rings are single 1.8 μm wide closed grounded N^+ rings as shown in Fig. 10-12. The measured results are displayed in Fig. 10-13. As compared with the measured results shown in Fig. 10-10, the substrate noise voltage coupled to the receiver is about six to eight times smaller than the noise voltage coupled to those receivers not surrounded by guard rings. Significant substrate coupling noise (as large as 7 mV as shown in Fig. 10-13), however, is measured for a receiver with a single closed grounded N^+ guard ring.

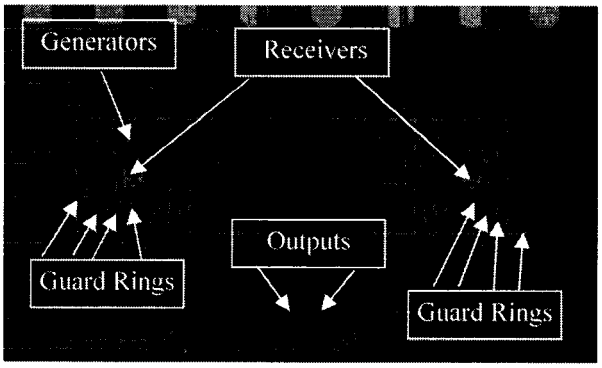


Figure 10-12: Microphotograph of the structures for evaluating the reduction in noise caused by guard rings

The reduction in noise for a single guard ring is approximately 85% (by comparing test data in Figs. 10-10 and 10-13). This measurement demonstrates that double or triple guard ring structures are required to efficiently reduce substrate coupling noise. In the measurement, the distance between the noise generator and noise receiver is shown to not influence the efficiency of the guard rings.

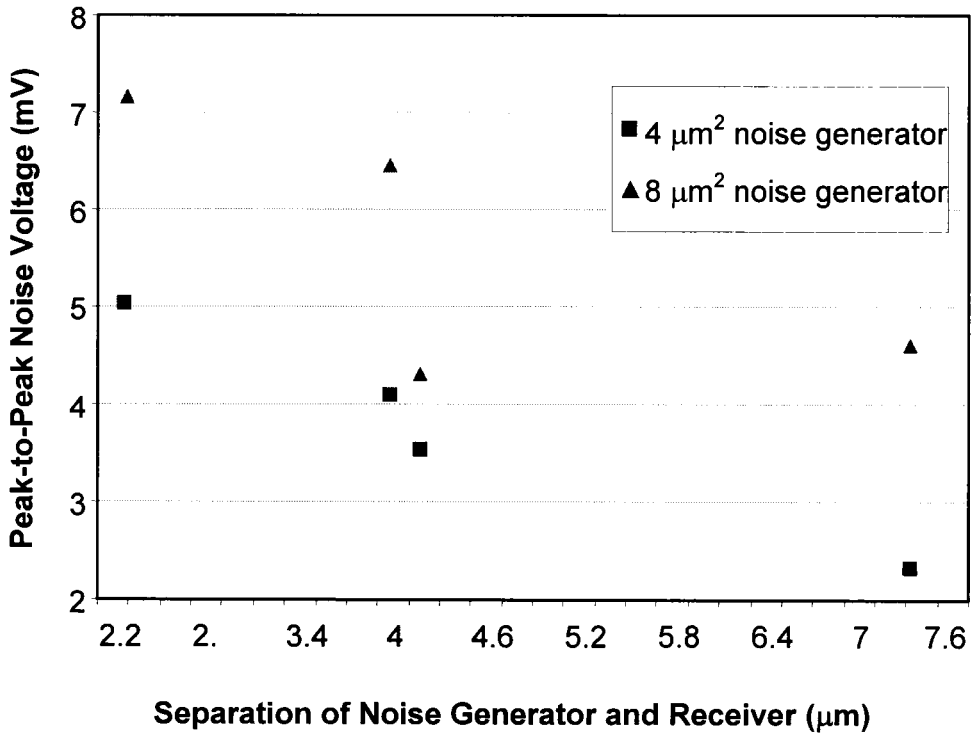


Figure 10-13: Measured reduction in substrate noise with guard rings

10.4. Line-to-Line Capacitive Coupling Measurement Results

Line-to-line capacitive coupling has also been evaluated based on the same signal processing circuitry but with different coupling structures as illustrated in

Figs. 10-14 and 10-15. In these test structures, all of the lines are 6 μm long and 0.7 μm in width. The coupling voltage between two lines on the same layer is measured from the digital output code pair (raw and calibration codes). An estimate of the coupling capacitance can also be obtained from

$$C_{coupling} = \left(\frac{1}{N} - \frac{1}{N_C} \right) \cdot \frac{V_{ref}}{V_{dd}} \cdot C_f \quad , \tag{10.1}$$

where N is the decimal value of the raw substrate coupling noise code, N_c is the decimal value of the calibration code, C_f is the feedback capacitance in the integrator circuit, V_{ref} is a DC reference voltage, and V_{dd} is the power supply voltage.

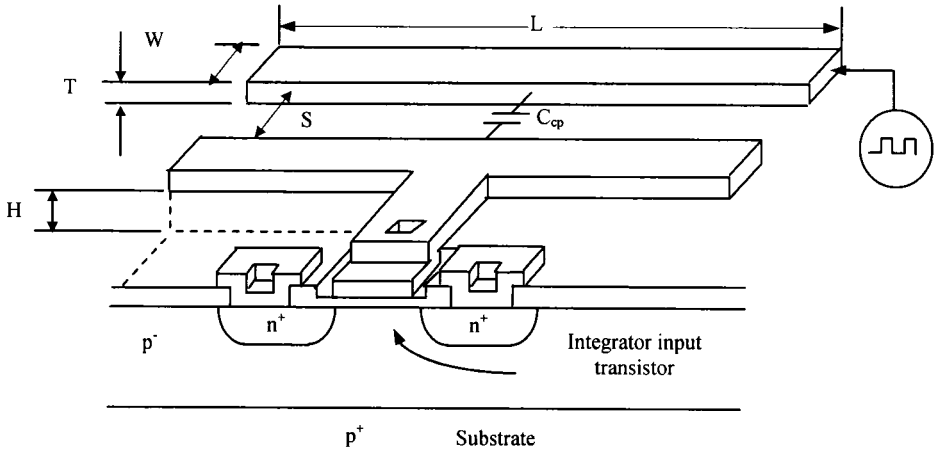


Figure 10-14: Test structure for sensing line-to-line capacitive coupling noise voltage

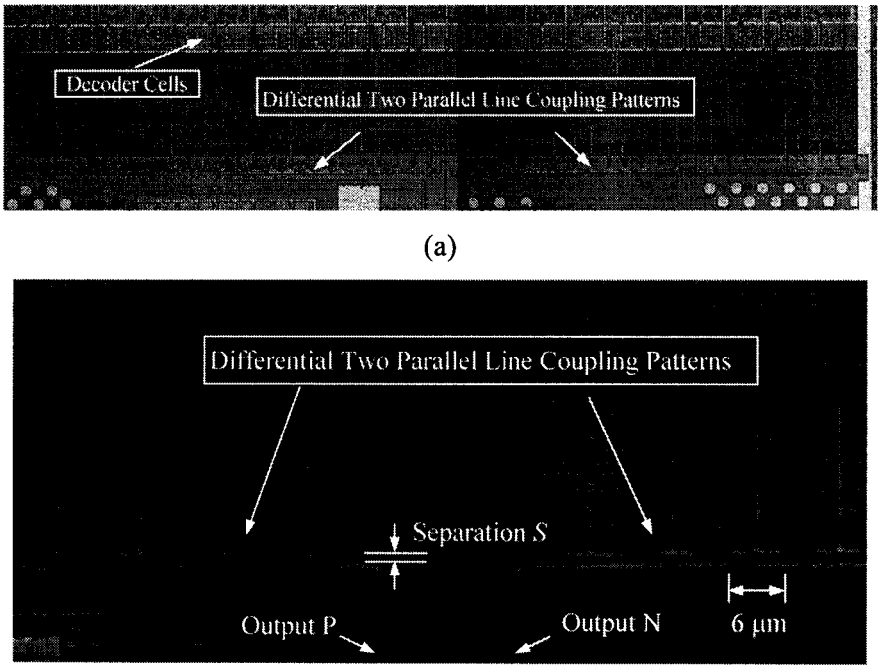


Figure 10-15: Microphotographs of (a) capacitive coupling circuit structures (b) detailed view of differential two-parallel-line coupling structures

The line-to-line coupling capacitance for three different metal layers is measured and compared to those values determined from the Sakurai and Tamaru model [77] and shown in Fig. 10-16. The difference between the experimental and analytic capacitances is 8.5%, 12.6%, and 17.7% for metal 1, metal 2, and metal 3, respectively. The error is due to the assumption that the length of a line in the Sakurai and Tamaru model is assumed infinite. In deep submicrometer ICs,

however, coupling between short lines can no longer be ignored. The unit capacitance for short lines can also not be considered as constant due to edge effects [122]. Note that in other line-to-line capacitive coupling models, *e.g.*, Chang [75], Elmasry [76], Mejis and Fokkema [79], and Yuan and Trick [78], the edge effect is also not considered. The line-to-line capacitive coupling test technique presented in this paper can be useful for measuring and modeling the coupling capacitance between short lines in deep submicrometer ICs.

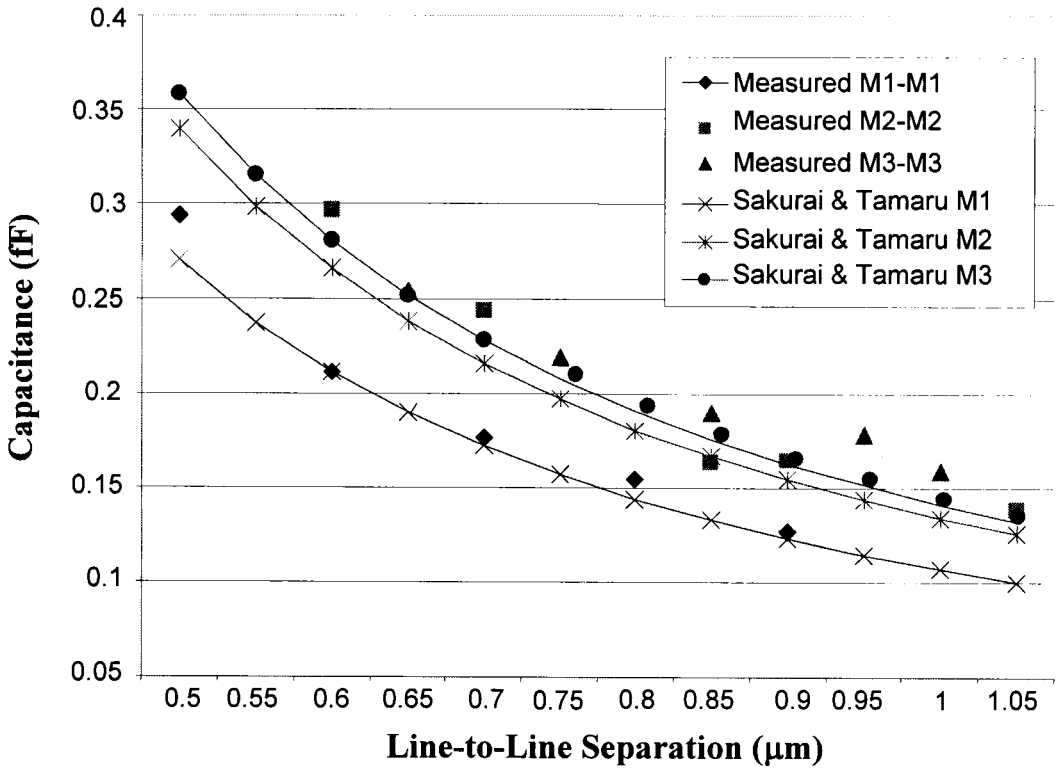


Figure 10-16: Comparison of measured and analytic line-to-line coupling capacitance

10.5. Summary

A specialized test circuit has been developed to directly measure substrate and line coupling noise, which consists of noise generators and signal processing circuitry. On-chip ADC and calibration are used to eliminate off-chip noise and to extend the measurement accuracy. A scan circuit is described that enables reconstruction of the noise waveform. Based on test data, noise generators of size 1 μm^2, 2 μm^2, 4 μm^2, and 6 μm^2 produce peak-to-peak substrate noise voltages that decrease as a function of distance and are 3.14 mV/μm, 3.08 mV/μm, 1.98 mV/μm, and 0.73 mV/μm, respectively, for a standard CMOS substrate. Open and closed guard rings are shown to reduce the substrate noise by 20% and 85%, respectively. The difference between experimental and analytic models of the line-to-line coupling capacitance ranges from 8.5% to 17.7% for different metal layers.

Chapter Eleven: Conclusions

The complexity of integrated circuits will continue to increase in both component count and functionality. Driven by market demands and the availability of powerful technologies, systems-on-a-chip will become commonplace for a wide range of applications. More ICs have both digital and analog circuits integrated on the same substrate. With developments in process, circuit design, and IC layout, small noise sources such as substrate coupling and line-to-line capacitive coupling are becoming serious problems. In certain applications, these sources of coupling noise may greatly degrade circuit performance as well as product yield. To deal with these problems, substrate and electromagnetic coupling noise will need to be carefully evaluated and experimentally characterized.

The primary focus of this research effort is the study of substrate and capacitive coupling noise in mixed-signal integrated circuits in order to develop a technique for accurately measuring coupling noise, and to use this technique as a tool for future study. The ultimate objective of this research effort is the development of accurate and efficient substrate coupling and capacitive coupling models for submicrometer mixed-signal IC design and characterization.

11.1. Measuring Substrate Coupling Noise

Substrate coupling has been known for a long time to be a source of significant noise. The capability for accurately and efficiently simulating substrate coupling noise remains difficult to integrate into the IC design process. Certain substrate models have been incorporated into CAD tools. The results of these simulations are primarily used as a reference and for preliminary design.

In this dissertation, the substrate coupling test technique has been successfully designed and manufactured in a 0.35 μm CMOS process. The objective is to determine the relation between substrate coupling noise and physical parameters such as the size of the noise generators, and the distance between the noise generators and noise receivers. A number of test structures have been designed, manufactured, and measured. The experimental data show that small noise voltages such as substrate coupling voltages can be accurately measured. The waveforms of the substrate coupling noise voltages have also been reconstructed from multi-point test results. It is shown that the substrate coupling noise waveforms exhibit a large damping factor; the amplitude of the waveforms quickly attenuates, diminishing in about 20 ns for a typical CMOS process. The measured data also show the nonlinear relationship between the size of the noise generator and the substrate noise voltage. A total of 21 substrate coupling noise test structures have been measured. For each test structure, the substrate coupling voltage waveform has been reconstructed from 32 test points. The substrate coupling and capacitive

coupling noise test techniques have been developed as an initial step towards developing accurate substrate and capacitive coupling models.

From this research, the reduction in substrate coupling noise due to the guard rings is evaluated from the measurement data. The test results indicate that the open loop guard rings have a limited effect on reducing the substrate coupling noise. For the 0.7 μm wide grounded N^+ open loop guard ring studied here, about 80% of the substrate coupling noise can pass the open guard ring to reach the receiver (the victim) as compared with the same noise generator without a guard ring. The reduction in noise is about 20% for this open loop, guard ring test structure. The measurement data also demonstrate that the closed ring can not completely isolate the substrate coupling noise. For a single 0.7 μm wide grounded closed N^+ guard ring, the reduction in the substrate coupling noise voltage is around 85%. Multiple-loop guard rings are suggested for more effectively reducing substrate coupling noise.

11.2. Measuring Capacitive Coupling Noise

Capacitive coupling between on-chip conductive lines has become a serious problem with technology scaling and the advent of mixed-signal ICs. Coupling from short lines may produce significant errors. Accurately simulating line-to-line capacitive coupling is already an important issue in existing IC design processes.

Based on the assumption of a constant unit capacitance, most capacitive coupling models are only accurate for long conductive lines. With technology scaling, the line-to-line spacing has become smaller and therefore capacitive coupling between short lines can no longer be ignored. For many applications, capacitive coupling between neighboring short lines to sensitive analog nodes may generate large errors at the circuit output, severely affecting circuit performance, circuit stability, and product yield. One focus of this research effort is to determine the coupling capacitance between these short lines so as to support the development of an accurate model for line-to-line capacitive coupling. Such a coupling capacitance model will be a function of line length and be accurate for both long and short lines.

A capacitive coupling test technique has been developed as part of this research dissertation. This test circuit has been successfully designed, manufactured, and tested. Twentyone short line coupling structures have been measured. Capacitive coupling voltages between two parallel lines on the same layers (three different metal layers) have been measured, permitting the coupling capacitance to be determined. All of the lines in the test structures are 6 μm long and 0.5 μm in width. The space between the two parallel lines ranges from 0.1 μm to 1 μm. Due to physical space limitations, different length coupling pairs (the test structures on the test circuit are all the same length) have not been included on the test circuits and the variation in the unit capacitance versus the length of the short coupling

lines has not been evaluated. The measured coupling capacitance between two conductive lines has been compared to the Sakurai and Tamaru model and the difference is found to be in the range of 10% to 17%.

Chapter Twelve: Future Work

The semiconductor industry is progressing at a fast pace in both process development and the development of related IC design methodologies. Many current ICs are fabricated in CMOS technologies ranging from 0.25 μm to 0.13 μm on 8″ wafers. Many of these ICs are mixed-signal. The share of mixed-signal ICs in the total IC market is rapidly increasing. In the author's opinion, in the near future almost all ICs will be mixed-signal.

Substrate coupling noise and capacitive coupling noise are two of the primary noise sources in high speed mixed-signal ICs. These noise sources have become primary challenges and require the development of accurate substrate coupling and capacitive coupling models in order to reduce the design-to-market time and to improve product performance and yield.

Novel substrate coupling and capacitor coupling test techniques have been successfully developed as described in this dissertation. Experimental data show that low level noise voltages such as substrate coupling and capacitive coupling noise voltages can be accurately measured. The nature of substrate coupling noise has been studied from these measurement results. Reducing substrate noise with the use of guard rings has also been evaluated. Capacitive coupling between conductive lines has been measured from test circuits. The coupling capacitance is determined

from the measured coupling voltages based on the formula described in Chapter 4 and compared with the Sakurai and Tamaru model [77].

Substrate coupling is currently not included in most IC design flows due to the lack of an accurate and efficient substrate coupling model and sufficient understanding about the mechanisms that produce substrate coupling. Many coupling capacitance models have been developed during recent years and are widely used in parasitic extraction CAD tools. All of these coupling capacitance models, however, calculate the unit capacitance by assuming the line length is infinitely long. The unit line-to-line coupling capacitance is therefore independent of the length of the coupled lines in these coupling capacitance models. In submicrometer processes, such assumptions for many cases are no longer valid. Coupling between short lines can cause serious problems in current high speed, low power integrated circuits. Under such conditions, the unit coupling capacitance of a short line is a function of the length of the line. The development of a line-to-line fringing coupling capacitance model which considers the length of the lines is required for accurate circuit simulation and layout optimization.

Two approaches can be employed to address these problems: applying circuit concepts to analytically develop models calibrated with experiment data, and develop models from experimental data and correlate this data with curve fitting methods. In both case, accurate noise measurement techniques are necessary. Currently, most substrate coupling noise models are developed based on the first

approach. In this dissertation, the second approach is used. Possible future work could include: a) the development of enhanced substrate coupling models where the substrate is treated as a separate electrical device or component; and b) the development of enhanced line-to-line capacitive coupling models which are characterized in terms of a unit capacitance as a function of the length of the coupling lines. Furthermore, in order to develop accurate models for substrate and capacitive coupling, more complex coupling structures should be developed and evaluated on test circuits.

In section 12.1, the substrate coupling test circuit is reviewed and suggestions for improvement are described. Modeling the effect of guard rings on reducing substrate noise is considered in section 12.2. The capacitive coupling test circuit which includes line-to-line coupling structures is discussed in section 12.3. The summary and conclusions of this chapter are provided in section 12.4.

12.1. Future Work on Modeling Substrate Coupling Noise

Future research on substrate coupling noise is focused on developing substrate coupling models based on more accurate experimental data. Due to the dependence of substrate coupling noise on the type of substrate, the development of a general substrate coupling model for different substrates requires the design and fabrication of test circuits on a wide variety of substrate types. In this section, modeling substrate coupling noise is limited to a standard CMOS process substrate (lightly

doped epi-layer on a thick low resistive substrate). The test techniques described in previous chapters are shown to be capable of accurately measuring substrate coupling noise. A modified substrate coupling noise test circuit is proposed for future research in substrate coupling noise.

12.1.1. Circuit Optimization

To achieve these research objectives, the on-chip analog-to-digital converter should be upgraded to 12-bits or higher resolution. The voltage gain of the integrator circuit should also be further reduced for longer integration time. Additional clock cycles can therefore be considered in the signal processing step when measuring noise. The random noise in the system will be better averaged out of the substrate coupling noise. An on-chip band-gap voltage generator is required to generate the common-mode reference voltage and the differential reference so that the noise in the reference voltages is cancelled out during the differential analog signal processing.

The addition of a more complicated digital timing circuit is also necessary so that the test system can automatically measure all of the substrate coupling noise generators in a specific sequence by transmitting the addresses to the two decoders (to replace the two switch arrays on the test board as shown in Fig. E.1 of Appendix E.) The timing block also performs the system calibration immediately after the substrate coupling test is completed. The noise in the raw data and calibration data will be better correlated and, therefore, additional system noise will

be removed from the measured data during the calibration process. A block diagram of the proposed circuit is shown in Fig. 12-1.

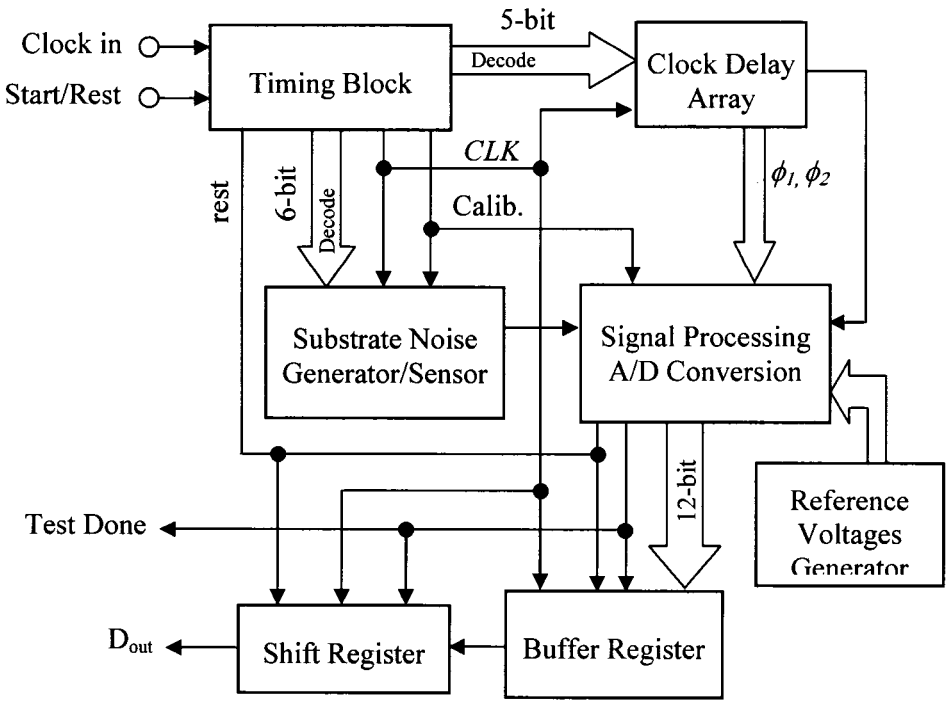


Figure 12-1: Block diagram of the proposed substrate noise waveform measuring circuit

12.1.2. Noise Generator Matrix

For a specific substrate type, the substrate coupling noise depends upon the size A of the noise generator, space S between the noise generator and the receiver, and the voltage swing of the noise generating signals. To develop a substrate coupling noise model from the experimental data, different combinations of size and space characterizing the noise generator and receiver pairs should be carefully selected

and designed. A set of possible combinations of noise generator and receiver pairs is listed in Table 12.1

12.1.3. Physical Design of the Noise Generator Matrix

To effectively use the receiver and the analog processing circuit, additional noise generators should be placed around the receiver. However, due to space limitations and to reduce the routing complexity of the decoder, only a limited number of noise generators should be placed near the receiver. A 64 noise generator array example is considered here. Each receiver senses 64 substrate coupling noise generators as listed in Table 12.1. The generators are composed of N^+ squares, each sized 0.25 μm^2. An example of the physical floorplan of a noise generating array within the substrate coupling noise test circuit is shown in Fig. 12-2.

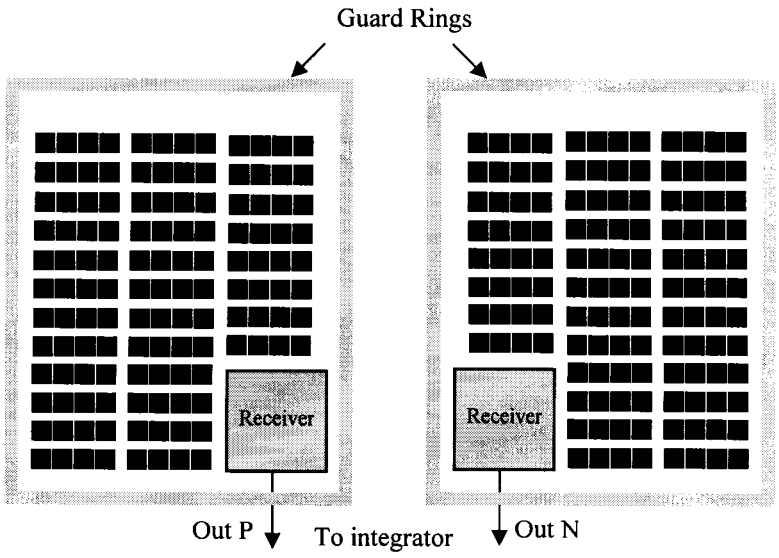


Figure 12-2: Proposed floorplan of a substrate coupling noise generator/receiver circuit

Table 12-2: Matrix of substrate coupling noise generators

$A(\mu m^2)$ / $S(\mu m)$	0.25	0.5	0.75	1	1.25	1.5	1.75	2	2.25	2.5	2.75	3	3.25	3.5	3.75	4
0.5	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14	#15	#16
0.75	#17	#18	#19	#20	#21	#22	#23	#24	#25	#26	#27	#28	#29	#30	#31	#32
1	#33	#34	#35	#36	#37	#38	#39	#40	#41	#42	#43	#44	#45	#46	#47	#48
1.25	#49	#50	#51	#52	#53	#54	#55	#56	#57	#58	#59	#60	#61	#62	#63	#64
1.5	#65	#66	#67	#68	#69	#70	#71	#72	#73	#74	#75	#76	#77	#78	#79	#80
2.5	#81	#82	#83	#84	#85	#85	#87	#88	#89	#90	#91	#92	#93	#94	#95	#96
3.5	#97	#98	#99	#100	#101	#102	#103	#104	#105	#106	#107	#108	#109	#110	#111	#112
5.5	#113	#114	#115	#116	#117	#118	#119	#120	#121	#122	#123	#124	#125	#126	#127	#128
7.5	#129	#130	#131	#132	#133	#134	#135	#136	#137	#138	#139	#140	#141	#142	#143	#144
11.5	#145	#146	#147	#148	#149	#150	#151	#152	#153	#154	#155	#156	#157	#158	#159	#160
15.5	#161	#162	#163	#164	#165	#166	#167	#168	#169	#170	#171	#172	#173	#174	#175	#176
19.5	#177	#178	#179	#180	#181	#182	#183	#184	#185	#186	#187	#188	#189	#190	#191	#192
27.5	#193	#194	#195	#196	#197	#198	#199	#200	#201	#202	#203	#204	#205	#206	#207	#208
35.5	#209	#210	#211	#212	#213	#214	#215	#216	#217	#218	#219	#220	#221	#222	#223	#224
43.5	#225	#226	#227	#228	#229	#230	#231	#232	#233	#234	#245	#236	#237	#238	#239	#240
53.5	#241	#242	#243	#244	#245	#246	#247	#248	#249	#250	#251	#252	#253	#254	#255	#256
63.5	#257	#258	#259	#260	#261	#262	#263	#264	#265	#266	#267	#268	#269	#270	#271	#272

Note: # indicates the number of the substrate noise generator within the noise generator array.

12.2. Substrate Coupling Noise Guard Rings

Guard rings are a popular way to reduce substrate coupling noise. Guard rings are commonly used when analog and digital circuits are integrated on the same substrate. The silicon space occupied by these guard rings is expected to increase rapidly. The size of the substrate noise guard ring structure is important to improve circuit performance and reduce cost. Possible future research is evaluating the efficiency of different substrate guard rings.

The research results presented in Chapter 10 show that about 85% of the substrate coupling noise can be reduced with a minimize size single loop guard ring. However, less than a 20% reduction in noise (as compared with the received noise without guard rings) can be achieved with open loop guard rings. A substrate coupling noise of 7 mV is detected at the receiver output, a level often unacceptable in many analog applications. Single loop guard rings do not provide a sufficient reduction in noise and are therefore not useful when low noise is required. To further understand and model the noise reduction mechanism in guard rings, double-loop, triple-loop, $N^+P^+N^+$, and $N^+P^+N^+$ structured guard rings should be developed and tested.

In order to determine the most efficient guard ring structures to reduce substrate coupling noise, a family of guard rings should be designed, manufactured, tested, and compared. The test structures should include guard rings with different widths,

different combinations of N^+ and P^+ rings, and various distances between the guard ring and noise receiver. The investigation should include:

- single N^+ or P^+ rings with different widths
- double N^+P^+ and N^+P^+ rings with minimum and larger widths
- triple minimum width $N^+P^+N^+$ and $P^+N^+P^+$ rings
- single guard rings placed at different distances from the noise receiver (from the minimum allowable space to several micrometers)

12.3. Future Work on Modeling Line-to-Line Capacitive Coupling

Line-to-line capacitive coupling can exist between digital and analog lines and also among multiple analog (and digital) lines. For short lines, the coupling capacitance is no longer a linear function of the length of the coupled lines. The technique described in Chapter 4 exhibits good results in measuring the line-to-line coupling capacitance. In this section, the development of a line-to-line coupling capacitance model applicable for any coupling line length is proposed.

As discussed in previous sections, a test circuit should be optimized by modifying both the analog circuits and digital control blocks. Potentially fruitful research is the development of models that characterize two-parallel-line coupling structures for a variety of lengths L, different metal layers, different space S between two lines, and different width W of the coupled lines.

12.4 Conclusions

Accurate substrate and capacitive coupling models are required in the design of high performance ICs. Suggested areas for possible research are the development of models from experimental data. The proposed research objective is the development of an accurate and computationally efficient substrate coupling noise model which permits the substrate to be treated as a two terminal device between the noise generator and receiver. Substrate noise guard rings should also be further investigated to improve circuit performance and reduce cost. An accurate line-to-line coupling capacitance model that characterizes short lines should also be developed and compared with data extracted from test circuits, so as to provide an accurate coupling capacitance model for short coupled lines.

References

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Appendix A: Random Noise Theorems

A.1. Energy Theorem

For a noise process, the power is a second order statistical property. It is convenient to discuss noise in term of Parseval's theorem or the energy theorem. For a noise process xT(t),

$$\int_{-\infty}^{+\infty}[x_T(t)]^2 = (1/2\pi)\int_{-\infty}^{+\infty}|X_T(j\omega)|^2 d\omega \quad . \tag{A.1}$$

Each side of (A.1) equals the total energy in xT(t) and |XT(jw)|2, respectively, and can be explained as the energy density of the process with units of energy per Hertz. For a finite T, the average power in the noise process is the total energy divided by T. The power spectral density of the stationary noise process xT(t) is defined as the ensemble average,

$$\overline{S_x(\omega)} = \lim_{T\to\infty}\frac{2\overline{|X_T(j\omega)|}^2}{T} \quad , \tag{A.2}$$

which converges to a specific value. The power spectral density of a stationary noise process is thus expressed as a property of the whole ensemble, not as a property of an individual member of the ensemble.

A2. Random Pulse Train

Random noise often occurs in a large number of independent discrete events. Each event produces a pulse with a certain shape, and the random composition of all such pulses constitutes the noise waveform. Such a waveform is known as a random pulse train. Common noise sources in IC's, the shot noise and the thermal noise, can be treated as a random pulse train. If f(t) or an independent discrete event is a pulse-shape function, the noise waveform is

$$x(t) = \sum_{k=1}^{K} a_k f(t - t_k) \quad , \tag{A.3}$$

where ak is the amplitude of the kth pulse, and tk is the time at which the kth event occurs. K is the number of pulses in a train of duration T, and causality requires that f(t) = 0 when t < 0.

The Fourier transform of x(t) is

$$X(j\omega) = \sum_{k=1}^{K} \{a_k \exp-(j\omega t_k) F(j\omega)\} \quad . \tag{A.4}$$

According to (A.3), the power spectral density of x(t) is

$$\overline{S_x(\omega)} = \lim_{T\to\infty} \frac{2\overline{|F(j\omega)|}^2}{T} \sum_{k,m=1}^{K} \overline{a_k a_m \exp- j\omega(t_k - t_m)} \quad . \tag{A.5}$$

The summation in (A.5) can be expressed as a sum over terms with $k = m$ plus a double sum of terms with $k \neq m$, allowing the power spectral density to be written as

$$\overline{S_x(\omega)} = \lim_{T\to\infty} \frac{2\overline{|F(j\omega)|}^2}{T} \left\{ \sum_{k=1}^{K} \overline{a_k^2} + \sum_{k,m=1}^{K} \overline{a_k a_m \exp - j\omega(t_k - t_m)} \right\} \quad , \qquad (A.6)$$

where the prime indicates $k \neq m$. For a symmetrical distribution of a_k about zero, the power spectral density is

$$\overline{S_x(\omega)} = \frac{2}{T} \overline{a^2} |F(j\omega)|^2 \quad , \qquad (A.7)$$

where $\overline{a^2}$ is the mean-square value of the $\overline{a_k a_m}$.

A.3. Wiener-Khintchine Theorem

A stationary random process is an infinite energy signal and hence the related Fourier transform does not exist. For a well behaved stationary random process, the power spectrum is equal to the Fourier transform of the autocorrelation function. The time average of the product of x(t) with the delayed version x(t+τ) is defined as the autocorrelation function of x(t)

$$C_x(\tau) = \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} x(t)x(t+\tau)dt = \frac{1}{T} \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} \int_{-\frac{T}{2}}^{\frac{T}{2}} d\omega \cdot d\omega' \cdot X_T(\omega) X_T(\omega') e^{j(\omega+\omega')t} e^{j\omega\tau} dt \quad . \qquad (A.8)$$

The function Cx(t) is the autocorrelation function of x(t).

When $T \to \infty$,

$$\lim_{T\to\infty} \int e^{j(\omega+\omega')t} dt = 2\pi\delta(\omega+\omega') \quad , \tag{A.9}$$

such that

$$C_x(\tau) = \lim_{T\to\infty} \frac{1}{2} \int_{-\infty}^{\infty} \frac{4\pi|X_T(\omega)|^2}{T} e^{j\omega t} d\omega \quad . \tag{A.10}$$

The quantity $4\pi|X_T(\omega)|^2 / T$ is the spectral density function Sx(ω) of x(t), such that

$$C_x(\tau) = \frac{1}{2} \int_{-\infty}^{\infty} S_x(\omega) e^{j\omega t} d\omega \quad , \tag{A.11}$$

and

$$S_x(\omega) = \frac{1}{\pi} \int_{-\infty}^{\infty} C_x(t) e^{-j\omega t} dt \quad . \tag{A.12}$$

The spectral density function Sx(ω) and the autocorrelation function Cx(τ) form a Fourier transform pair.

Appendix B: Formulas of the Line-to-Line Coupling Capacitance

Many models have been developed for on-chip line-to-line capacitive coupling. Some of the most widely used models are listed below. A comparison of these models is summarized in Fig. B-1 at the end of this appendix.

B.1. Chang Formula [75]

$$\begin{aligned} C &= \frac{2\varepsilon}{\pi}\ln\left(\frac{2R_b}{R_a}\right) \\ &= \frac{2\varepsilon}{\pi}\left(1+\frac{\pi W}{2H}+\left(\frac{P+1}{\sqrt{P}}\right)\tanh^{-1}\left(\sqrt{P}\right)+\ln\left(\frac{2\eta(P-1)+\left(P^2-1\right)\ln(\Delta)}{4P}\right)\right) \quad , \\ R_b &= \eta+\frac{P+1}{2}\ln\Delta \quad , \end{aligned} \tag{B.1}$$

where

$$\eta = \sqrt{P}\left[\frac{\pi W}{2H}+\frac{P+1}{2\sqrt{P}}\cdot\frac{P-1+\ln 4}{P-1}-2\tanh^{-1}\left(\sqrt{P}\right)\right] \quad ,$$

$$P = 2\left(1+\frac{T}{H}\right)^2-1+\sqrt{\left[2\left(1+\frac{T}{H}\right)^2-1\right]^2-1} \quad .$$

Δ is the larger of η or P. Provided $W/H \geq 5$ and $1 \leq T/H \leq 5$,

$$R_b(new) = R_b - \sqrt{(R_b - 1)(R_b - P)} + (P+1)\tanh^{-1}\left(\sqrt{\frac{R_b - P}{R_b - 1}}\right) - 2\sqrt{P}\tanh^{-1}\left(\sqrt{\frac{R_b - P}{B(R_b - 1)}}\right) + \frac{\pi W}{2H\sqrt{P}} \quad . \tag{B.2}$$

B.2. Elmasry's Formula [76]

$$C = \varepsilon\left[\frac{W}{H} + 2\ln\left(1 + \frac{T}{H}\right) + \frac{2T}{H}\ln\left(1 + \frac{W/2}{T+H}\right)\right], \tag{B.3}$$

provided W/H = 1.

The first term in (B.3) describes the parallel plate capacitance, the second term describes the side capacitance, and the third term describes the top plate capacitance.

B.3. Yuan and Trick Formula [78]

$$C = \varepsilon\left[\frac{W - T/2}{H} + \frac{2\pi}{\ln\left(1 + \frac{2\pi}{T}\right) + \sqrt{\frac{2\pi}{T}\left(2 + \frac{2H}{T}\right)}}\right], \tag{B.4}$$

provided $0.3 \le W/H \le 30$ and $0.3 \le T/H \le 30$. The first term in (B.4) describes the parallel plate capacitance, and the second term describes the side wall capacitance.

B.4. Meijs and Fokkema Formula [79]

$$C = \varepsilon\left[\left(\frac{W}{H}\right) + 0.77 + 1.06\left(\frac{W}{H}\right)^{0.25} + 1.06\left(\frac{T}{H}\right)^{0.5}\right], \tag{B.5}$$

provided $W/H \geq 1$ and $0.3 \leq T/H \leq 4$. In (B.5) the first term describes the parallel plate capacitance, and the second, third, and fourth terms describe the side wall capacitance.

Comparison

The Chang formula is the most complicated expression of the all four mentioned expressions and has the highest accuracy. Barke [120] evaluated these capacitive coupling formulas relative to the Chang formula. The relative computational efficiency is illustrated in Fig. B-1. According to Barke's comparison, the Meijs/Fokkema formula is superior to the other expressions in terms of accuracy. Over a wide width range, the accuracy of the Meijs/Fokkema formula is within 1% as compared to the Chang formula. The Sakurai formula yields better results for smaller line sizes. The Yuan formula is useful for a larger W/H ratio, but is not effective when W/H is smaller than three.

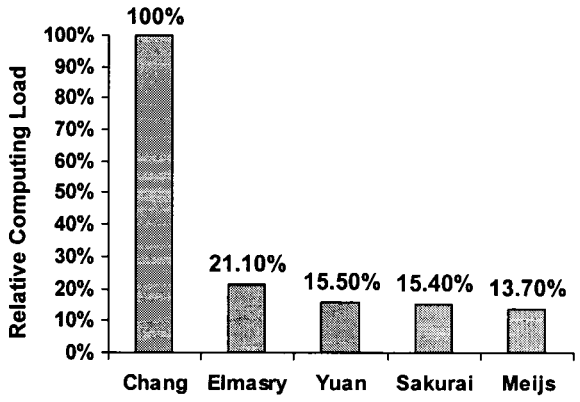

Figure B-1: Comparison of different capacitive coupling models

Appendix C: On-Chip Coupling Noise Test Patterns

The noise generators in the substrate coupling array within the substrate coupling noise test circuits described in Chapters 4, 5, and 10 are listed in Tables C.1 and C.2. The parallel line capacitive coupling structures used in the capacitive coupling test circuit are listed in Table C.3. The physical layout of the noise generators from the substrate coupling noise test circuit II is shown in Fig. C-1.

Table C-1: Noise generators of the substrate coupling noise test circuit I.

Generator #	Size (μm^2)	Distance from the Sensor (μm)
1	0.5	1.0
2	0.5	2.5
3	0.5	5.0
4	0.5	6.5
5	0.25	5.0
6	0.25	6.5
7	1.5	20
8	1.5	15
9	1.5	10
10	1.5	5.0
11	0.25	4.0
12	0.25	2.5
13	1	2.0
14	1	4.0
15	1	5.0
16	1	10
17	1	15
18	1	20
19	1	2.8
20	2	3.5 *

* With a grounded N^+ line between the noise generator and the receiver

Table C-2: Noise generators within the substrate coupling noise test circuit II

Generator #	Size (μm^2)	Distance from the Receiver (μm)	Guard Ring
1	4	2.2	# 1
2	8	2.2	# 1
3	4	3.8	# 2
4	8	3.8	# 2
5	4	4.3	# 3
6	8	4.3	# 3
7	4	7.8	# 4
8	8	7.8	# 4

Note: # indicates each individual ring as shown in Fig. C.1.

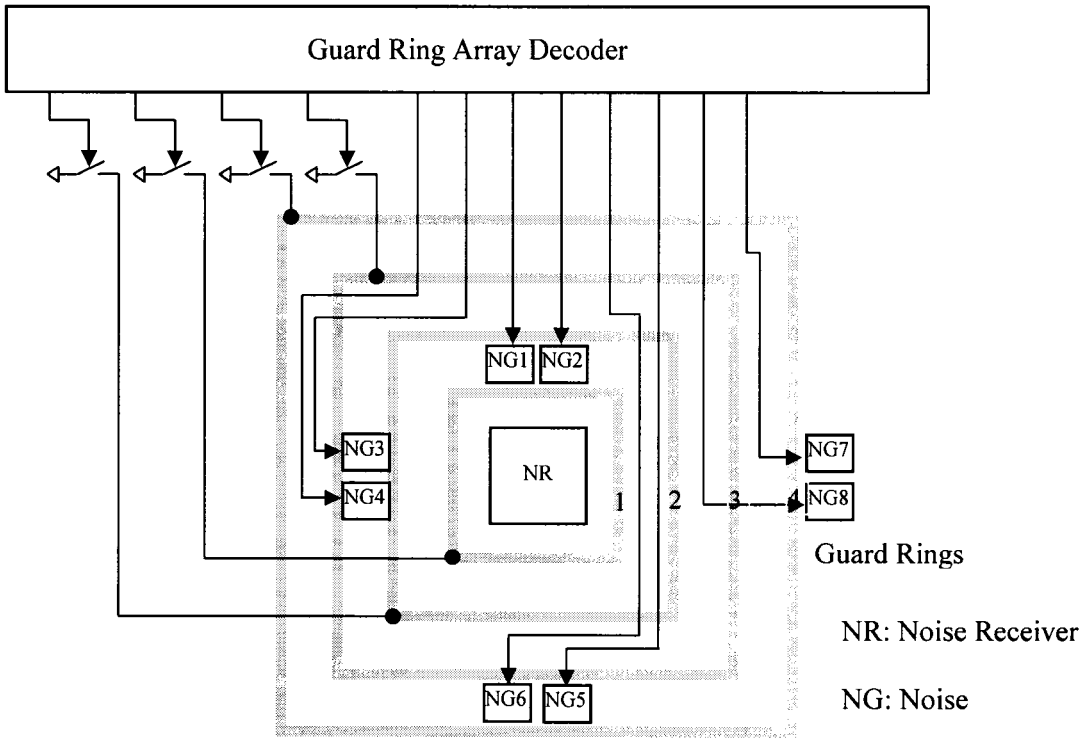

Figure C-1: Physical layout of the noise generators in substrate coupling noise test circuit II

Table C-3: List of the two-parallel-line capacitive coupling structures

Generator #	Metal Layer	Separation, S	Metal Layer Thickness, T	Metal to Substrate, H
1	Metal 1 to Metal 1	0.5 μm	0.62 μm	0.97 μm
2	Metal 1 to Metal 1	0.6 μm	0.62 μm	0.97 μm
3	Metal 1 to Metal 1	0.7 μm	0.62 μm	0.97 μm
4	Metal 1 to Metal 1	0.8 μm	0.62 μm	0.97 μm
5	Metal 1 to Metal 1	0.9 μm	0.62 μm	0.97 μm
6	Metal 1 to Metal 2	0.1 μm	–	–
7	Metal 1 to Metal 2	0.2 μm	–	–
8	Metal 1 to Metal 2	0.3 μm	–	–
9	Metal 1 to Metal 2	0.4 μm	–	–
10	Metal 1 to Metal 2	0.5 μm	–	–
11	Metal 1 to Metal 2	0.6 μm	–	–
12	Metal 2 to Metal 2	0.6 μm	0.65 μm	2.54 μm
13	Metal 2 to Metal 2	0.7 μm	0.65 μm	2.54 μm
14	Metal 2 to Metal 2	0.85 μm	0.65 μm	2.54 μm
15	Metal 2 to Metal 2	0.9 μm	0.65 μm	2.54 μm
16	Metal 2 to Metal 2	1.05 μm	0.65 μm	2.54 μm
17	Metal 3 to Metal 3	0.65 μm	0.67 μm	2.54 μm
18	Metal 3 to Metal 3	0.75 μm	0.67 μm	4.14 μm
19	Metal 3 to Metal 3	0.85 μm	0.67 μm	4.14 μm
20	Metal 3 to Metal 3	0.95 μm	0.67 μm	4.14 μm
21	Metal 3 to Metal 3	1.0 μm	0.67 μm	4.14 μm

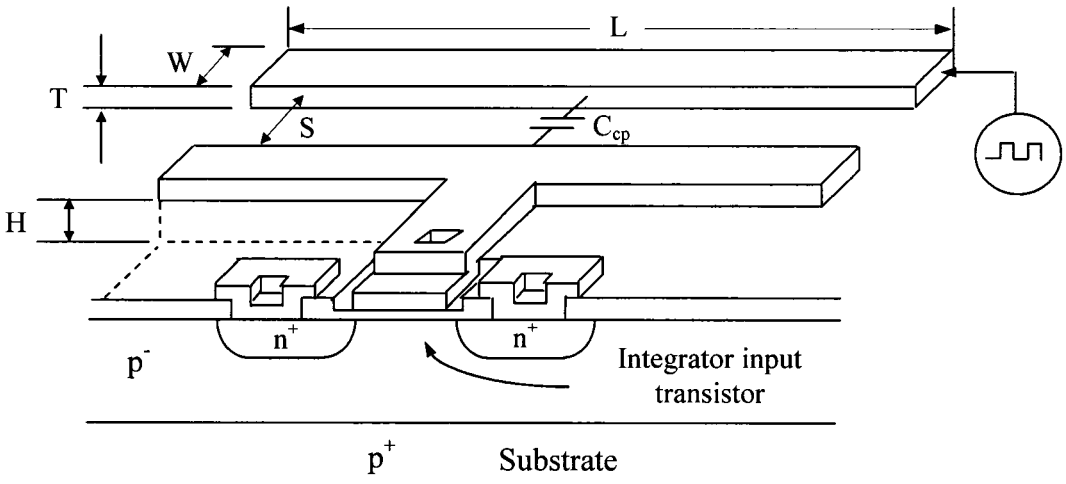

Figure C-2: The two-parallel-line capacitive coupling test structure

Appendix D: IC Package and Pin List

The circuits are packaged in a 84 pin ceramic pin grid array (CPGA) package. 36 of the 84 total pins are used. A drawing of the package is shown in Fig. D.1 and the test setup is displayed in Fig. D.2. Each pin of the test circuit is listed and described in Table D.1. A microphotograph of the packaged test circuit is shown in Fig. D.3.

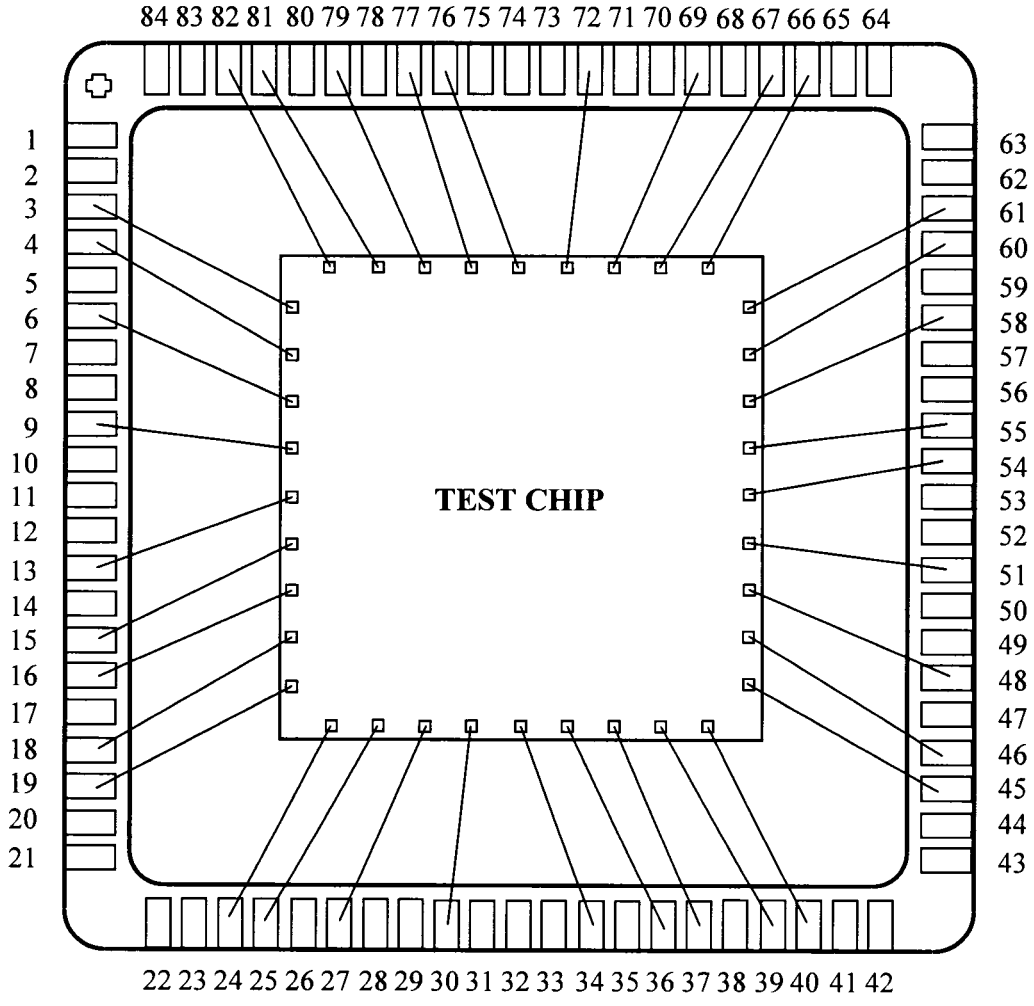

Figure D-1: Diagram of the 84-pin CPGA IC package

Table D-1: Descriptions of the 36 pin names of the test circuit

Pin #	Pin Name	Description	Comments
1	CAP_DONE2	Output, digital	Completion of the test for cap. test circuit 2 when it is
2	V_{dda}	Input, analog	Analog power supply voltage
3	CAP_DOUT1	Output, digital	Output test data of the cap. test circuit 1
4	CAP_DONE1	Output, digital	Completion of the test for cap. test circuit 2 when it is
5	V_{ss}	Input, analog	Digital ground
6	V_{CM}	Input, analog	Common mode voltage (DC) for the differential
7	V_{REFM}	Input, analog	"Minus" reference voltage
8	V_{REFP}	Input, analog	"Plus" reference voltage
9	V_{dda}	Input, analog	Analog power supply voltage
10	NGSEL_5	Input, digital	5^{th} bit of the noise generator selecting decode address
11	NGSEL_4	Input, digital	4^{th} bit of the noise generator selecting decode address
12	NGSEL_3	Input, digital	3^{rd} bit of the noise generator selecting decode address
13	NGSEL_2	Input, digital	2^{nd} bit of the noise generator selecting decode address
14	NGSEL_1	Input, digital	1^{st} bit of the noise generator selecting decode address
15	SUB_DOUT1	Output, digital	Output test data of the sub. test circuit 1
16	SUB_DONE1	Output, digital	Completion of the test for sub. test circuit 1 when it is
17	R_IN	Input, analog	External resistor input to set the bias current
18	CALIB	Input, digital	System calibration when it is set to "1"
19	V_{ss}	Input, analog	Digital ground
20	V_{dda}	Input, analog	Analog power supply voltage
21	EXT_NG_CLK	Input, digital	Ext. clock to operate the noise generator when pin 32 is
22	EXT_REC_CLK	Input, digital	Ext. clock to operate the ASP when pin 32 is "1"
23	DEL_SEL_1	Input, digital	1^{st} bit of the receiver clock delay selecting decode
24	DEL_SEL_2	Input, digital	2^{nd} bit of the receiver clock delay selecting decode
25	DEL_SEL_3	Input, digital	3^{rd} bit of the receiver clock delay selecting decode
26	DEL_SEL_4	Input, digital	4^{th} bit of the receiver clock delay selecting decode
27	DEL_SEL_5	Input, digital	5^{th} bit of the receiver clock delay selecting decode
28	REST_IN	Input, analog	System rest clock
29	V_{dda}	Input, analog	Analog power supply voltage
30	V_{ssa}	Input, analog	Analog ground
31	CLK	Input, digital	External master clock
32	EXT_CLK_SEL	Input, digital	Use external clocks to operate noise generator and
33	SUB_DOUT2	Output, digital	Output test data of the sub. test circuit 2
34	SUB_DONE2	Output, digital	Completion of the test for sub. test circuit 2 when it is
35	CAP_DOUT2	Output, digital	Output test data of the cap. test circuit 2
36	V_{dd}	Input, analog	Digital power supply voltage

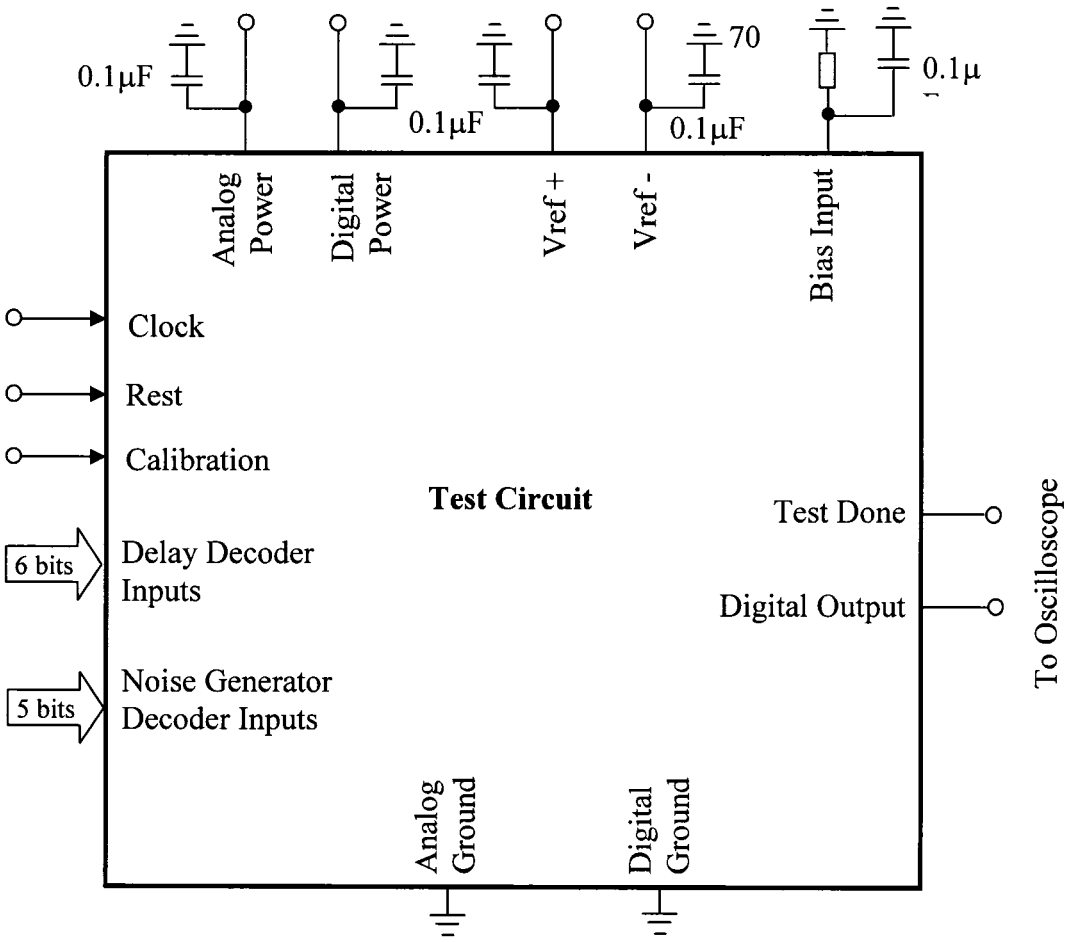

Figure D-2: I/O pin connections for circuit test setup

Figure D-3: Photograph of the packaged test circuit

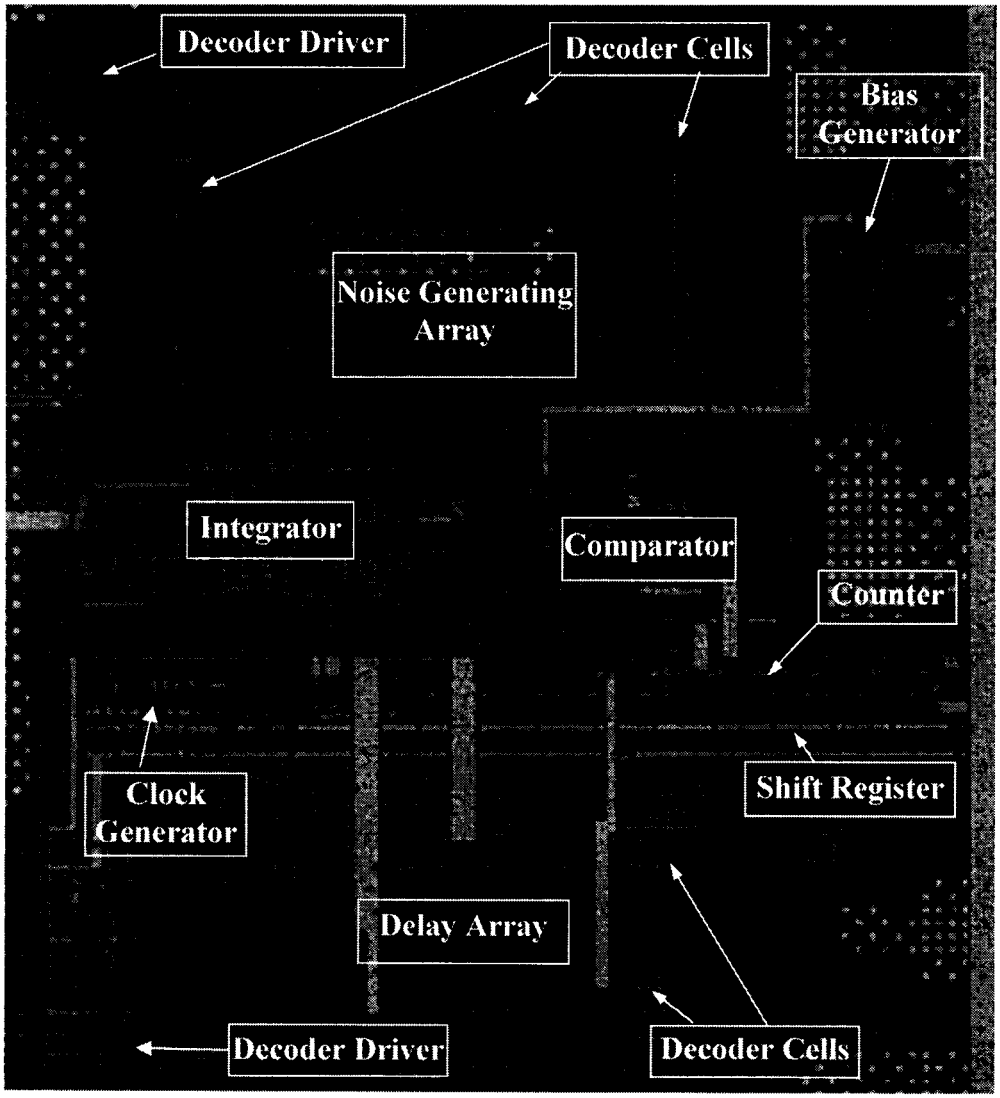

Figure D-4: Microphotograph of the substrate coupling noise test circuit I

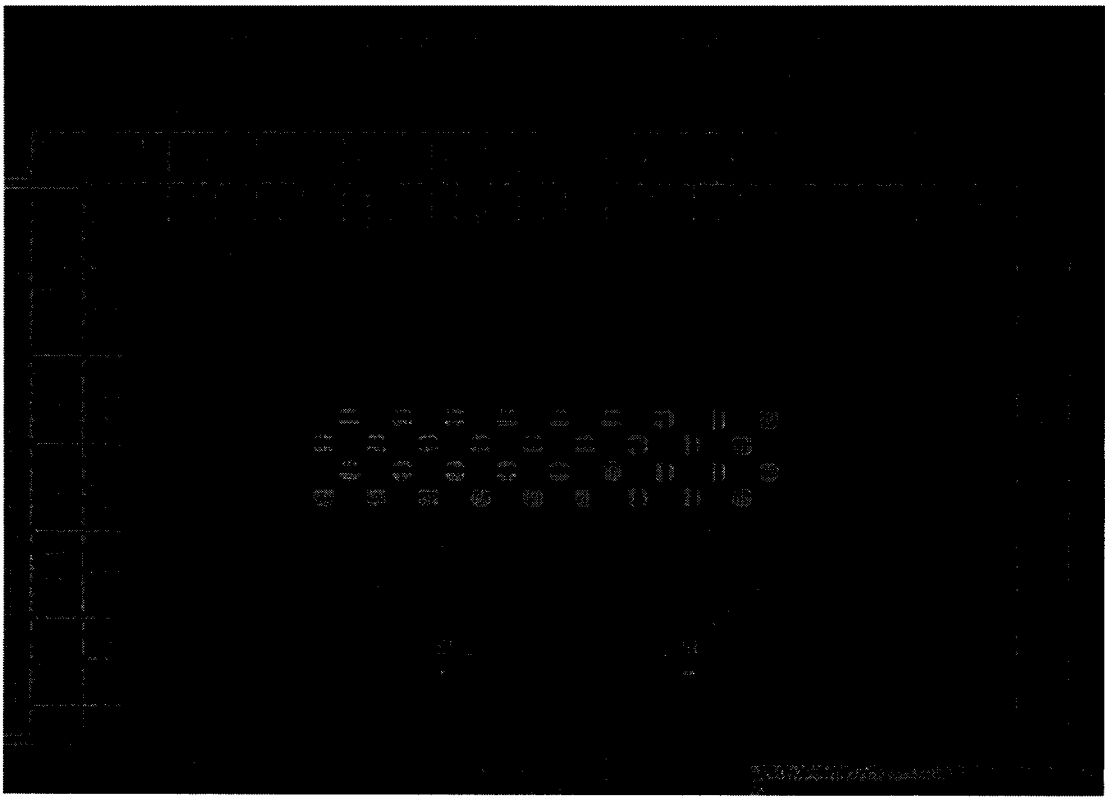

Figure D-5: Microphotograph of noise generating circuit within the substrate coupling noise test circuit I

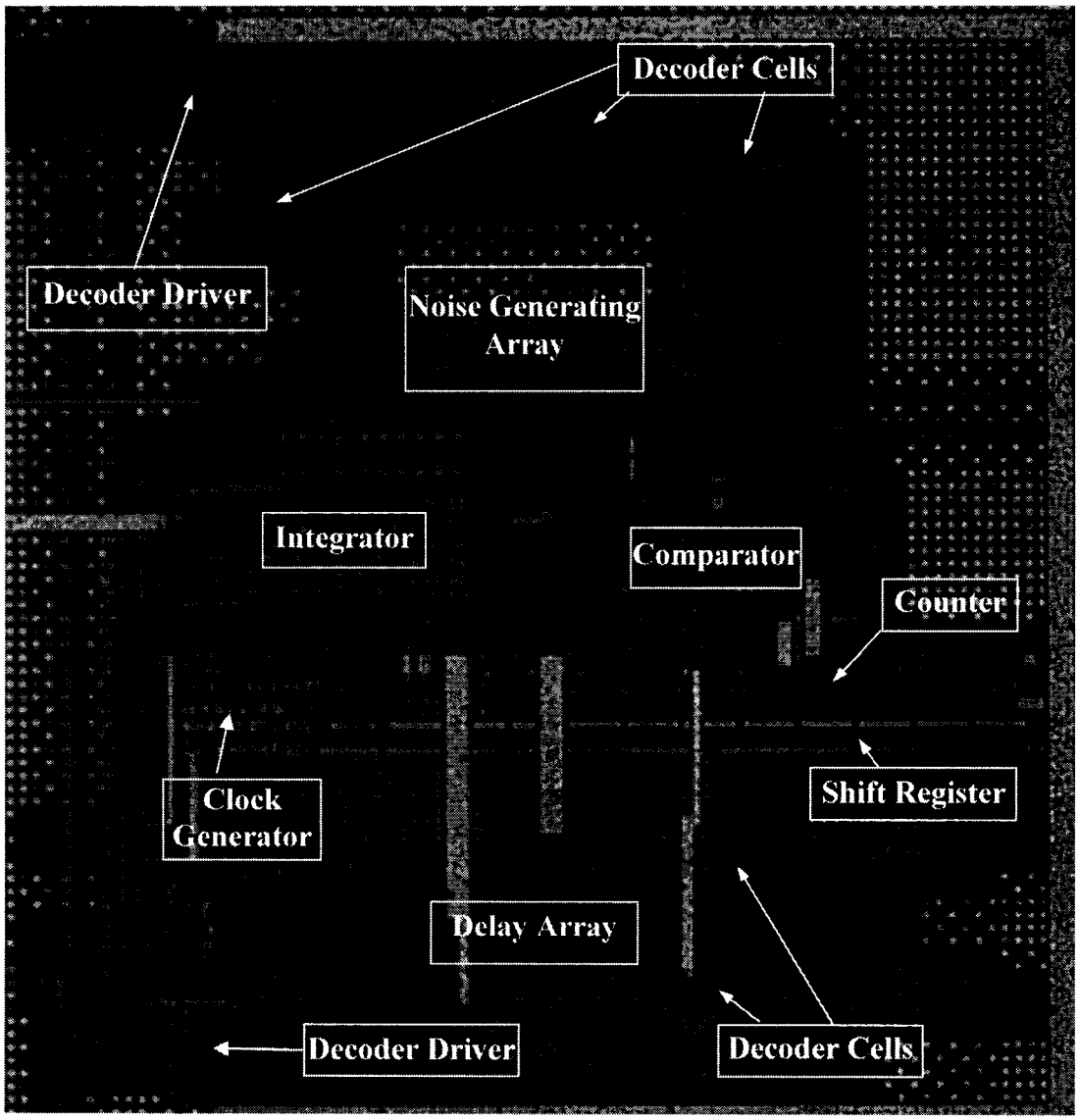

Figure D-6: Microphotograph of the substrate coupling noise test circuit II used to evaluate the reduction in noise caused by the guard rings

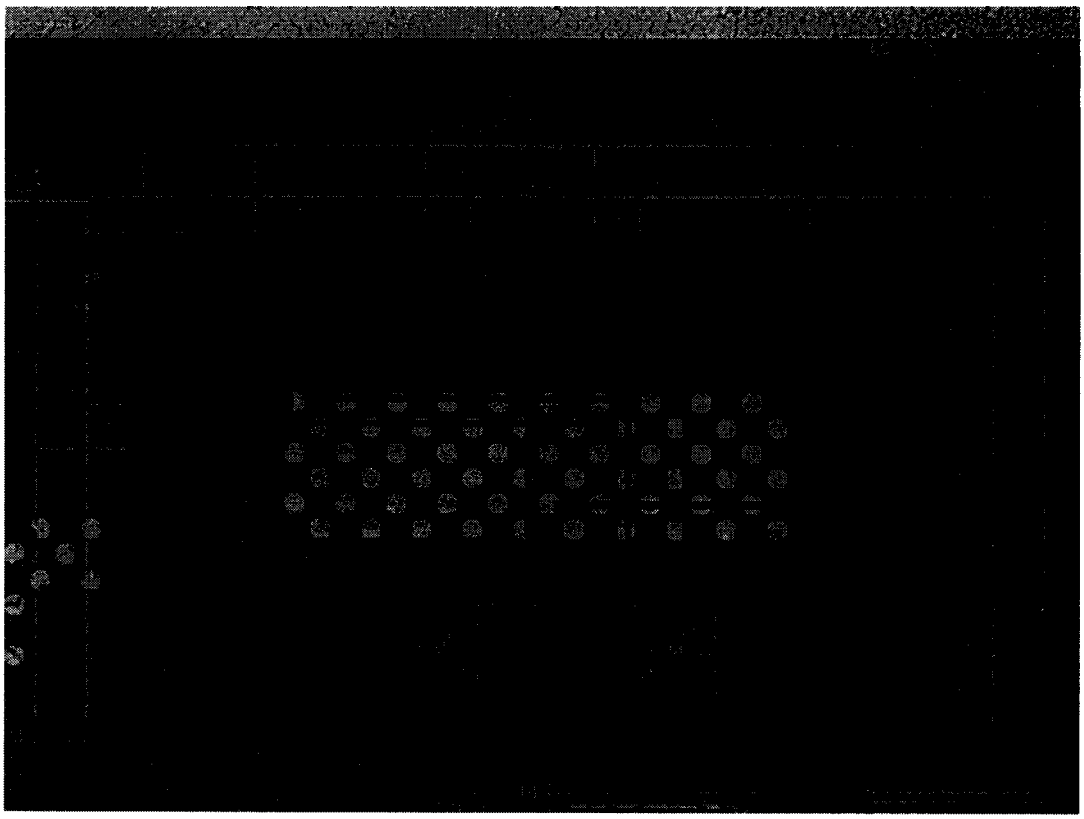

Figure D-7: Microphotograph of the noise generating circuit of the substrate coupling noise test circuit II

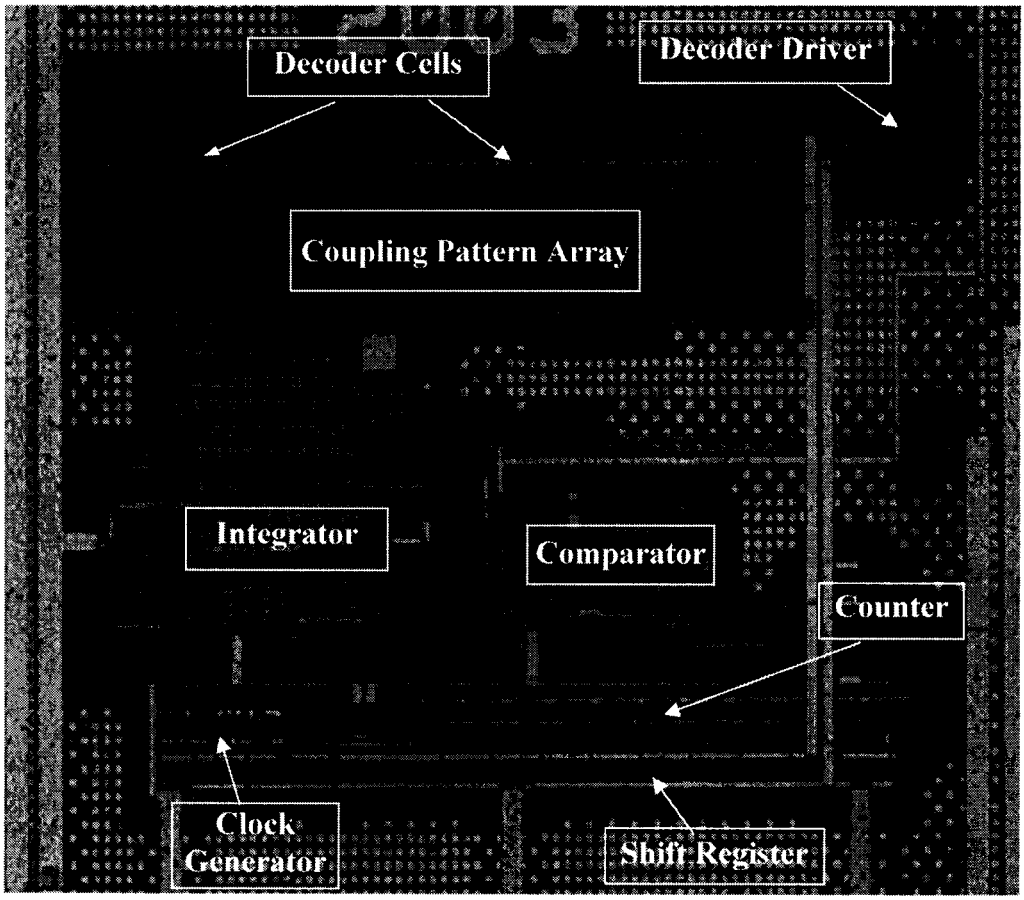

Figure D-8: Microphotograph of the capacitive coupling noise test circuit I

Figure D-9: Microphotograph of the integrator used in the substrate coupling noise test circuits

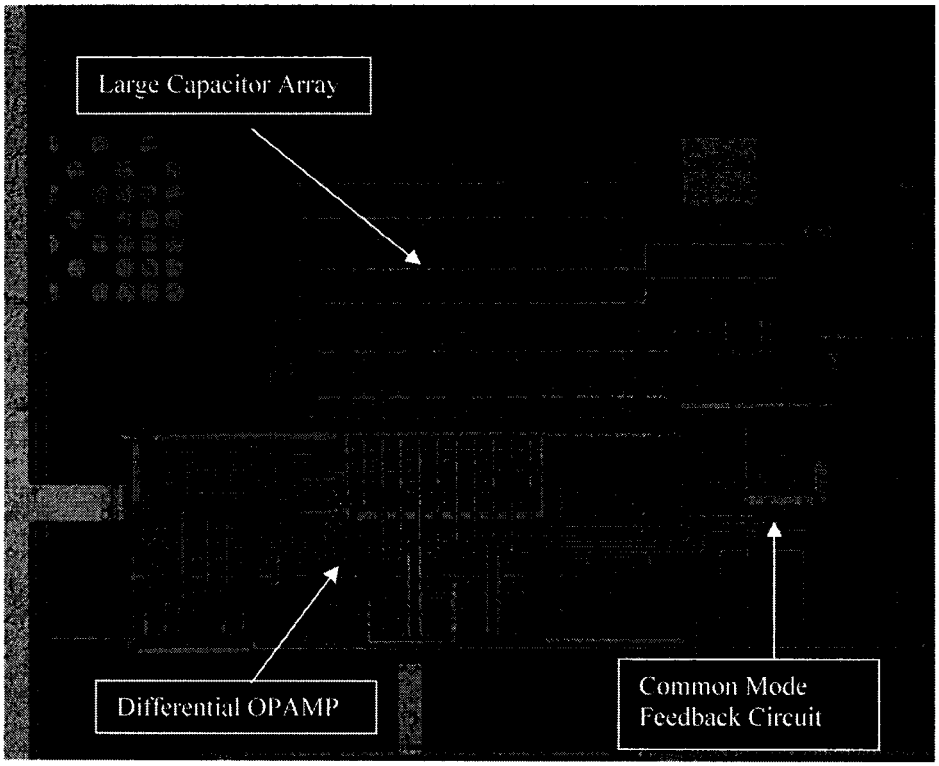

Figure D-10: Microphotograph of the integrator used in the capacitive coupling noise test circuit I (due to the larger coupling noise voltage, the voltage gain of the integrator used in the capacitive coupling noise test circuit I is set smaller, see the larger capacitance array on the top of the microphotograph)

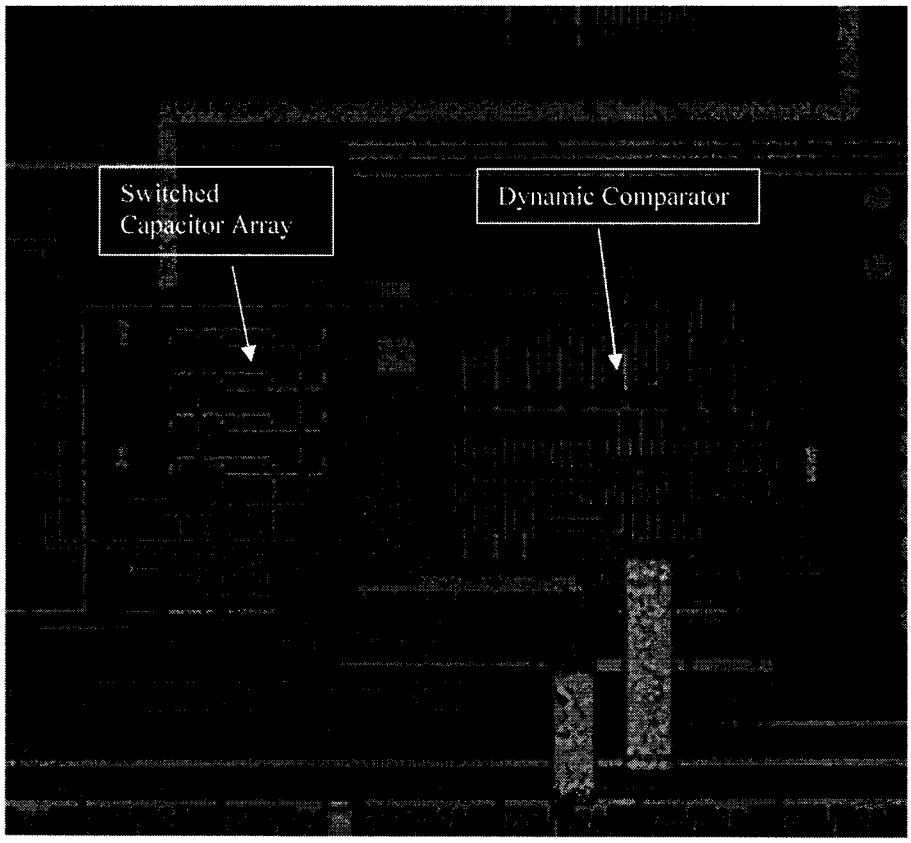

Figure D-11: Microphotograph of the comparator circuit used to compare the integrated coupling noise voltage and the reference voltages.

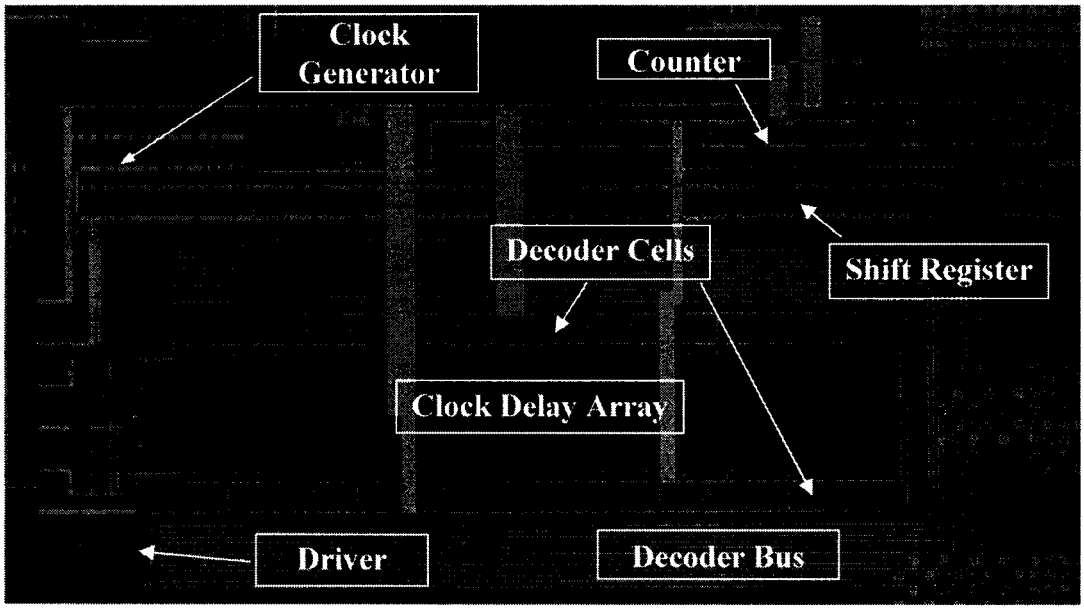

Figure D-12: Microphotograph of the digital section of the substrate coupling noise test circuits

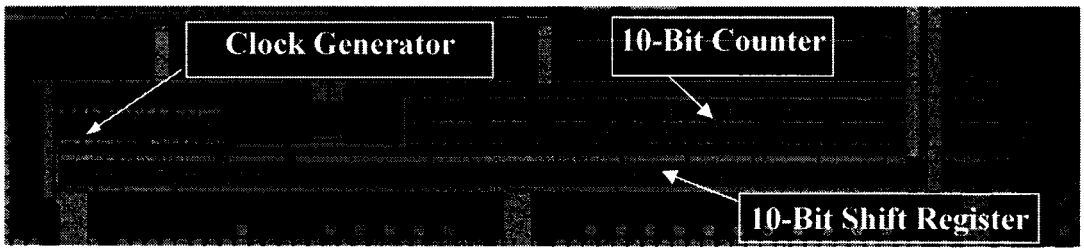

Figure D-13: Microphotograph of the digital section of the line-to-line capacitive coupling noise test circuit I

Appendix E: IC Test Setup

The use of on-chip A/D conversion greatly simplifies the IC test setup. All of the analog circuits operate in the differential mode and are designed with a high power noise rejection ratio. The analog inputs to the test circuit are the power supply voltage, common-mode reference voltage, and the reference voltages. Based on the nature of the circuits, only noise from the reference voltages may affect the test accuracy. The reference voltages are generated on the test board and are designed to match the differential reference voltage pair (V_{REFP} and V_{REFM}.) The remaining inputs and outputs are digital signals. All of the digital input signals are generated on the test board from a master clock which is derived from a stand alone external pulse generator. The select for the noise generator and the delay time is set by the on-board switch arrays.

The two test boards shown in Fig. E.2 are used to measure the noise. Printed circuit board A has two switch arrays for generating the address codes for the noise selecting decode and the delay selecting decode. A zero force insert socket is located at the center of test board A. The common mode voltage and the reference voltages are generated on test board A. The power supply voltage is generated by the "daughter" board B, as shown in Fig. E.2. The test board B is an interface board to connect the test board to the Kodak data processing system (which is not shown

in Fig. E.2). Test board A is plugged onto the pin connectors of test board B during test as shown in Fig. E.1. The equipment used during the noise measurement is listed in Table E.1.

Procedures for the noise measurement are:

1. Insert the test circuit (C) into the on-board socket (S) as shown in Fig. E.1.
2. Connect the power supply (P in Fig. E.1) to the test board. The reference voltages V_{REFP}, V_{REFM}, and the common mode voltage V_{CM} are generated on the test board.
3. Set the switch arrays (A and B) to select the noise generator and the delay time.
4. Connect the pulse generator to the CLK pin of the test board. The system calibration and system rest clocks are generated on the printed circuit board.
5. Connect the ""DONE," "DOUT," and "CALIBRATION" pins to different channels of the digital oscilloscope.
6. Record the digital codes from the digital oscilloscope.

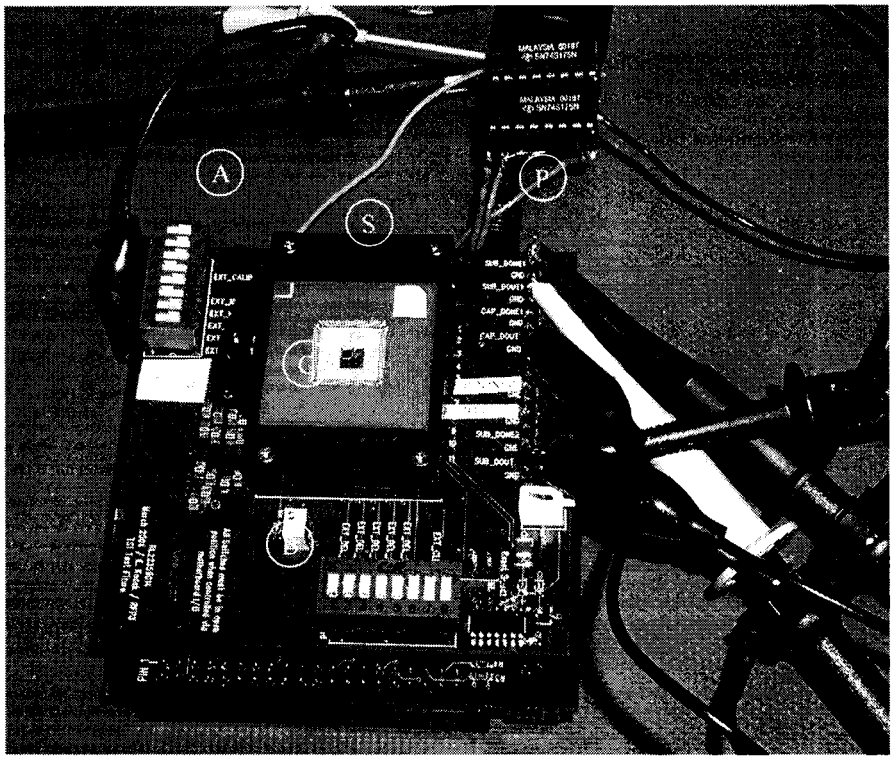

Figure E-1: Photograph of the test board and test setup

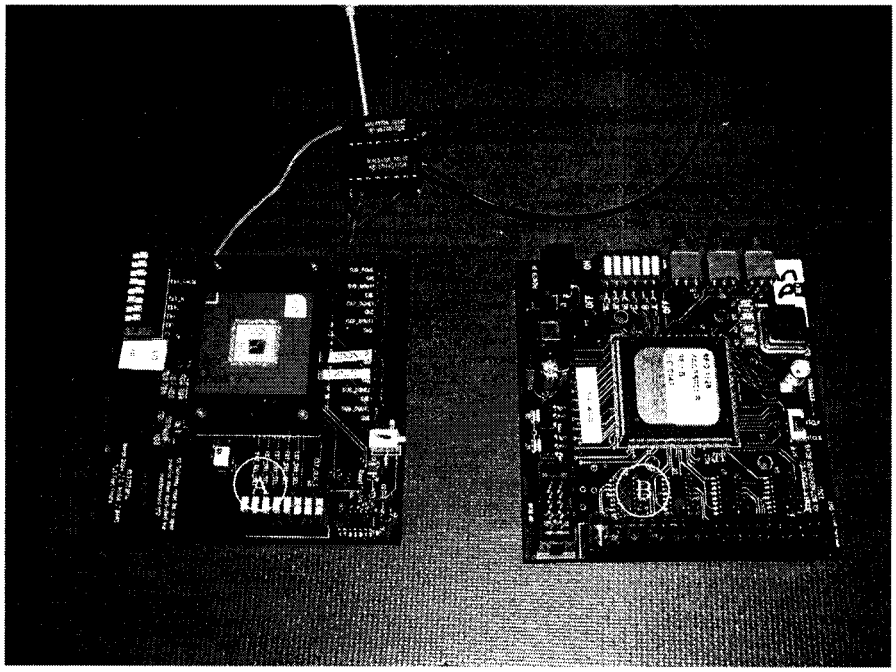

Figure E-2: Photograph of the test board (A) and "daughter" board (B) which acts as the interface board between the test board (A) and the Kodak automatic data acquisition system (not shown)

Table E.1: Equipment use during the IC test process

Name	**Function**	**Comments**
Tektronix PS280	Dual DC Power Supply	
HP 8112A	Pulse Generator	Frequency up to 50 MHz
LeCroy LT344 Waverunner	Digital Oscilloscope	4 channels, 500 MS/s
A 4" X 4" test board	With IC socket and connection pins	

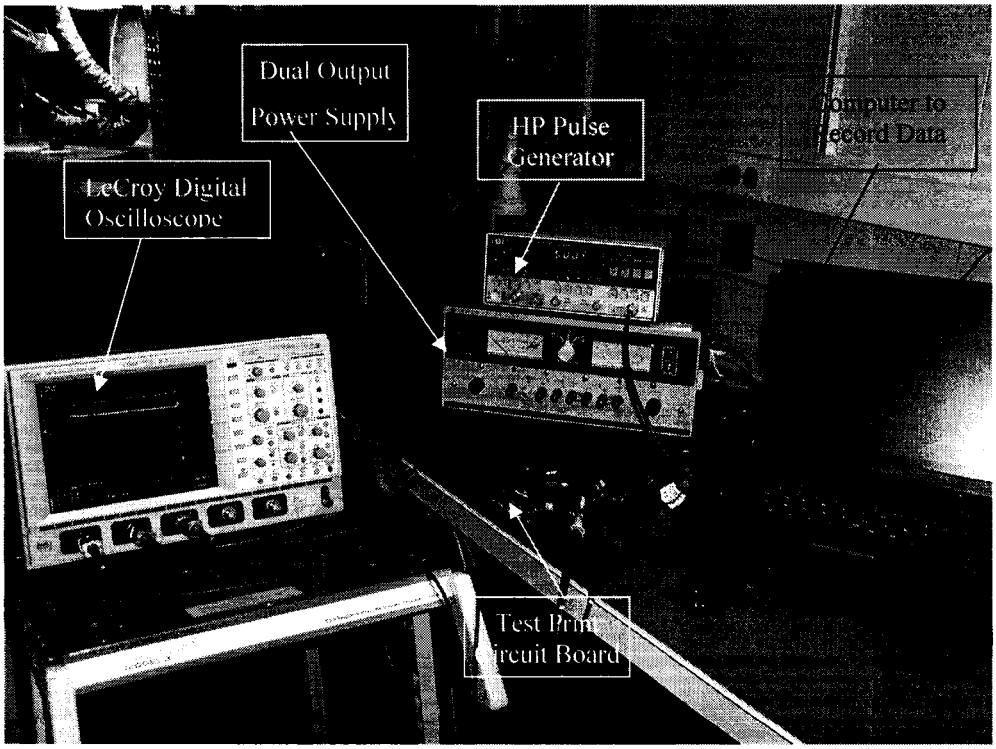

Figure E-3: Photograph of the test setup