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Abstract

In a synchronous digital system, the clock signal is used to define a time reference for the movement of data within that system. Since this function is vital to the operation of a synchronous system, much attention has been given to the characteristics of these clock signals and the networks used in their distribution. Clock signals are often regarded as simple control signals; however, these signals have some very special characteristics and attributes.Clock signals are typically loaded with the greatest fanout, travel over the greatest distances, and operate at the highest speeds of any signal, either control or data, with in the entire synchronous system. Since the data signals are provided with a temporal reference by the clock signals, the clock waveforms must be particularly clean and sharp. Furthermore, these clock signals are

of the primary reasons for the increasing significance of clock distribution on synchronous performance. Finally, the control of any differences and uncertainty in the arrival times of the

synchronous digital systems consist of cascaded banks of sequential registers with combinatorial logic between each set of registers. The functional requirements of the digital system are satisfied by the logic stages. The global performance and local timing requirements are satisfied by the careful insertion of pipeline registers into equally spaced time windows to satisfy critical worst case timing constraints. The proper design of the clock distribution network ensures that these critical timing requirements are satisfied and that no race conditions exist.The delay components that make up a general synchronous system are composed of the following three individual subsystems: the memory storage elements, the logic elements, and the clocking circuitry and distribution network. Interrelationships among these three subsystems of a synchronous digital system are critical to achieving maximum levels of performance and reliability.Novel structures are currently under development to ameliorate these issues and provide effective solutions. Important area of research include resonant clocking techniques, on-chip optical interconnect, and local synchronization methodologies.The literature in this field exists in a variety of journals and conference proceedings. Examples include the IEEE Transactions of Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, the IEEE/ACM Design Automation Conference, and a host of related computer, circuits, and CAD conferences. Survey and review articles exist that summarize many of the primary results while providing background and perspective.

References

1. E. G. Friedman (Ed.), Clock Distribution Networks in VLSI Circuits and Systems, IEEE Press. 1995.

2. E. G. Friedman, "Clock Distribution Networks in Synchronous Digital Integrated Circuits," Proceedings of the IEEE, Vol. 89, No. 5, pp. 665-692, May 2001.

Index Terms

What are clock distribution networks?

Hardware

Integrated circuits

Robustness

Digital switches

Logic families

Logic circuits

Comments