

# Receiver Power Issues Related to Matched Filter Implementation for Portable Wireless Communication Terminals<sup>†</sup>

Mark D. Hahm, Eby G. Friedman, and Edward L. Titlebaum  
Department of Electrical Engineering  
University of Rochester  
Rochester, New York 14627

hahm@ee.rochester.edu, friedman@ee.rochester.edu, tbaum@ee.rochester.edu

**Abstract** — A number of recently proposed personal communication systems (PCS) call for the use of spread-spectrum techniques for transmitting digital data through multiple-access channels. In these systems, a correlator or matched filter is used within the receiver to despread the encoded waveform before the underlying digital data is recovered. The receiver matched filter block lies between the analog front-end electronics and the digital data-decoding electronics. As such, the matched filter may be implemented either before or after the received waveform has undergone analog-to-digital conversion. Since power consumption is a principal concern for portable PCS terminals, it is proper to consider which matched filter implementation— analog or digital— leads to a more power efficient spread-spectrum receiver.

In this paper, these two different implementations are examined, and a methodology is provided for choosing the appropriate circuit-implementing technology using power consumption—as a function of data precision, filter length, operating frequency, technology scaling, and the maturity of the fabrication process—as the primary metric of comparison. It is shown that neither the analog nor the digital matched filter implementation is universally appropriate. Rather, a surface is mapped out in the multi-dimensional design space where, on one side of this surface, a digital solution is preferable, while on the other side of the surface, an analog circuit is appropriate. Equations are given which delineate the position of this transitional surface in terms of the design space parameters, and example calculations and plots depicting the regions of dominance for the digital and analog matched filters for specific process and system parameters are provided.

## I. INTRODUCTION

In the past, most of the interest in spread-spectrum systems has been confined to military applications and satellite communications. Within the past several years, however, commercial systems have been proposed and implemented which exploit desirable spread-spectrum characteristics such as immunity to the fading effects of multipath, ease of multiple-access overlay, and the ability to transmit at lower radiated power levels [1-5]. A birth of interest in spread-spectrum communication systems targeted to commercial applications

has occurred and is due in part to the steady advances in high density semiconductor fabrication technologies, which allow the complex modulate and demodulate functions of the spread-spectrum transceivers to be realized while still meeting the size, cost, and power budgets imposed by the consumer marketplace.

A matched filter [6,7] is an integral part of an asynchronous spread-spectrum communication receiver or range-finding device and may be used to shorten search and synchronization times within receivers of *long code* systems [5,8,9], such as the CDMA cellular proposal, IS-95 [10]. Many of the new areas of commercial utility employ portable communication terminals with limited power sources. Thus, low-power transmitters and receivers are needed if spread-spectrum is to become commercially viable. Though the generation and transmission of spread-spectrum signals is well understood and can be realized by technologies which consume relatively small amounts of power [11,12], the receivers for these systems—including the matched filter block—are considerably more complex [4,5,13], and work is ongoing to develop practical lower-power devices.

The matched filter block (shown in Figure 1a) of a radio occupies a place between the RF input circuitry and the digital data-processing circuitry. As such, the conversion from analog to digital can take place either just before the matched filter input or just after its output. This leaves the designer with the freedom to use the most suitable matched filter, analog or digital.

In the discussion that follows, two different CMOS realizations of a programmable parallel matched filter—one digital and one analog—are studied and compared in order to determine the most appropriate circuit-implementing technology for use in commercial spread-spectrum communication systems. Throughout this paper, power consumption—as a function of data precision, filter length, operating frequency, technology scaling, and the maturity of the fabrication process—is used as the primary metric of comparison.

## II. DIGITAL IMPLEMENTATION

The digital programmable parallel matched filter structure that is used in this analysis is pictured in block diagram form in Figure 1b. The operation of the filter is such that each new input data sample appears simultaneously at the input of each multiplier block. After multiplication with the  $N$  stored reference coefficients, the partial sums of products are shifted one cell to the right during each clock cycle, with the final sum at the bottom right being the desired matched filter output. This structure is commonly used in FIR filters (e.g., [14]) and has several advantages over a direct implementation

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of Figure 1a, such as ease of layout and no need for a single large adder to generate the output result.

The power consumption of the digital matched filter can be estimated by summing the contribution of the major logic blocks: the registers, adders, and multipliers. In the following analysis, it is assumed that the dynamic charging and discharging of the inherent circuit capacitances is the primary contributor to the total circuit power consumption. The total circuit power may therefore be estimated by computing or measuring the effective switched capacitance of each of the major logic blocks and calculating the familiar  $CV^2f$  dynamic power dissipation. However, in the spirit of [15], supply voltage can vary as a function of operating frequency and quantization level. A single supply voltage is assumed for the entire matched filter, with the value for  $V_{DD}$  being determined by the speed requirements of the most

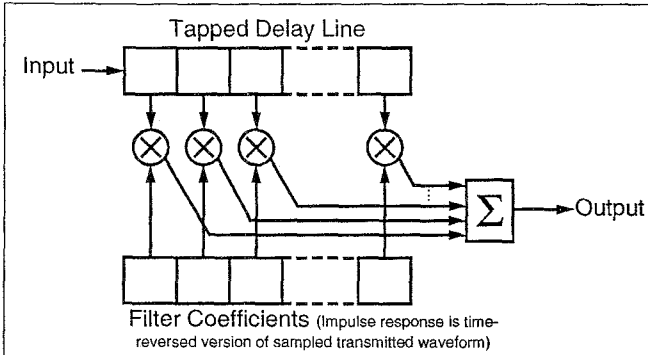


Figure 1a. Parallel matched filter structure.

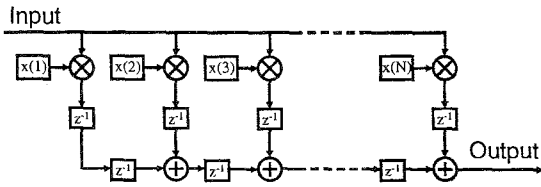


Figure 1b. Digital matched filter architecture.

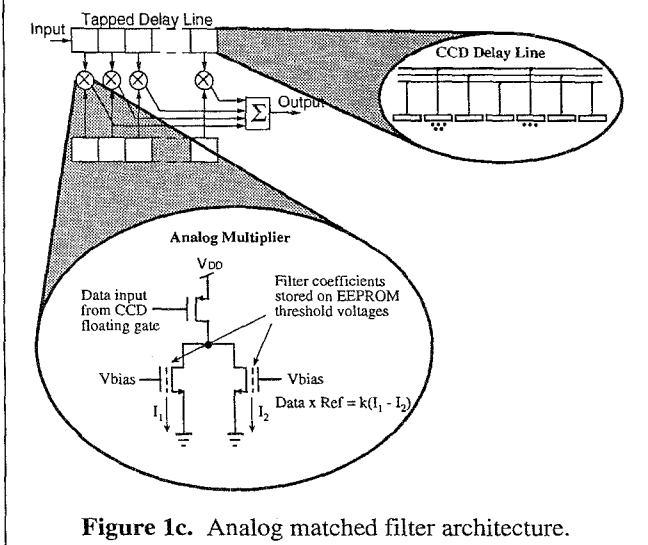


Figure 1c. Analog matched filter architecture.

performance limiting circuit elements: the multipliers.

From [15], an estimate of gate propagation delay  $T_d$  is given as a function of supply voltage  $V_{DD}$ , threshold voltage  $V_T$ , load capacitance  $C_L$ , oxide capacitance per unit area  $C_{ox}$ , electron mobility  $\mu$ , and the CMOS gate width-to-length ratio  $W/L$ :

$$T_d \cong \frac{C_L}{\mu C_{ox} W/L} \cdot \frac{V_{DD}}{(V_{DD} - V_T)^2} \quad (1)$$

Also, for a given technology, the time required to complete a  $Q_d$  bit  $\times$   $Q_r$  bit multiplication can be approximated as [16,17]

$$T_{multiply} \cong M(Q_d + Q_r - 1), \quad (2)$$

where  $M$  is the delay of a one-bit adder in units of seconds/bit, and  $Q_d$  and  $Q_r$  are the level of data and reference quantization, respectively.

Combining (1) and (2) gives

$$T_{multiply} \cong K_d(Q_d + Q_r - 1) \cdot \frac{V_{DD}}{(V_{DD} - V_T)^2}, \quad (3)$$

where  $\frac{C_L}{\mu C_{ox} W/L}$  and  $M$  have been merged to form  $K_d$ , a technology dependent constant with units of volt  $\cdot$  seconds / bit.

From (3),  $V_{DD}$  can be solved, which, in turn, can be used to estimate the power consumption of a digital multiplier,

$$P_{multiply} \cong \frac{K_p Q_d (Q_r - 1)}{T_{multiply}} \left[ \frac{1}{2} \left( \beta + \sqrt{\beta^2 - 4V_T^2} \right) \right]^2, \quad (4)$$

$$\text{where } \beta = 2V_T + \frac{K_d(Q_d + Q_r - 1)}{T_{multiply}},$$

and  $K_p$  is a technology dependent constant with units of farads / bit<sup>2</sup>.

The total power consumption of the digital matched filter  $P_{DMF}$  is

$$P_{DMF} \cong NP_{multiply} + AC_{ADDER}V_{DD}^2f_{clk} + RC_{REGISTER}V_{DD}^2f_{clk}, \quad (5)$$

where  $N = 2^K$  is the number of filter taps,  $f_{clk}$  is the operating frequency of the matched filter,  $C_{ADDER}$  and  $C_{REGISTER}$  are the effective switched capacitance of the full adders and one-bit registers, respectively, and  $A$  and  $R$  are the number of full adders and one-bit registers in the digital matched filter, as given by

$$A = (2^K - 1)(Q_d + Q_r) - K + \sum_{m=1}^{K-1} (m2^m),$$

and

$$R = 2^{K+1}(Q_d + Q_r) - (2^K + 1) + \sum_{m=1}^{K-1} (m2^m).$$

In the plots that follow, the values below are assumed for a 2.0  $\mu\text{m}$  CMOS process:

$$V_T = 1.0 \text{ volt},$$

$$C_{\text{REGISTER}} = 250 \text{ fF},$$

$$C_{\text{ADDER}} = 600 \text{ fF},$$

$$K_p = 1.5 \text{ pF / bit}^2, \text{ and}$$

$$K_d = 10^{-8} \text{ volt} \cdot \text{seconds / bit}.$$

The choice of implementing technology has an enormous effect on the power consumption of the digital matched filter. Assuming the operating frequency requirements of the matched filter can be satisfied by a particular technology, the supply voltage in the scaled technology can be decreased to realize additional power savings [15] beyond those achievable by a direct application of classical scaling rules [18,19]. The reduction in power dissipation depends upon the degree of technology scaling (represented by the scaling constant  $\kappa$  [18]) and the ratio of the threshold voltage to the supply voltage in the unscaled technology,

$$\rho = \frac{V_{T_{\text{unscaled}}}}{V_{DD_{\text{unscaled}}}}. \quad (6)$$

The power scaling constant, which is defined in this paper as  $S_C$ , is

$$S_{C_{CE}} = \frac{1}{\kappa^3} \left( \rho + \frac{(1-\rho)^2}{2\kappa} + \frac{(1-\rho)}{2} \sqrt{\frac{4\rho}{\kappa} + \left(\frac{1-\rho}{\kappa}\right)^2} \right)^2, \quad (7)$$

or

$$S_{C_{CVT}} = \frac{1}{\kappa} \left( \rho + \frac{(1-\rho)^2}{2\kappa^2} + \frac{(1-\rho)}{2\kappa} \sqrt{4 - \left(\frac{1-\rho}{\kappa}\right)^2} \right)^2. \quad (8)$$

$S_{C_{CE}}$  is applicable assuming ideal constant electric-field scaling [18].  $S_{C_{CVT}}$  is applicable assuming the threshold voltage does not scale with the other device parameters. The current industry trend lies somewhere between these two schemes, as shown in Figure 2.

The estimate of the power consumption of the digital matched filter is a function of operating frequency, quantization level, filter length (number of taps), and technology scaling:

$$P_{DMF_{CE}} \equiv S_{C_{CE}} P_{DMF}, \quad (9a)$$

or

$$P_{DMF_{CVT}} \equiv S_{C_{CVT}} P_{DMF}, \quad (9b)$$

depending on which scaling procedure is used to shrink the device dimensions and operating voltages.

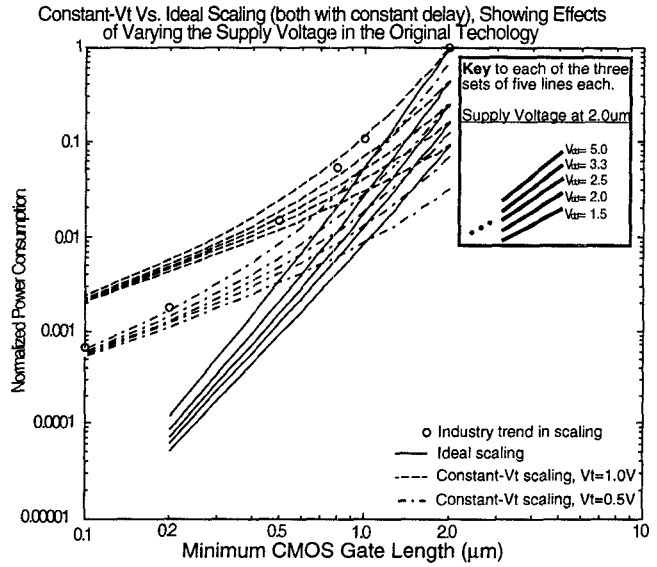


Figure 2. Effects of technology scaling on digital circuit power consumption.

### III. ANALOG IMPLEMENTATION

The analog matched filter structure shown in Figure 1c is used to compare the analog and digital circuit-implementing technologies. The tapped delay line function is realized by a surface channel charge-coupled-device (CCD) analog shift register, which may be simply understood as a bank of sequentially switched MOS capacitors. The signal is in the form of electrically injected minority carriers present under the appropriately clocked CCD gates. A surface channel device is used rather than a buried channel device because the surface channel device is inherently more linear and, due to electrical injection of the signal charge, the surface channel device is capable of higher signal integrity [20].

In the configuration shown in Figure 1c, a floating-gate tap [22] is attached to every third CCD gate and is used to non-destructively sense the signal charge packets which pass under these gates. The multiply function and reference coefficient storage are achieved by the two-transistor EEPROM structure shown in Figure 1c. The reference coefficient voltage  $V_{REF}$  is stored by altering the threshold voltages of the two EEPROMs in a cell via control circuitry (not shown in Figure 1c). The resulting thresholds are:

$$V_{T_1} = V_T - \delta V_{REF},$$

and

$$V_{T_2} = V_T + \delta V_{REF}.$$

The sources of the two EEPROMs are connected to separate current-summing busses, both of which are held at virtual ground. When operating in the triode (or linear) region, the difference between the drain currents through the two EEPROMs is proportional to a multiplication of the drain voltage and the stored reference voltages.

The structure and circuit elements pictured in Figure 1c have appeared in the literature in various forms for over two decades [21-24]. The structure is used here because, as far as the authors are aware, it is the most power-efficient means to

implement an analog parallel programmable matched filter in readily available silicon technology. As such, the structure is suitable for comparison with its digital counterpart.

The power consumption of the analog matched filter is a function of the signal-to-noise ratio (SNR). This relationship is completely analogous to considering the power consumption of the digital matched filter as a function of quantization level. The analog SNR and the digital quantization level are related via

$$SNR = \sqrt{3}(2^{Q_d} - 1), \quad (10)$$

where  $Q_d$  is the data quantization level used in (2).

The static current of the multiplier/tap structures and the dynamic switching of the CCD gates are the dominant sources of power dissipation within the analog matched filter. The dominant noise sources are the thermal noise of the tap and multiplier FETs and interface trapping effects under the CCD gates [20,25,26]. The problem of flicker noise is assumed to be alleviated by a correlated-double-sampling amplifier [29] on the matched filter output. With these assumptions, and with the aid of the CCD signal capacity and signal quality equations given in [20,26] and the CMOS amplifier noise equations given in [25], an estimate of the power dissipation within the entire analog matched filter is

$$P_{AMF} \cong 8 \cdot SNR^2 \cdot f_{clk} \cdot kT \cdot N \left( \frac{a(a-b)}{a-\sqrt{ab}} + \frac{b(b-a)}{b-\sqrt{ab}} \right), \quad (11)$$

$$\text{where } a = \ln(2) \cdot N \cdot N_{ss} \cdot \frac{q}{C_{ox}} \cdot \frac{V_{DD}}{V_{DD} - \phi_s},$$

$$b = \frac{\sqrt{2} \cdot V_{DD}}{3(V_{DD} - 3V_T)} + \frac{V_{DD}(V_{DD} - 2V_T)}{(V_{DD} - 5V_T/2)V_T}.$$

The thermal energy  $kT$  is in units of joules,  $N$  is the number of filter taps,  $f_{clk}$  is the operating frequency,  $N_{ss}$  is the surface state density,  $V_T$  is the threshold voltage of the EEPROM and PFETs (assumed to be equal in magnitude),  $q$  is the charge of an electron,  $C_{ox}$  is the oxide capacitance per unit area, and  $\phi_s$  is the minimum surface potential under the CCD gates. Note also that the  $a$  term in (11) is dependent upon the physical parameters of the CCD fabrication process, while the  $b$  term is dependent upon the bias conditions of the multiplier/tap FETs.

As noted above, by scaling the device dimensions and power supply voltage, an enormous power savings in the digital circuitry is possible. These significant savings are not as likely with the analog matched filter implementation of Figure 1c. The decrease in anneal time for thinner gate oxides leads to an increase in surface state density [27]. Thus, even though the switched capacitance of a scaled analog matched filter may be smaller than the unscaled filter, the supply voltage may need to be raised to offset the negative effects of the increased surface state density within the scaled device. Thus the effect of scaling on the power consumption of the analog matched filter is process dependent. Similar, more general conclusions pertaining to analog circuits and scaling issues are drawn in [28].

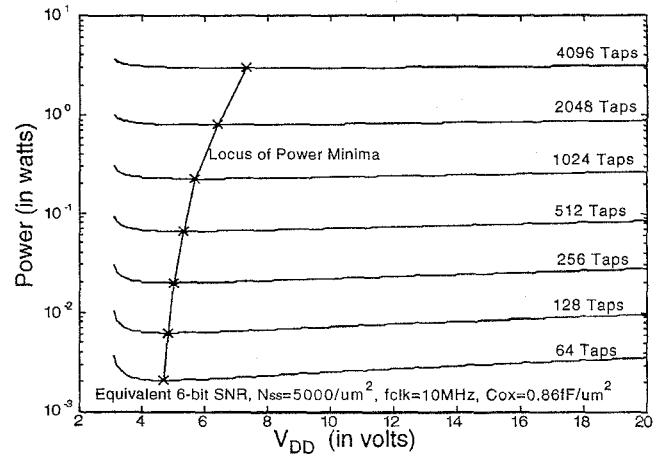


Figure 3. Analog matched filter power as a function of supply voltage and filter length.

The choice of supply voltage is more flexible in the analog filter than in the digital filter. This flexibility exists because a matched filter of equivalent performance can be made from a circuit with a higher supply voltage if the CCD gate areas are decreased. For example, in Figure 3 it is shown that only a small change in the power dissipation of the analog matched filter occurs for wide changes in the supply voltage.

#### IV. COMPARISON AND CONCLUSIONS

Both of the circuit implementations under consideration perform the same operation and use the same physical device—the MOS capacitor—as the primary circuit element. The digital implementation, in treating the MOS capacitor-based devices as binary switches, sacrifices power efficiency for the ability to regenerate weak or degraded signals within the circuit.

The analog implementation uses the fundamental device I-V transistor relationships to efficiently achieve the sum and multiplication functions. However, the analog circuit is unable to regenerate weak or degraded internal signals. Thus, at the cost of additional power consumption, the analog circuit must inject added signal quality (surplus SNR) at the input of the shift register structure, such that the design specifications are satisfied by the degraded signal at the end of the shift register. This difference is depicted in the power consumption equations, which quantify how the power consumption as a function of filter length increases at a quadratic rate for the analog circuit, while at a less harsh linear-plus-logarithmic rate for the digital circuit.

The digital implementation is more sensitive to changes in circuit speed. This sensitivity is due to the ability of the digital circuit to exploit a decrease in operating frequency by supporting a corresponding decrease in the supply voltage.

The digital circuit is also more sensitive to changes in technology. By decreasing the minimum gate length of the CMOS technology, significant power savings may be realized. This behavior is not necessarily true for the analog circuit, since device physics limit the analog circuit more severely than the digital circuit.

Since changes in filter size, technology scaling, and operating frequency have different effects on the power consumption of the analog and digital circuits, it follows that

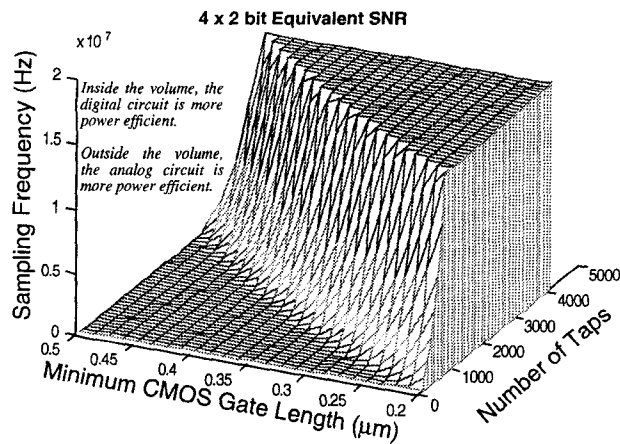


Figure 4. Surface of equal power dissipation for the analog and digital matched filter implementations as a function of filter length, sampling frequency, and technology.

there may be points in the design space where the digital circuit is more power efficient than the analog circuit, and still other points in the design space where the opposite may be true. As shown in Figure 4, for a given effective quantization level (4 x 2 bit in this example), a surface in the multi-dimensional design space exists that defines the boundary between the regions of superior power efficiency of the analog and digital circuits. Inside the volume in the figure, the digital implementation is more power efficient. Outside the volume, the analog circuit is more power efficient. Specific power estimates of the digital and analog circuit implementations may be obtained with (9) and (11), respectively.

In conclusion, note that the analog circuit implementation discussed in this paper is more power efficient for shorter, faster matched filters, and, conversely, the digital circuit is more power efficient where the filters are longer and slower. These generalizations, when coupled with the specific information that is contained in the digital and analog power equations, (9) and (11), indicate which circuit-implementing technology is most power efficient for a given set of system and process parameters.

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## BIOGRAPHIES



Mark D. Hahm (S'93) was born in Rochester, NY in 1971. He received the B.S. (highest distinction) and M.S. degrees in electrical engineering from the University of Rochester in 1993.

Currently, he is an AT&T Ph.D. Fellow working towards the Ph.D. degree in electrical engineering at the University of Rochester. His research interests include the communications theory and hardware implementation issues associated with wireless and fiber optic spread-spectrum receivers. While pursuing these degrees, he worked summers in the Test Equipment Design group of Eastman Kodak Company and, more recently, as a summer intern at AT&T Bell Laboratories in the Wireless Multi-Media Technology group, where he designed, implemented, and tested a prototype forward link transmitter for an enhanced IS-95-compatible wireless data network.



**Eby G. Friedman** was born in Jersey City, NJ in 1957. He received the B.S. degree from Lafayette College, Easton, PA in 1979, and the M.S. and Ph.D. degrees from the University of California, Irvine, in 1981 and 1989, respectively, all in electrical engineering.

He was with Philips Gloeilampen Fabrieken, Eindhoven, The Netherlands, in 1978 where he worked on the design of bipolar differential amplifiers. From 1979 to 1991, he was with Hughes Aircraft Company, rising to the position of manager of the Signal Processing Design and Test Department, responsible for the design and test of high performance VLSI/VHSIC CMOS and BIMOS digital and analog IC's, the development of supporting design and test methodologies and CAD tools, and the development of high performance and high resolution DSP and oversampled systems. He has been in the Department of Electrical Engineering at the University of Rochester, Rochester, NY, since 1991, where he is an Associate Professor and Director of the High Performance VLSI/IC Design and Analysis Laboratory. His current research and teaching interest are in the areas of high performance VLSI/IC design and analysis and related system applications.

He has published in the fields of high speed and low power CMOS design techniques, pipelining and retiming, and the theory and application of synchronous clock distribution networks, and has edited one book, *Clock Distribution Networks in VLSI Circuits and Systems* (IEEE Press, 1995). Dr. Friedman is a Senior Member of the IEEE, a Member of the editorial boards of the *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* and *Analog Integrated Circuits and Signal Processing*, Chair of the VLSI Systems and Applications CAS Technical Committee, a Member of the technical program committee of several conferences, and Chair of the Electron Devices Chapter of the IEEE Rochester Section.



**Edward L. Titlebaum** was born in Boston, MA in 1937 and was educated in the public schools of Boston. He received a B.S.E.E. degree in 1959 from Northeastern University, Boston, MA, and the M.S. and a Ph.D. degrees in 1962 and 1964, respectively, both in electrical engineering from Cornell University, Ithica, New York.

He has been in the Department of Electrical Engineering at the University of Rochester from 1964 to the present, currently holding the position of Professor of Electrical Engineering. His research interests lie in the general areas of radar, sonar, and communications signal design and natural echolocation systems, including those used by bats and whales. Currently he is studying frequency hop codes based upon congruential coding methods for use in multiple access spread-spectrum communications and multiuser radar and sonar systems. He is investigating the role of these signals in CDMA spread-spectrum communications systems, computer networks, and line alarm systems for power companies.