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Delay and noise estimation of CMOS logic gates driving coupled resistive–capacitive interconnections

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Abstract

The effect of interconnect coupling capacitance on the transient characteristics of a CMOS logic gate strongly depends upon the signal activity. A transient analysis of CMOS logic gates driving two and three coupled resistive–capacitive interconnect lines is presented in this paper for different signal combinations. Analytical expressions characterizing the output voltage and the propagation delay of a CMOS logic gate are presented for a variety of signal activity conditions. The uncertainty of the effective load capacitance on the propagation delay due to the signal activity is also addressed. It is demonstrated that the effective load capacitance of a CMOS logic gate depends upon the intrinsic load capacitance, the coupling capacitance, the signal activity, and the size of the CMOS logic gates within a capacitively coupled system. Some design strategies are also suggested to reduce the peak noise voltage and the propagation delay caused by the interconnect coupling capacitance.

Keywords: Coupling noise; Signal activity; Delay uncertainty; Deep submicrometer; CMOS integrated circuits; Interconnect; VLSI

1. Introduction

On-chip coupling noise in CMOS integrated circuits (ICs), until recently considered a second-order effect [1,2], has become an important issue in deep submicrometer (DSM) CMOS integrated circuits [3–5]. With decreasing feature size and increasing average length of on-chip interconnections, the interconnect capacitance has become comparable to or larger than the gate capacitance [6–8].

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Nomenclature

For a three-line coupled system:

B_{n}	transconductance of an NMOS transistor
$B_{\mathrm{n}1}$	transconductance of the NMOS transistor in Inv_1
$B_{\mathrm{n}2}$	transconductance of the NMOS transistor in Inv_2
$B_{\mathrm{n}3}$	transconductance of the NMOS transistor in Inv_3
B_{p}	transconductance of a PMOS transistor
$B_{\mathrm{p}1}$	transconductance of the PMOS transistor in Inv_1
$B_{\mathrm{p}2}$	transconductance of the PMOS transistor in Inv_2
$B_{\mathrm{p}3}$	transconductance of the PMOS transistor in Inv_3
C_1	intrinsic load capacitance of Inv_1 including the interconnect capacitance of line 1 and the gate capacitance of the following stage
C_2	intrinsic load capacitance of Inv_2 including the interconnect capacitance of line 2 and the gate capacitance of the following stage
C_3	intrinsic load capacitance of Inv_3 including the interconnect capacitance of line 3 and the gate capacitance of the following stage
C_{12}	coupling capacitance between lines 1 and 2
C_{23}	coupling capacitance between lines 2 and 3
$C_{1_{\mathrm{eff}}}$	effective load capacitance of Inv_1
$C_{2_{\mathrm{eff}}}$	effective load capacitance of Inv_2
$C_{3_{\mathrm{eff}}}$	effective load capacitance of Inv_3
γ	effective output conductance of an MOS transistor in the linear region
n_{n}	parameter characterizing a short-channel NMOS transistor
n_{p}	parameter characterizing a short-channel PMOS transistor
R_1	interconnect resistance of line 1
R_2	interconnect resistance of line 2
R_3	interconnect resistance of line 3
$t_{0.5}$	time for the output voltage reaching $0.5V_{\mathrm{dd}}$
$t_{\mathrm{P_{HL}}}$	high-to-low propagation delay
$t_{\mathrm{P_{LH}}}$	low-to-high propagation delay
τ_{n}	turn-on time of an NMOS transistor
τ_{p}	turn-on time of a PMOS transistor
τ_{r}	transition time of an input signal
τ_{sat}	duration time when an MOS transistor operates in the saturation region
τ_{nsat}	duration time when an NMOS transistor operates in the saturation region
τ_{psat}	duration time when a PMOS transistor operates in the saturation region
$\tau_{\mathrm{sat}}^{\mathrm{min}}$	time when one active transistor operating in the linear region in a coupled system
$\tau_{\mathrm{sat}}^{\mathrm{max}}$	time when all active transistors operating in the linear region in a coupled system
V_1	output voltage of Inv_1
V_2	output voltage of Inv_2
V_3	output voltage of Inv_3
V_{dd}	supply voltage

V_{in}	input voltage
V_{nsat}	saturation voltage of an NMOS transistor
V_{psat}	saturation voltage of a PMOS transistor
V_{TN}	threshold voltage of an NMOS transistor
V_{TP}	threshold voltage of a PMOS transistor
For a two-line coupled system:	
C_c	coupling capacitance between lines 1 and 2

Interconnections in a CMOS integrated circuit are conductors deposited on dielectric insulation layers [9,10]. The mutual electric field flux between neighboring interconnect lines results in a coupling (or fringing) capacitance [11–16]. The coupling capacitance increases as the spacing between adjacent interconnect lines is reduced and/or the aspect ratio of the interconnect thickness-to-width is increased [7,8]. The coupling capacitance may become comparable to the line-to-ground interconnect capacitance [14,16,17]. Therefore, capacitive coupling has emerged as one of the primary issues in evaluating the signal integrity of CMOS integrated circuits [18–22].

The importance of interconnect coupling capacitances depends upon the signal behavior of a CMOS logic gate [23]. If a CMOS logic gate driving a coupled interconnection is in transition, the coupling capacitance can affect the propagation delay and the waveform shape of the output voltage signal [24]. For a capacitively coupled system, if one of these CMOS logic gates is quiet and the other logic gates are in transition, the coupling capacitance can not only change the propagation delay of the active logic gates, but can also induce a voltage change at the output of the quiet logic gate [25,26]. If the voltage change is greater than the threshold voltage of the following logic gates, circuit malfunctions and unexpected power dissipation in the fanout stages may occur [3]. Furthermore, a change in voltage may cause overshoots (the signal rises above the voltage supply) or undershoots (the signal falls below ground) [27,28].

In most current IC design processes, coupling effects cannot be accurately estimated until the physical layout of a CMOS integrated circuit is determined. Therefore, several design iterations may be required to minimize the effects of interconnect coupling capacitance to satisfy a target performance requirement [21,22]. In order to reduce both the design cost and time, coupling effects should also be estimated at the system level [29]. The coupling noise voltage on a quiet interconnect line has been analyzed by Shoji in Ref. [3] using a simple linear *RC* circuit. Delay uncertainty and noise expressions of coupled resistive interconnect have been presented by Kahng using π and L lumped-circuit models in Refs. [30,31]. The effects of the coupling capacitance have also been addressed by Sakurai in Ref. [32] based on a coupled *RC* transmission line model. Estimates of the peak coupling noise voltage based on a coupled *RLC* transmission line model have been presented by the authors in Ref. [33]. A two-line coupled system is presented in the literature [3,23,30,32,33] to analyze this coupling effect. A three-line coupled system is presented in Ref. [34] using an *RC* transmission line model. The CMOS logic gates are approximated by the effective output resistance; the nonlinear behavior of the MOS transistors is therefore neglected in these analyses [3,30,32–34]. Similar interconnect structures (or line impedances) are also assumed in Refs. [32–34] where the impedance differences among the on-chip interconnections are neglected.

The maximum effective load capacitance, i.e., the intrinsic load capacitance plus two times the coupling capacitance ($C + 2C_c$), is typically used to estimate the worst case propagation delay of an active CMOS logic gate [3,32,34].

In this paper, a transient analysis of a CMOS logic gate driving a coupled resistive–capacitive interconnect based on the signal activity is presented. The interconnect-to-ground capacitance (or the self-capacitance) and the gate capacitance of the following logic stage are included in the intrinsic load capacitance (C_1, C_2, or C_3 for a three-line coupled structure). An analysis of an in-phase transition in which two (or three) coupled logic gates transition in the same direction demonstrates that the effective load capacitance of a CMOS logic gate depends upon the intrinsic load capacitance, the coupling capacitance, the signal activity, and the transistor size of the CMOS logic gates within the coupled system. Therefore, the effective load capacitances may deviate from the intrinsic load capacitances if the CMOS logic gates and intrinsic load capacitances are different within a coupled system. The same conclusion can also be observed for an out-of-phase transition, where the transition changes in the opposite direction for a two-line coupled system, making the effective load capacitances deviate from $C_1 + 2C_c$ and $C_2 + 2C_c$, which are typically assumed in a system level analysis [3,32,34].

For two adjacent interconnect lines driven by CMOS logic gates, if one logic gate is active and the other is quiet, the coupling capacitance may cause the effective load capacitance of the active logic gate to be less than $C_1 + C_c$ or $C_2 + C_c$ when the active logic gate transitions from high-to-low and the quiet state is at a logic low (ground). However, if the quiet state is at a logic high (V_{dd}), the effective load capacitance of the active logic gate exceeds $C_1 + C_c$ or $C_2 + C_c$. If the active logic gate transitions from high-to-low and the quiet state is at a logic low, the coupling noise voltage causes the quiet state to drop below ground (undershoots). Overshoots occur when the inverter transitions from low-to-high and the quiet state is at a logic high (V_{dd}). Overshoots or undershoots may cause current to flow through the substrate, possibly corrupting data in dynamic logic circuits [27,28]. This issue is also of significant concern in the logic elements within a bistable latch structure [35].

Analytical expressions characterizing the output voltages for each CMOS logic gate are presented for both a two-line and a three-line coupled system. Delay estimates based on the analytical expressions are within 10% as compared to SPICE [36], while the error of the estimates neglecting the nonlinear behavior of a CMOS logic gate for an in-phase, an out-of-phase, and one active/one quiet transition can reach 50%, 18%, and 16% of SPICE, respectively, for a two-line coupled system. The peak noise voltage based on the analytical prediction is within 7% and 13% of SPICE for a two-line and a three-line coupled system, respectively.

The dependence of the interconnect coupling capacitance on the signal activity is discussed for both a two-line and a three-line coupled system in Section 2. Analytical expressions characterizing the effective load capacitance, the output voltage, and the propagation delay during an in-phase and an out-of-phase transition are addressed in Sections 3 and 4, respectively, for a two-line and a three-line coupled system. In Section 5, an analytical expression characterizing the coupling noise voltage at the output of a quiet logic gate is presented for a two-line coupled system. This analytical model is also applied to a three-line coupled system to predict the peak coupling noise voltage. Strategies to manage the effects of interconnect coupling capacitance are discussed in Section 6, followed by some concluding remarks in Section 7.

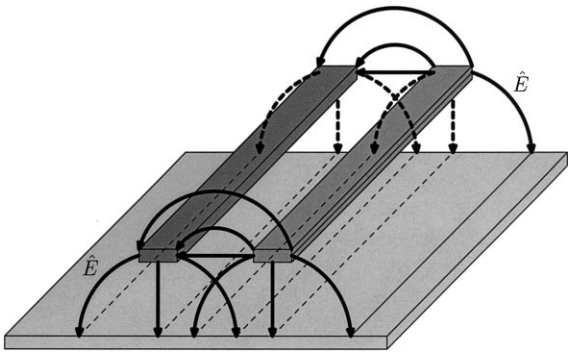

Fig. 1. Physical structure of two capacitively coupled interconnect lines.

2. Signal activity of coupled interconnect

A physical structure of two coplanar interconnect lines is shown in Fig. 1. A self-interconnect capacitance includes a parallel plate capacitance and a sidewall-to-ground capacitance [6,13,17]. The sidewall-to-sidewall electric field between these two lines results in a fringing (or coupling) capacitance as shown in Fig. 1 [11,12,14–16].

In a CMOS integrated circuit, interconnect lines are typically driven by CMOS logic gates. Therefore, the CMOS logic gates driving adjacent interconnect lines are capacitively coupled. A circuit diagram of N capacitively coupled interconnect lines driven by N CMOS inverters is shown in Fig. 2. This coupled system can be analyzed by applying a two-line coupled structure to line 1 and 2 as well as line $N-1$ and N, and modeling the remaining adjacent lines using a three-line coupled structure.

In order to simplify this analysis as well as emphasize the nonlinear behavior of a CMOS inverter during a logic transition, the interconnect is modeled as a lumped resistive–capacitive load where R_1 (R_2, R_3) is the parasitic resistance of line 1 (2, 3) and C_1 (C_2, C_3) includes both the self-interconnect capacitance of line 1 (2, 3) and the gate capacitance of the following logic stage. C_c is the coupling (or fringing) capacitance in a two-line structure while C_{12} and C_{23} are the coupling (or fringing) capacitances between two neighboring interconnect lines 1 and 2, and 2 and 3, respectively, in a three-line system. The output voltages (V_1, V_2, and V_3) and currents (I_1, I_2, and I_3) are shown in Figs. 3 and 4 for a two-line and a three-line coupled structure, respectively. Differential equations characterizing the behavior of a coupled system are listed in Table 1 for both a two-line and a three-line coupled structure [34].

The transient response of a single CMOS inverter within a coupled system strongly depends upon the signal activity of each inverter. There are three possible conditions for each inverter, a high-to-low transition, a low-to-high transition, and a quiet state in which the output voltage of the inverter remains at either the voltage supply level (V_{dd}) or ground. A high-to-low or low-to-high transition is described as a dynamic transition. If the signal at the input of each inverter is purely random and uncorrelated, there are a total of nine (9) (as listed in Table 2) and twenty seven (27) (as listed in Table 3) possible signal combinations which can occur for a two-line and a three-line coupled system, respectively.

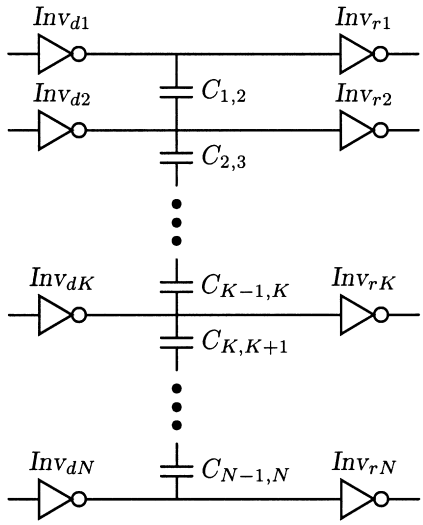

Fig. 2. A circuit structure of N coupled interconnect lines driven by N CMOS inverters.

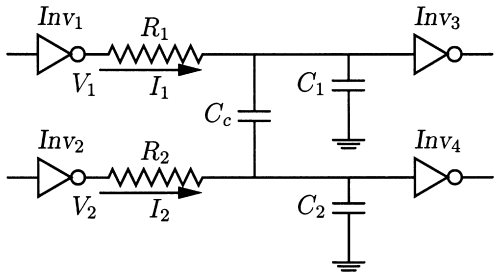

Fig. 3. A circuit diagram of two coupled resistive–capacitive interconnections driven by CMOS inverters.

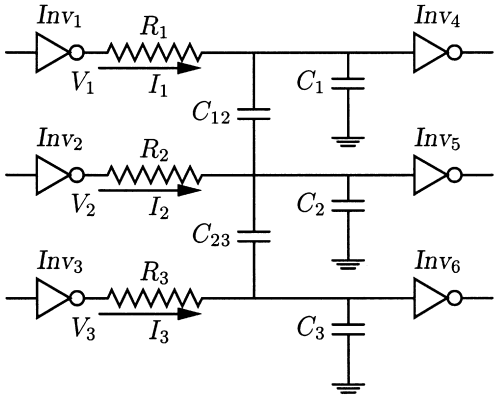

Fig. 4. A circuit diagram of three coupled resistive–capacitive interconnections driven by CMOS inverters.

Table 1
Differential equations characterizing a system of coupled resistive–capacitive interconnections

Two coupled resistive–capacitive interconnections
$(C_1 + C_c)\frac{dV_1}{dt} - C_c\frac{dV_2}{dt} = I_1 + R_1(C_1 + C_c)\frac{dI_1}{dt} - R_2C_c\frac{dI_2}{dt}$
$(C_2 + C_c)\frac{dV_2}{dt} - C_c\frac{dV_1}{dt} = I_2 + R_2(C_2 + C_c)\frac{dI_2}{dt} - R_1C_c\frac{dI_1}{dt}$
Three coupled resistive–capacitive interconnections
$(C_1 + C_{12})\frac{dV_1}{dt} - C_{12}\frac{dV_2}{dt} = I_1 + R_1(C_1 + C_{12})\frac{dI_1}{dt} - R_2C_{12}\frac{dI_2}{dt}$
$(C_2 + C_{12} + C_{23})\frac{dV_2}{dt} - C_{12}\frac{dV_1}{dt} - C_{23}\frac{dV_3}{dt} = I_2 + R_2(C_2 + C_{12} + C_{23})\frac{dI_2}{dt} - R_1C_{12}\frac{dI_1}{dt} - R_3C_{23}\frac{dI_3}{dt}$
$(C_3 + C_{23})\frac{dV_3}{dt} - C_{23}\frac{dV_2}{dt} = I_3 + R_3(C_3 + C_{23})\frac{dI_3}{dt} - R_2C_{23}\frac{dI_2}{dt}$

Table 2
Possible signal activities for a two-line coupled system

V_{in1}	Inv_1	V_{in2}	Inv_2	
0 to V_{dd}	High-to-low	0 to V_{dd}	High-to-low	In-phase
		V_{dd} to 0	Low-to-high	Out-of-phase
		V_{dd} or 0	Quiet	One active/one quiet
V_{dd} to 0	Low-to-high	0 to V_{dd}	High-to-low	Out-of-phase
		V_{dd} to 0	Low-to-high	In-phase
		0 or V_{dd}	Quiet	One active/one quiet
V_{dd} or 0	Quiet	0 to V_{dd}	High-to-low	One active/one quiet
		V_{dd} to 0	Low-to-high	One active/one quiet
		0 or V_{dd}	Quiet	No transition

In the following analysis, if the CMOS inverters within a coupled system are dynamically transitioning, it is assumed that these inverters are triggered at the same time and at the same input slew rate. During a dynamic transition, only the active transistor in each inverter is considered in the development of the analytical expressions describing the waveform of the output voltage. The MOS transistors are characterized by the nth power law I–V model in the saturation region and the effective output conductance γ in the linear region [37–39].

3. In-phase transition

An in-phase transition, in which all inverters have the same dynamic transitions, is an optimistic condition in terms of the effect of the interconnect coupling capacitance on the propagation delay of a CMOS inverter [24,34]. The probability of an in-phase transition is $\frac{2}{9}$ for a two-line coupled

Table 3
Possible signal activities for a three-line coupled system

V_{in1}	Inv_1	V_{in2}	Inv_2	V_{in3}	Inv_3
				0 to V_{dd}	High-to-low
		0 to V_{dd}	High-to-low	V_{dd} to 0	Low-to-high
				V_{dd} or 0	Quiet
				0 to V_{dd}	High-to-low
0 to V_{dd}	High-to-low	V_{dd} to 0	Low-to-high	V_{dd} to 0	Low-to-high
				V_{dd} or 0	Quiet
				0 to V_{dd}	High-to-low
		0 or V_{dd}	Quiet	V_{dd} to 0	Low-to-high
				V_{dd} or 0	Quiet
				0 to V_{dd}	High-to-low
		0 to V_{dd}	High-to-low	V_{dd} to 0	Low-to-high
				V_{dd} or 0	Quiet
				0 to V_{dd}	High-to-low
V_{dd} to 0	Low-to-high	V_{dd} to 0	Low-to-high	V_{dd} to 0	Low-to-high
				V_{dd} or 0	Quiet
				0 to V_{dd}	High-to-low
		0 or V_{dd}	Quiet	V_{dd} to 0	Low-to-high
				V_{dd} or 0	Quiet
				0 to V_{dd}	High-to-low
		0 to V_{dd}	High-to-low	V_{dd} to 0	Low-to-high
				V_{dd} or 0	Quiet
				0 to V_{dd}	High-to-low
V_{dd} or 0	Quiet	V_{dd} to 0	Low-to-high	V_{dd} to 0	Low-to-high
				V_{dd} or 0	Quiet
				0 to V_{dd}	High-to-low
		0 or V_{dd}	Quiet	V_{dd} to 0	Low-to-high
				V_{dd} or 0	Quiet

system (as listed in Table 2) and $\frac{2}{27}$ (see Table 3) for a three-line coupled system, respectively. In this section, analytical expressions characterizing the output voltage, the effective capacitive load, and the propagation delay of each CMOS inverter within a two-line and a three-line coupled system are presented. The analytic propagation delay is also compared in this section to SPICE [36].

3.1. The output voltage of each CMOS inverter

For a two-line coupled system, the outputs of both inverters are assumed to transition from high-to-low. The PMOS transistors are neglected based on an assumption of a fast ramp input signal [40]. $NMOS_1$ and $NMOS_2$ are the active transistors in each inverter and may have different geometric sizes. The shape of the input signals driving each inverter is

Table 4
Analytical expressions characterizing the output voltage of a CMOS inverter driving an *RC* load within a two-line coupled system for an in-phase transition

Operation region	Output voltage $V_1(t)$ and $V_2(t)$
$[\tau_n,\tau_r]$	$V_1 = V_{dd} - \beta_{21}\frac{\tau_r}{(n_n+1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1} - R_1 B_{n1}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}$
	$V_2 = V_{dd} - \beta_{22}\frac{\tau_r}{(n_n+1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1} - R_2 B_{n2}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}$
	$\beta_{21} = \frac{(C_2+C_c)B_{n1}+C_c B_{n2}}{C_1C_2+C_c(C_1+C_2)}$
	$\beta_{22} = \frac{(C_1+C_c)B_{n2}+C_c B_{n1}}{C_1C_2+C_c(C_1+C_2)}$
$[\tau_r,\tau_{sat}^{min}]$	$V_1 = V_1(\tau_r) - \beta_{21}(V_{dd} - V_{TN})^{n_n}(t-\tau_r)$
	$V_2 = V_2(\tau_r) - \beta_{22}(V_{dd} - V_{TN})^{n_n}(t-\tau_r)$
	$\tau_{sat}^{min} = \min(\tau_{nsat}^1,\tau_{nsat}^2)$
	$\tau_{sat}^{max} = \max(\tau_{nsat}^1,\tau_{nsat}^2)$
$[\tau_{sat}^{min},\tau_{sat}^{max}]$	$V_1 = -V_{1a} + (V_{nsat} + V_{1a})e^{-\alpha_{n1}(t-\tau_{nsat}^1)}$
	$V_2 = V_2(\tau_{nsat}^1) - \frac{B_{n2}}{C_2+C_c}(V_{dd} - V_{TN})^{n_n}(t-\tau_{nsat}^1) - V_{2a}$
	$V_{1a} = \frac{C_c}{(C_2+C_c)\gamma_{n1}}B_{n2}(V_{dd} - V_{TN})^{n_n}$
	$\alpha_{n1} = -\frac{\gamma_{n1}(C_2+C_c)}{(1+R_1\gamma_{n1})(C_1C_2+C_c(C_1+C_2))}$
	$V_{2a} = \frac{C_c}{C_2+C_c}(1+R_1\gamma_{n1})(V_{nsat}+V_{1a})(1-e^{-\alpha_{n1}(t-\tau_{nsat}^1)})$
$t \geqslant \tau_{sat}^{max}$	$V_1 = \frac{K_1}{2}[e^{-\nu_1 t} + e^{-\nu_2 t} + \frac{\chi_c}{\chi_a}(e^{-\nu_1 t} - e^{-\nu_2 t})] + \frac{\chi_d}{\chi_a}K_2(e^{-\nu_1 t} - e^{-\nu_2 t})$
	$V_2 = \frac{K_2}{2}[e^{-\nu_1 t} + e^{-\nu_2 t} - \frac{\chi_c}{\chi_a}(e^{-\nu_1 t} - e^{-\nu_2 t})] + \frac{\chi_c}{\chi_a}K_1(e^{-\nu_1 t} - e^{-\nu_2 t})$
	$\nu_1 = \frac{1+R_1\gamma_{n1}}{1+R_2\gamma_{n2}}\cdot\frac{\chi_b+\chi_a}{C_1C_2+C_c(C_1+C_2)}$
	$\nu_2 = \frac{1+R_1\gamma_{n1}}{1+R_2\gamma_{n2}}\cdot\frac{\chi_b-\chi_a}{C_1C_2+C_c(C_1+C_2)}$
	$\chi_a = \sqrt{\chi_c^2 + 4\gamma_{n1}\gamma_{n2}C_c^2(1+R_1\gamma_{n1})(1+R_2\gamma_{n2})}$
	$\chi_b = \gamma_{n1}(1+R_2\gamma_{n2})(C_2+C_c) + \gamma_{n2}(1+R_1\gamma_{n1})(C_1+C_c)$
	$\chi_c = \gamma_{n1}(1+R_2\gamma_{n2})(C_2+C_c) - \gamma_{n2}(1+R_1\gamma_{n1})(C_1+C_c)$
	$\chi_d = \gamma_{n2}(1+R_2\gamma_{n2})C_c$
	$\chi_e = \gamma_{n1}(1+R_1\gamma_{n1})C_c$

characterized by a ramp signal,

$$V_{in} = \frac{t}{\tau_r}V_{dd} \quad \text{for } 0 \leqslant t \leqslant \tau_r. \tag{6}$$

An assumption of a fast ramp input signal supports the condition that each inverter operates in the saturation region before the input transition is completed. Analytical expressions characterizing the output voltages, V_1 and V_2, are listed in Table 4. τ_n is the time when the NMOS transistor turns

Table 5
Analytical expressions characterizing the output voltage of a CMOS inverter driving an *RC* load for an in-phase transition within a three-line coupled system

Operation region	Output voltage $V_1(t)$, $V_2(t)$, and $V_3(t)$
$[\tau_n,\tau_r]$	$V_1 = V_{dd} - \beta_{31}\frac{\tau_r}{(n_n+1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1} - R_1 B_{n1}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}$
	$V_2 = V_{dd} - \beta_{32}\frac{\tau_r}{(n_n+1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1} - R_2 B_{n2}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}$
	$V_3 = V_{dd} - \beta_{33}\frac{\tau_r}{(n_n+1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1} - R_2 B_{n3}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}$
	$\beta_{31} = \frac{C_{2t} - C_{23}^2/C_{3t}}{C_{1t}(C_{2t} - C_{23}^2/C_{3t}) - C_{12}^2}[B_{n1} + \frac{C_{12}}{C_{2t} - C_{23}^2/C_{3t}}B_{n2} + \frac{C_{23}}{C_{3t}}\frac{C_{12}}{C_{2t} - C_{23}^2/C_{3t}}B_{n3}]$
	$\beta_{32} = \frac{1}{C_{2t} - C_{12}^2/C_{1t} - C_{23}^2/C_{3t}}(\frac{C_{12}}{C_{1t}}B_{n1} + B_{n2} + \frac{C_{23}}{C_{3t}}B_{n3})$
	$\beta_{33} = \frac{C_{2t} - C_{12}^2/C_{1t}}{C_{1t}(C_{2t} - C_{12}^2/C_{1t}) - C_{23}^2}[B_{n3} + \frac{C_{23}}{C_{2t} - C_{12}^2/C_{1t}}B_{n2} + \frac{C_{12}}{C_{1t}}\frac{C_{23}}{C_{2t} - C_{12}^2/C_{1t}}B_{n1}]$
	$C_{1t} = C_1 + C_{12}$
	$C_{2t} = C_2 + C_{12} + C_{23}$
	$C_{3t} = C_3 + C_{23}$
$[\tau_r,\tau_{sat}^{min}]$	$V_1 = V_1(\tau_r) - \beta_{31}(V_{dd} - V_{TN})^{n_n}(t - \tau_r)$
	$V_2 = V_2(\tau_r) - \beta_{32}(V_{dd} - V_{TN})^{n_n}(t - \tau_r)$
	$V_3 = V_3(\tau_r) - \beta_{33}(V_{dd} - V_{TN})^{n_n}(t - \tau_r)$
	$\tau_{sat}^{min} = \min(\tau_{nsat}^1,\tau_{nsat}^2,\tau_{nsat}^3)$

ON where $\tau_n = (V_{TN}/V_{dd})\tau_r$. τ_{nsat}^1 and τ_{nsat}^2 are the duration times when $NMOS_1$ and $NMOS_2$ operate in the saturation region, respectively. These times can be determined from (11) and (12). It is assumed in this analysis that $NMOS_1$ leaves the saturation region first, i.e., $\tau_{nsat}^1 < \tau_{nsat}^2$. After τ_{sat}^{max} [defined in (13)], both of the NMOS transistors operate in the linear region. K_1 and K_2 [defined in (20) and (21)] are integration constants which can be determined from $V_1(\tau_{sat}^{max})$ and $V_2(\tau_{sat}^{max})$ which are initial value of V_1 and V_2 at τ_{sat}^{max}, respectively .

For a three-line coupled system, $NMOS_1$, $NMOS_2$, and $NMOS_3$ are the active transistors in each CMOS inverter. Following the same procedure as for the two-line coupled system, analytical expressions characterizing the output voltage of each CMOS inverter are listed in Table 5 before one of these three active NMOS transistors starts to operate in the linear region. The analytical solutions of the output voltages, V_1, V_2, and V_3, after τ_{sat}^{min} [defined in (14)] are presented in Appendix B.

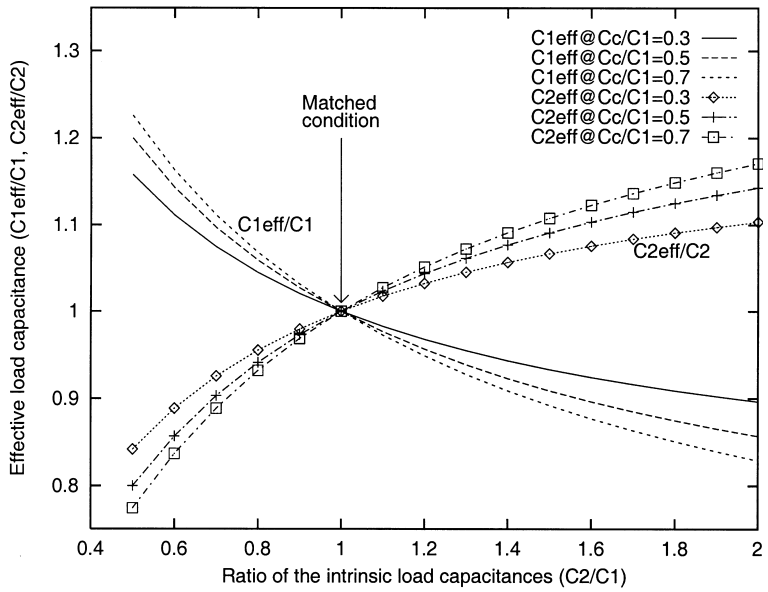

Fig. 5. The ratio of the effective load capacitances $C_{n1_{eff}}$ and $C_{n2_{eff}}$ to C_1 and C_2, respectively, for an in-phase transition assuming $B_{n1} = B_{n2}$.

3.2. *Effective capacitive load of each CMOS inverter*

For a two-line coupled system, the effective capacitive load of each inverter in an in-phase transition is

$$C_{1_{eff}} = \frac{C_1 C_2 + C_c(C_1 + C_2)}{C_2 + (1 + B_{n2}/B_{n1})C_c}, \tag{42}$$

$$C_{2_{eff}} = \frac{C_1 C_2 + C_c(C_1 + C_2)}{C_1 + (1 + B_{n1}/B_{n2})C_c}, \tag{43}$$

respectively. Assuming B_{n1} is equal to B_{n2}, i.e., both NMOS transistors have the same geometric sizes (or output gain), the effective load capacitance of each inverter is shown in Fig. 5. The solid lines shown in Fig. 5 depict the ratio of $C_{1_{eff}}$ to C_1 and the dotted lines represent the ratio of $C_{2_{eff}}$ to C_2. The horizontal axis represents the ratio of C_2 to C_1, which characterizes the difference between the intrinsic load capacitances. Ratios of the coupling capacitance to the line capacitance, C_c to C_1, of 0.3, 0.5, and 0.7 are considered. Note that the deviation of the effective load capacitances from the intrinsic capacitances (C_1 and C_2) increases if the difference between the intrinsic load capacitances increases. The deviation also increases with increasing coupling capacitance for the same ratio of C_2/C_1. Note in Fig. 5 that the effective load capacitance of one inverter increases above the corresponding intrinsic load capacitance while the effective load capacitance of the second inverter drops below the corresponding intrinsic load capacitance. The deviation of the effective load capacitances from the intrinsic load capacitances results in different propagation delays.

For a three-line coupled system, the effective capacitive load of each CMOS inverter is

$$C_{1_{\text{eff}}} = \frac{C_{1t} - C_{12}^2/(C_{2t} - C_{23}^2/C_{3t})}{1 + [C_{12}/(C_{2t} - C_{23}^2/C_{3t})]B_{\text{n}2}/B_{\text{n}1} + (C_{23}/C_{3t})[C_{12}/(C_{2t} - C_{23}^2/C_{3t})]B_{\text{n}3}/B_{\text{n}1}}, \quad (44)$$

$$C_{2_{\text{eff}}} = \frac{C_{2t} - (C_{12}/C_{1t})C_{12} - (C_{23}/C_{3t})C_{23}}{(C_{12}/C_{1t})B_{\text{n}1}/B_{\text{n}2} + 1 + (C_{23}/C_{3t})B_{\text{n}3}/B_{\text{n}2}}, \quad (45)$$

$$C_{3_{\text{eff}}} = \frac{C_{3t} - C_{23}^2/(C_{2t} - C_{12}^2/C_{1t})}{(C_{12}/C_{1t})[C_{23}/(C_{2t} - C_{12}^2/C_{1t})]B_{\text{n}1}/B_{\text{n}3} + [C_{23}/(C_{2t} - C_{12}^2/C_{1t})]B_{\text{n}2}/B_{\text{n}3} + 1}, \quad (46)$$

respectively. Note that the effective capacitive load of each CMOS inverter depends not only upon the intrinsic load capacitance and the coupling capacitance but also the transconductance of each active transistor (the geometric size and device characteristics of each active transistor).

3.3. Propagation delay time

The propagation delay $t_{0.5}$ of a CMOS inverter is defined here as the time from 50% V_{dd} of the input to 50% V_{dd} of the output. For a high-to-low transition at the output, if V_{nsat} is greater than $0.5V_{\text{dd}}$, the time when the output voltage reaches $0.5V_{\text{dd}}$ can be determined from an analytic expression characterizing the transistor operating within the saturation region. If V_{nsat} is less than $0.5V_{\text{dd}}$, the time when the output voltage reaches $0.5V_{\text{dd}}$ occurs primarily when the transistor operates within the linear region. Note that the analytical expressions, (20) and (21), listed in Table 4 characterizing the output voltages in the linear region are intractable and do not permit a closed form analytical expression characterizing the propagation delay of a CMOS inverter to be developed. In the following analysis, analytical expressions characterizing the transistor operating in the saturation region are extrapolated to approximate the time for the output signal to reach $0.5V_{\text{dd}}$ [37,38]. Therefore, based on this assumption, analytical expressions characterizing the propagation delay of each CMOS inverter within a two-line and a three-line coupled system are listed in Table 6.

The effect of the interconnect coupling capacitance on the propagation delay is characterized by β_{21} and β_{22} [defined by (9) and (10), respectively] for a two-line coupled system and β_{31}, β_{32}, and β_{33} [defined by (32), (33), and (34), respectively] for a three-line coupled system. Note that the propagation delay also depends upon the intrinsic capacitive loads, the coupling capacitances, and the size of each active transistor, which is the same observation as for the effective capacitive load of each CMOS inverter.

A comparison of the propagation delay based on these analytical expressions with SPICE is listed in Tables 7 and 8. *No coupling* is defined as the condition under which the propagation delay is estimated based solely on the intrinsic load capacitance [3,32,34]. The maximum error under the *no coupling* condition can exceed 50% as compared to SPICE for a two-line and a three-line coupled system while the maximum error of the analytic propagation delay model listed in Table 6 is within 9% of SPICE. For a two-line coupled structure, the maximum and average improvement of the proposed propagation delay model are about 46% and 19% of SPICE, respectively; while the maximum and average improvement for a three-line coupled system are 44% and 20% of SPICE, respectively, as listed in Tables 7 and 8.

Table 6
Propagation delay of a CMOS inverter for an in-phase transition

Two coupled resistive–capacitive lines
$t_{P_{HL1}} = \frac{0.5V_{dd} - R_1 B_{n1}(V_{dd} - V_{TN})^{\alpha_n}}{\beta_{21}(V_{dd} - V_{TN})^{\alpha_n}} - \frac{\tau_r(V_{dd} - V_{TN})}{(\alpha_n + 1)V_{dd}} + \tau_r$
$t_{P_{HL2}} = \frac{0.5V_{dd} - R_2 B_{n2}(V_{dd} - V_{TN})^{\alpha_n}}{\beta_{22}(V_{dd} - V_{TN})^{\alpha_n}} - \frac{\tau_r(V_{dd} - V_{TN})}{(\alpha_n + 1)V_{dd}} + \tau_r$
Three coupled resistive–capacitive lines
$t_{P_{HL1}} = \frac{0.5V_{dd} - R_1 B_{n1}(V_{dd} - V_{TN})^{\alpha_n}}{\beta_{31}(V_{dd} - V_{TN})^{\alpha_n}} - \frac{\tau_r(V_{dd} - V_{TN})}{(\alpha_n + 1)V_{dd}} + \tau_r$
$t_{P_{HL2}} = \frac{0.5V_{dd} - R_2 B_{n2}(V_{dd} - V_{TN})^{\alpha_n}}{\beta_{32}(V_{dd} - V_{TN})^{\alpha_n}} - \frac{\tau_r(V_{dd} - V_{TN})}{(\alpha_n + 1)V_{dd}} + \tau_r$
$t_{P_{HL3}} = \frac{0.5V_{dd} - R_3 B_{n3}(V_{dd} - V_{TN})^{\alpha_n}}{\beta_{33}(V_{dd} - V_{TN})^{\alpha_n}} - \frac{\tau_r(V_{dd} - V_{TN})}{(\alpha_n + 1)V_{dd}} + \tau_r$

Table 7
Comparison of an in-phase transition with SPICE for a two-line coupled system

	Circuit parameters							SPICE		No coupling				Analytic estimation			
τ_r (ns)	w_{n1} (μm)	R_1 (Ω)	C_1 (pF)	w_{n2} (μm)	R_2 (Ω)	C_2 (pF)	C_c (pF)	τ_1 (ps)	τ_2 (ps)	τ_1 (ps)	τ_2 (ps)	δ_1 (%)	δ_2 (%)	τ_1 (ps)	τ_2 (ps)	δ_1 (%)	δ_2 (%)
0.2	1.8	100	0.2	1.8	100	0.2	0.1	312	312	297	297	4.8	4.8	297	297	4.8	4.8
0.2	1.8	100	0.1	1.8	100	0.2	0.1	210	270	160	296	23.8	9.6	195	252	7.15	6.67
0.2	1.8	100	0.2	1.8	100	0.1	0.1	270	210	296	160	9.63	23.81	252	195	6.67	7.15
0.2	1.8	300	0.1	3.6	100	0.3	0.1	177	219	82	202	53.67	7.76	165	213	6.78	2.74
0.2	3.6	100	0.3	1.8	300	0.1	0.1	219	177	202	82	7.76	53.67	213	165	2.74	6.78
0.2	1.8	100	0.2	3.6	100	0.4	0.1	310	294	160	276	48.38	6.12	298	281	3.87	4.42
0.2	3.6	100	0.4	1.8	100	0.2	0.1	294	310	276	160	6.12	48.38	281	298	4.42	3.87
0.3	1.8	200	0.2	3.6	200	0.4	0.2	310	270	163	249	47.42	7.78	290	258	6.45	4.40
0.3	3.6	200	0.4	1.8	200	0.2	0.2	270	310	249	163	7.78	47.42	258	290	4.40	6.45
0.3	1.8	100	0.2	3.6	100	0.3	0.2	300	251	173	226	42.33	9.96	282	243	6.0	3.2
0.3	3.6	100	0.3	1.8	100	0.2	0.2	251	300	226	173	9.96	42.33	243	282	3.2	6.0
0.5	1.8	100	0.2	3.6	100	0.4	0.1	355	337	198	314	44.22	6.82	335	318	5.64	5.60
0.5	3.6	100	0.4	1.8	100	0.2	0.1	337	355	314	198	6.82	44.22	318	335	5.60	5.64
Statistical analysis						No coupling				Analytic estimation				Improvement			
Maximum error (%)						53.67				7.15				46.52			
Average error (%)						24.61				5.21				19.52			

4. Out-of-phase transition

An out-of-phase transition is a pessimistic condition in terms of the effect of the interconnect coupling capacitance on the propagation delay of a CMOS inverter [24,34]. Analytical expressions characterizing the output voltage, the effective capacitive load, and the propagation delay of each CMOS inverter within a two-line and a three-line coupled system are developed in this section for

Table 8
Comparison of an in-phase transition with SPICE for a three-line coupled system

	Circuit parameters											SPICE No coupling			Analytic	
τ_r (ns)	w_{n1} (μm)	R_1 (Ω)	C_1 (pF)	w_{n2} (μm)	R_2 (Ω)	C_2 (pF)	w_{n3} (μm)	R_3 (Ω)	C_3 (pF)	C_{12} (pF)	C_{23} (pF)	τ_2 (ps)	τ_2 (ps)	δ_2 (%)	τ_2 (ps)	δ_2 (%)
0.2	1.8	80	0.1	3.6	100	0.15	1.8	90	0.08	0.05	0.05	139	124	10.79	131	6.10
0.2	1.8	80	0.1	3.6	100	0.15	1.8	90	0.1	0.1	0.1	145	124	14.48	137	5.52
0.2	3.6	100	0.1	3.6	100	0.2	3.6	100	0.1	0.1	0.1	136	158	16.17	126	7.35
0.2	3.6	100	0.1	3.6	100	0.3	3.6	100	0.1	0.1	0.1	170	224	31.76	158	7.06
0.2	3.6	100	0.1	3.6	100	0.2	3.6	100	0.2	0.1	0.1	150	158	5.3	143	4.67
0.2	3.6	100	0.1	3.6	200	0.4	3.6	100	0.1	0.1	0.1	180	248	37.78	165	8.33
0.2	3.6	100	0.1	3.6	200	0.4	3.6	100	0.1	0.2	0.2	166	248	49.40	153	7.83
0.2	3.6	100	0.1	3.6	200	0.5	3.6	100	0.1	0.2	0.2	189	289	52.91	176	6.88
Statistical analysis					No coupling				Analytic estimation				Improvement			
Maximum error (%)					52.91				8.33				44.58			
Average error (%)					27.32				6.72				20.60			

an out-of-phase transition. A comparison of the analytic estimations with SPICE is also presented in this section.

4.1. The output voltage of each CMOS inverter

For a two-line coupled system, an out-of-phase transition has the same probability as an in-phase transition. It is assumed in this section that the output of Inv_1 transitions from high-to-low while the output of Inv_2 transitions from low-to-high. $NMOS_1$ and $PMOS_2$ are the active transistors in each inverter. The input signals are

$$V_{in1} = \frac{t}{\tau_r} V_{dd} \quad \text{for } 0 \leqslant t \leqslant \tau_r, \tag{52}$$

$$V_{in2} = \left(1 - \frac{t}{\tau_r}\right) V_{dd} \quad \text{for } 0 \leqslant t \leqslant \tau_r. \tag{53}$$

The initial states of V_1 and V_2 are V_{dd} and ground, respectively. It is assumed in this analysis that the absolute value of the threshold voltages of the NMOS and PMOS transistors are approximately equal. In the following analysis, parameters describing the voltages of the PMOS transistor are absolute values. Analytical expressions characterizing the output voltage for a two-line coupled systems are listed in Table 9 assuming $PMOS_2$ starts operating in the linear region. When both active transistors operate in the linear region, a solution of the output voltages can be obtained by following the same procedure as for an in-phase transition, as elaborated in Appendix A.

Table 9
Analytical expressions characterizing the output voltage of a CMOS inverter driving an *RC* load within a two-line coupled system for an out-of-phase transition

Operation region	Output voltage $V_1(t)$ and $V_2(t)$
$[\tau_n(\tau_p),\tau_r]$	$V_1 = V_{dd} - \frac{(C_2+C_c)V_{n,1}-C_cV_{p,1}}{C_1C_2+C_c(C_1+C_2)} - R_1B_{n1}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}$
	$V_2 = \frac{(C_1+C_c)V_{p,1}-C_cV_{n,1}}{C_1C_2+C_c(C_1+C_2)} + R_2B_{p2}(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p}$
	$V_{n,1} = B_{n1}\frac{\tau_r}{(n_n+1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1}$
	$V_{p,1} = B_{p2}\frac{\tau_r}{(n_p+1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p+1}$
$[\tau_r,\tau_{sat}^{min}]$	$V_1 = V_1(\tau_r) - \frac{(C_2+C_c)V_{n,2}-C_cV_{p,2}}{C_1C_2+C_c(C_1+C_2)}(t-\tau_r)$
	$V_2 = V_2(\tau_r) + \frac{(C_1+C_c)V_{p,2}-C_cV_{n,2}}{C_1C_2+C_c(C_1+C_2)}(t-\tau_r)$
	$V_{n,2} = B_{n1}(V_{dd} - V_{TN})^{n_n}$
	$V_{p,2} = B_{p2}(V_{dd} - V_{TP})^{n_p}$
	$\tau_{sat}^{min} = \min(\tau_{nsat}^1,\tau_{psat}^2)$
	$\tau_{sat}^{max} = \max(\tau_{nsat}^1,\tau_{psat}^2)$
$[\tau_{sat}^{min},\tau_{sat}^{max}]$	$V_1 = V_1(\tau_{sat}^{min}) + V_{n,3}(t-\tau_{sat}^{min}) + \frac{C_c(1+R_2\gamma_{p2})}{C_1+C_c}(V_{psat} - V_{p,3})(1 - e^{-\alpha_{p2}(t-\tau_{sat}^{min})})$
	$V_2 = V_{dd} - V_{p,3} - (V_{psat} - V_{p,3})e^{-\alpha_{p2}(t-\tau_{sat}^{min})}$
	$V_{n,3} = \frac{1}{C_1+C_c}B_{n1}(V_{dd} - V_{TN})^{n_n}$
	$V_{p,3} = \frac{C_c}{(C_1+C_c)\gamma_{p2}}B_{n1}(V_{dd} - V_{TN})^{n_n}$
	$\alpha_{p2} = \frac{\gamma_{p2}(C_1+C_c)}{(1+R_2\gamma_{p2})(C_1C_2+C_c(C_1+C_2))}$

For a three-line coupled system, as shown in Fig. 4, an out-of-phase transition is defined where the middle line (driven by Inv_2) dynamically transitions opposite to that of the neighboring lines (driven by Inv_1 and Inv_3). The probability of this occurrence is $\frac{2}{27}$ (see Table 3). For example, the output of Inv_2 transitions from high-to-low while the outputs of Inv_1 and Inv_3 transition from low-to-high. Assuming the input signal has the same waveform shape as a two-line coupled system, $PMOS_1$, $NMOS_2$, and $PMOS_3$ are the active transistors in each of the CMOS inverters. The initial value of V_1, V_2, and V_3 are ground, V_{dd}, and ground, respectively. Analytical expressions characterizing the output voltage of each CMOS inverter before one of these three active transistors starts operating in the linear region are listed in Table 10.

For a three-line coupled system, there are several signal combinations where the effect of the interconnect coupling capacitance on the propagation delay of Inv_2 lies between an in-phase and an out-of-phase transition. These combinations have the probability of $\frac{4}{27}$ (see Table 3). For example, the outputs of Inv_1 and Inv_2 transition from high-to-low while the output of Inv_3 transitions from low-to-high. Under this condition, $NMOS_1$, $NMOS_2$, and $PMOS_3$ are the active transistors in each CMOS inverter. The initial value of V_1, V_2, and V_3 are V_{dd}, V_{dd}, and ground, respectively. Analytical expressions characterizing the output voltage of each CMOS inverter

Table 10
Analytical expressions characterizing the output voltage of a CMOS inverter driving an *RC* load within a three-line coupled system. Inv_2 transitions from high-to-low while Inv_1 and Inv_3 transition from low-to-high

Region	Output voltage $V_1(t)$, $V_2(t)$, and $V_3(t)$
$[\tau_n,\tau_r]$	$V_1 = \frac{C_{2t}-C_{23}^2/C_{3t}}{C_{1t}(C_{2t}-C_{23}^2/C_{3t})-C_{12}^2}(V_{p1,1} - \frac{C_{12}}{C_{2t}-C_{23}^2/C_{3t}}V_{n2,1} + \frac{C_{23}}{C_{3t}} \cdot \frac{C_{12}}{C_{2t}-C_{23}^2/C_{3t}}V_{p3,1})$
	$+ R_1 B_{p1}(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p}$
	$V_2 = V_{dd} - \frac{1}{C_{2t}-C_{12}^2/C_{1t}-C_{23}^2/C_{3t}}(V_{n2,1} - \frac{C_{12}}{C_{1t}}V_{p1,1} - \frac{C_{23}}{C_{3t}}V_{p3,1}) - R_2 B_{n2}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}$
	$V_3 = \frac{C_{2t}-C_{12}^2/C_{1t}}{C_{3t}(C_{2t}-C_{12}^2/C_{1t})-C_{23}^2}(V_{p3,1} - \frac{C_{23}}{C_{2t}-C_{12}^2/C_{1t}}V_{n2,1} + \frac{C_{12}}{C_{1t}} \cdot \frac{C_{23}}{C_{2t}-C_{12}^2/C_{1t}}V_{p1,1})$
	$+ R_3 B_{p3}(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p}$
	$V_{p1,1} = \frac{\tau_r}{(n_p+1)V_{dd}}B_{p1}(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p+1}$
	$V_{n2,1} = \frac{\tau_r}{(n_n+1)V_{dd}}B_{n2}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1}$
	$V_{p3,1} = \frac{\tau_r}{(n_p+1)V_{dd}}B_{p3}(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p+1}$
$[\tau_r,\tau_{sat}^{min}]$	$V_1 = V_1(\tau_r) + \frac{C_{2t}-C_{23}^2/C_{3t}}{C_{1t}(C_{2t}-C_{23}^2/C_{3t})-C_{12}^2}(V_{p1,2} - \frac{C_{12}}{C_{2t}-C_{23}^2/C_{3t}}V_{n2,2} + \frac{C_{23}}{C_{3t}} \cdot \frac{C_{12}}{C_{2t}-C_{23}^2/C_{3t}}V_{p3,2})(t-\tau_r)$
	$V_2 = V_2(\tau_r) - \frac{1}{C_{2t}-C_{12}^2/C_{1t}-C_{23}^2/C_{3t}}(V_{n2,2} - \frac{C_{12}}{C_{1t}}V_{p1,2} - \frac{C_{23}}{C_{3t}}V_{p3,2})(t-\tau_r)$
	$V_3 = V_3(\tau_r) + \frac{C_{2t}-C_{12}^2/C_{1t}}{C_{3t}(C_{2t}-C_{12}^2/C_{1t})-C_{23}^2}(V_{p3,2} - \frac{C_{23}}{C_{2t}-C_{12}^2/C_{1t}}V_{n2,2} + \frac{C_{12}}{C_{1t}} \cdot \frac{C_{23}}{C_{2t}-C_{12}^2/C_{1t}}V_{p1,2})(t-\tau_r)$
	$V_{p1,2} = B_{p1}(V_{dd} - V_{TP})^{n_p}$
	$V_{n2,2} = B_{n2}(V_{dd} - V_{TN})^{n_n}$
	$V_{p3,2} = B_{p3}(V_{dd} - V_{TP})^{n_p}$
	$\tau_{sat}^{min} = \min(\tau_{psat}^1,\tau_{nsat}^2,\tau_{psat}^3)$

before one of these three active transistors begins operating in the linear region are listed in Table 11.

4.2. Effective capacitive load of each CMOS inverter

In order to simplify the analysis of the effective capacitive load of each CMOS inverter for an out-of-phase transition, it is assumed that both the NMOS and PMOS transistors have similar I–V characteristics in a dynamic transition, i.e.,

$$\frac{((t/\tau_r)V_{dd} - V_{TN})^{n_n+1}}{n_n+1} = \frac{((t/\tau_r)V_{dd} - V_{TP})^{n_p+1}}{n_p+1}, \tag{95}$$

where $\tau_n \leqslant t \leqslant \tau_r$, which is the ideal condition ensuring both rising and falling edges of the on-chip signals to be similar. For a two-line coupled system, the effective capacitive load of each inverter in

Table 11
Analytical expressions characterizing the output voltage of a CMOS inverter driving an *RC* load within a three-line coupled system. Inv_1 and Inv_2 transition from high-to-low while Inv_3 transitions from low-to-high

Region	Output voltage $V_1(t)$, $V_2(t)$, and $V_3(t)$3
$[\tau_n,\tau_r]$	$V_1 = V_{dd} - \frac{C_{2t}-C_{23}^2/C_{3t}}{C_{1t}(C_{2t}-C_{23}^2/C_{3t})}(V_{n1,1} + \frac{C_{12}}{C_{2t}-C_{23}^2/C_{3t}}V_{n2,1} - \frac{C_{23}}{C_{3t}}\cdot\frac{C_{12}}{C_{2t}-C_{23}^2/C_{3t}}V_{p3,1})$
	$+ R_1 B_{p1}(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p}$
	$V_2 = V_{dd} - \frac{1}{C_{2t}-C_{12}^2/C_{1t}-C_{23}^2/C_{3t}}(V_{n2,1} + \frac{C_{12}}{C_{1t}}V_{n1,1} - \frac{C_{23}}{C_{3t}}V_{p3,1}) - R_2 B_{n2}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}$
	$V_3 = \frac{C_{2t}-C_{12}^2/C_{1t}}{C_{3t}(C_{2t}-C_{12}^2/C_{1t})}(V_{p3,1} - \frac{C_{23}}{C_{2t}-C_{12}^2/C_{1t}}V_{n2,1} - \frac{C_{12}}{C_{1t}}\cdot\frac{C_{23}}{C_{2t}-C_{12}^2/C_{1t}}V_{n1,1}) + R_3 B_{p3}(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p}$
	$V_{n1,1} = \frac{\tau_r}{(n_n+1)V_{dd}}B_{n1}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1}$
	$V_{n2,1} = \frac{\tau_r}{(n_n+1)V_{dd}}B_{n2}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1}$
	$V_{p3,1} = \frac{\tau_r}{(n_p+1)V_{dd}}B_{p3}(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p+1}$
$[\tau_r,\tau_{sat}^{min}]$	$V_1 = V_1(\tau_r) - \frac{C_{2t}-C_{23}^2/C_{3t}}{C_{1t}(C_{2t}-C_{23}^2/C_{3t})}(V_{n1,2} + \frac{C_{12}}{C_{2t}-C_{23}^2/C_{3t}}V_{n2,2} - \frac{C_{23}}{C_{3t}}\cdot\frac{C_{12}}{C_{2t}-C_{23}^2/C_{3t}}V_{p3,2})(t-\tau_r)$
	$V_2 = V_2(\tau_r) - \frac{1}{C_{2t}-C_{12}^2/C_{1t}-C_{23}^2/C_{3t}}(V_{n2,2} + \frac{C_{12}}{C_{1t}}V_{n1,2} - \frac{C_{23}}{C_{3t}}V_{p3,2}(t-\tau_r)$
	$V_3 = V_3(\tau_r) + \frac{C_{2t}-C_{12}^2/C_{1t}}{C_{3t}(C_{2t}-C_{12}^2/C_{1t})}(V_{p3,2} - \frac{C_{23}}{C_{2t}-C_{12}^2/C_{1t}}V_{n2,2} - \frac{C_{12}}{C_{1t}}\cdot\frac{C_{23}}{C_{2t}-C_{12}^2/C_{1t}}V_{n1,2})(t-\tau_r)$
	$V_{n1,2} = B_{n1}(V_{dd} - V_{TN})^{n_n}$
	$V_{n2,2} = B_{n2}(V_{dd} - V_{TN})^{n_n}$
	$V_{p3,2} = B_{p3}(V_{dd} - V_{TP})^{n_p}$
	$\tau_{sat}^{min} = \min(\tau_{nsat}^1,\tau_{nsat}^2,\tau_{psat}^3)$

an out-of-phase transition is approximated as

$$C_{1_{eff}} = \frac{C_1C_2 + C_c(C_1 + C_2)}{C_2 + (1 - B_{p2}/B_{n1})C_c}, \tag{96}$$

$$C_{2_{eff}} = \frac{C_1C_2 + C_c(C_1 + C_2)}{C_1 + (1 + B_{n1}/B_{p2})C_c}, \tag{97}$$

respectively. In this analysis, $B_{n1} = B_{p2}$ is assumed. The solid lines shown in Fig. 6 describe the ratio of $C_{n1_{eff}}$ to $C_1 + 2C_c$, and the dotted lines depict the ratio of $C_{n2_{eff}}$ to $C_2 + 2C_c$. The horizontal axis represents the ratio of C_2 to C_1, and ratios of C_c to C_1 of 0.3, 0.5, and 0.7 are considered for each condition. If C_1 is identical to C_2, $C_{1_{eff}}$ and $C_{2_{eff}}$ are equal to $C_1 + 2C_c$ and $C_2 + 2C_c$, respectively. Note that the effective load capacitance of Inv_1 (Inv_2) may not be equal to $C_1 + 2C_c$ ($C_2 + 2C_c$) due to the difference between the load capacitances.

For a three-line coupled system, the effective capacitive load of each CMOS inverter when the output of Inv_2 transitions from high-to-low while the outputs of Inv_1 and Inv_3 transition from

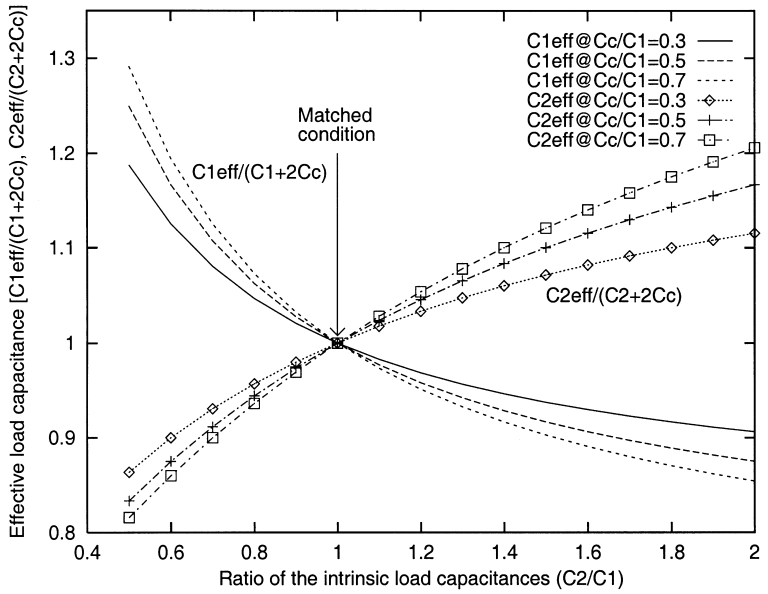

Fig. 6. The ratio of the effective load capacitances $C_{n1_{eff}}$ and $C_{n2_{eff}}$ to $C_1 + 2C_c$ and $C_2 + 2C_c$, respectively, for an out-of-phase transition assuming $B_{n1} = B_{p2}$.

low-to-high, is

$$C_{1_{eff}} = \frac{C_{1t} - C_{12}^2/(C_{2t} - C_{23}^2/C_{3t})}{1 - [C_{12}/(C_{2t} - C_{23}^2/C_{3t})]B_{n2}/B_{p1} + (C_{23}/C_{3t})[C_{12}/(C_{2t} - C_{23}^2/C_{3t})]B_{p3}/B_{p1}}, \quad (98)$$

$$C_{2_{eff}} = \frac{C_{1t} - (C_{12}/C_{1t})C_{12} - (C_{23}/C_{3t})C_{23}}{1 - (C_{12}/C_{1t})B_{p1}/B_{n2} - (C_{23}/C_{3t})B_{p3}/B_{n2}}, \quad (99)$$

$$C_{3_{eff}} = \frac{C_{3t} - C_{23}^2/(C_{2t} - C_{12}^2/C_{1t})}{(C_{12}/C_{1t})[C_{23}/(C_{2t} - C_{12}^2/C_{1t})]B_{p1}/B_{p3} - (C_{23}/C_{2t} - C_{12}^2/C_{1t})B_{n2}/B_{p3} + 1}, \quad (100)$$

respectively. When the outputs of Inv_1 and Inv_2 transition from high-to-low while the output of Inv_3 transitions from low-to-high, the effective capacitive load of each CMOS inverter is

$$C_{1_{eff}} = \frac{C_{1t} - C_{12}^2/(C_{2t} - C_{23}^2/C_{3t})}{1 + [C_{12}/(C_{2t} - C_{23}^2/C_{3t})]B_{n2}/B_{n1} - C_{23}/C_{3t}[C_{12}/(C_{2t} - C_{23}^2/C_{3t})]B_{p3}/B_{n1}}, \quad (101)$$

$$C_{2_{eff}} = \frac{C_{1t} - (C_{12}/C_{1t})C_{12} - (C_{23}/C_{3t})C_{23}}{(C_{12}/C_{1t})B_{n1}/B_{n2} + 1 - (C_{23}/C_{3t})B_{p3}/B_{n2}}, \quad (102)$$

$$C_{3_{eff}} = \frac{C_{3t} - C_{23}^2/(C_{2t} - C_{12}^2/C_{1t})}{1 - (C_{12}/C_{1t})[C_{23}/(C_{2t} - C_{12}^2/C_{1t})]B_{n1}/B_{n3} - [C_{23}/(C_{2t} - C_{12}^2/C_{1t})]B_{n2}/B_{p3}}, \quad (103)$$

Table 12
Propagation delay of a CMOS inverter in a two- and three-line coupled system

Out-of-phase transition for a two-line coupled system

$$t_{P_{HL1}} = \frac{(V_1(\tau_r) - 0.5V_{dd})(C_1C_2 + C_c(C_1 + C_2))}{(C_2 + C_c)B_{n1}(V_{dd} - V_{TN})^{n_n} - C_cB_{p2}(V_{dd} - V_{TP})^{n_p}} + \tau_r$$

$$t_{P_{LH2}} = \frac{(0.5V_{dd} - V_2(\tau_r))(C_1C_2 + C_c(C_1 + C_2))}{(C_2 + C_c)B_{p2}(V_{dd} - V_{TP})^{n_p} - C_cB_{n1}(V_{dd} - V_{TN})^{n_n}} + \tau_r$$

$$V_1(\tau_r) = V_{dd} - \frac{[(C_2 + C_c)\tau_r/(n_n + 1)V_{dd}]B_{n1}(V_{dd} - V_{TN})^{n_n+1} - [C_c\tau_r/(n_p + 1)V_{dd}]B_{p2}(V_{dd} - V_{TP})^{n_p+1}}{C_1C_2 + C_c(C_1 + C_2)} - R_1B_{n1}(V_{dd} - V_{TN})^{n_n}$$

$$V_2(\tau_r) = \frac{[(C_1 + C_c)\tau_r/(n_p + 1)V_{dd}]B_{p2}(V_{dd} - V_{TP})^{n_p+1} - [C_c\tau_r/(n_n + 1)V_{dd}]B_{n1}(V_{dd} - V_{TN})^{n_n+1}}{C_1C_2 + C_c(C_1 + C_2)} - R_2B_{p2}(V_{dd} - V_{TP})^{n_p}$$

Out-of-phase transition for a three-line coupled system
Inv_2 transitions from high-to-low while Inv_1 and Inv_3 transition from low-to-high

$$t_{P_{LH1}} = \frac{[0.5V_{dd} - V_1(\tau_r)][C_{1t}(C_{2t} - C_{23}^2/C_{3t}) - C_{12}^2]}{B_{p1}(V_{dd} - V_{TP})^{n_p} - [C_{12}/(C_{2t} - C_{23}^2/C_{3t})]B_{n2}(V_{dd} - V_{TN})^{n_n} + C_{23}/C_{3t}[C_{12}/(C_{2t} - C_{23}^2/C_{3t})]B_{p3}(V_{dd} - V_{TP})^{n_p}} + \tau_r$$

$$t_{P_{HL2}} = \frac{[V_2(\tau_r) - 0.5V_{dd}][C_{2t} - C_{12}^2/C_{1t} - C_{23}^2/C_{3t}]}{B_{n2}(V_{dd} - V_{TN})^{n_n} - (C_{12}/C_{1t})B_{p1}(V_{dd} - V_{TP})^{n_p} - (C_{23}/C_{3t})B_{p3}(V_{dd} - V_{TP})^{n_p}} + \tau_r$$

$$t_{P_{LH3}} = \frac{[0.5V_{dd} - V_3(\tau_r)][C_{3t}(C_{2t} - C_{13}^2/C_{1t}) - C_{23}^2]}{B_{p3}(V_{dd} - V_{TP})^{n_p} - [C_{23}/(C_{2t} - C_{12}^2/C_{1t})]B_{n2}(V_{dd} - V_{TN})^{n_n} + C_{12}/C_{1t}[C_{23}/(C_{2t} - C_{12}^2/C_{1t})]B_{p1}(V_{dd} - V_{TP})^{n_p}} + \tau_r$$

$$V_1(\tau_r) = \frac{C_{2t} - C_{23}^2/C_{3t}}{C_{1t}(C_{2t} - C_{23}^2/C_{3t}) - C_{12}^2}\left(\frac{\tau_rB_{p1}(V_{dd} - V_{TP})^{n_p+1}}{(n_p + 1)V_{dd}} - \frac{C_{12}}{C_{2t} - C_{23}^2/C_{3t}}\frac{\tau_rB_{n2}(V_{dd} - V_{TN})^{n_n+1}}{(n_n + 1)V_{dd}}\right.$$
$$\left. + \frac{C_{23}}{C_{3t}} \cdot \frac{C_{12}}{C_{2t} - C_{23}^2/C_{3t}}\frac{\tau_rB_{p3}(V_{dd} - V_{TP})^{n_p+1}}{(n_p + 1)V_{dd}}\right) + R_1B_{p1}(V_{dd} - V_{TP})^{n_p}$$

$$V_2(\tau_r) = V_{dd} - \frac{1}{C_{2t} - C_{12}^2/C_{1t} - C_{23}^2/C_{3t}}\left(\frac{\tau_rB_{n2}(V_{dd} - V_{TN})^{n_n+1}}{(n_n + 1)V_{dd}} - \frac{C_{12}\tau_rB_{p1}(V_{dd} - V_{TP})^{n_p+1}}{C_{1t}\quad(n_p + 1)V_{dd}}\right.$$
$$\left. - \frac{C_{23}\tau_rB_{p3}(V_{dd} - V_{TP})^{n_p+1}}{C_{3t}\quad(n_p + 1)V_{dd}}\right) - R_2B_{n2}(V_{dd} - V_{TN})^{n_n}$$

$$V_3(\tau_r) = \frac{C_{2t} - C_{12}^2/C_{1t}}{C_{3t}(C_{2t} - C_{12}^2/C_{1t}) - C_{23}^2}\left(\frac{\tau_rB_{p3}(V_{dd} - V_{TP})^{n_p+1}}{(n_p + 1)V_{dd}} - \frac{C_{23}}{C_{2t} - C_{12}^2/C_{1t}}\frac{\tau_rB_{n2}(V_{dd} - V_{TN})^{n_n+1}}{(n_n + 1)V_{dd}}\right.$$
$$\left. + \frac{C_{12}}{C_t} \cdot \frac{C_{23}}{C_{2t} - C_{12}^2/C_{1t}}\frac{\tau_rB_{p3}(V_{dd} - V_{TP})^{n_p+1}}{(n_p + 1)V_{dd}}\right) + R_3B_{p3}(V_{dd} - V_{TP})^{n_p}$$

respectively. The same conclusion for an out-of-phase transition can also be drawn as for an in-phase transition where the effective capacitive load of each CMOS inverter within a capacitively coupled system depends upon the intrinsic load capacitance, the coupling capacitance, and the transconductance of each active transistor.

4.3. Propagation delay time

Similar to the procedure of an in-phase transition, analytical expressions characterizing the propagation delay of each CMOS inverter during an out-of-phase transition within a two-line and a three-line coupled system are listed in Table 12.

Based on the same assumption, when the outputs of Inv_1 and Inv_2 transition from high-to-low while the output of Inv_3 transitions from low-to-high, the propagation delay of each CMOS inverter can be determined from (88), (89), and (90), respectively.

A comparison of the analytic propagation delay of a CMOS inverter with SPICE for an out-of-phase transition is listed in Tables 13 and 14 for a two-line and a three-line coupled system,

Table 13
Comparison of an out-of-phase transition with SPICE for a two-line coupled system assuming $w_p = 2w_n$

	Circuit parameters							SPICE		No coupling				Analytic estimation			
τ_r (ns)	w_{n1} (μm)	R_1 (Ω)	C_1 (pF)	w_{n2} (μm)	R_2 (Ω)	C_2 (pF)	C_c (pF)	τ_1 (ns)	τ_2 (ns)	τ_1 (ns)	τ_2 (ns)	δ_1 (%)	δ_2 (%)	τ_1 (ns)	τ_2 (ns)	δ_1 (%)	δ_2 (%)
0.2	3.6	100	0.1	3.6	100	0.2	0.1	200	321	218	267	9.0	16.82	186	314	7.0	2.18
0.2	3.6	100	0.2	3.6	100	0.1	0.1	321	200	267	218	16.82	9.0	314	186	2.18	7.0
0.2	3.6	100	0.2	5.4	100	0.3	0.1	311	225	276	202	11.25	10.22	307	212	1.28	5.78
0.2	5.4	100	0.3	3.6	100	0.2	0.1	225	311	202	276	10.22	11.25	212	307	5.78	1.28
0.2	3.6	100	0.2	5.4	100	0.2	0.1	341	184	276	201	19.06	9.23	367	177	7.50	3.8
0.2	5.4	100	0.2	3.6	100	0.2	0.1	184	341	201	276	9.23	19.06	177	367	3.8	7.50
0.4	5.4	100	0.2	5.4	100	0.4	0.2	270	437	235	355	12.9	18.76	281	423	4.07	3.2
0.4	5.4	100	0.4	3.6	100	0.2	0.2	437	270	355	235	18.76	12.9	423	281	3.2	4.07
0.4	5.4	100	0.2	5.4	100	0.4	0.3	329	515	368	425	11.85	17.47	304	505	7.6	1.95
0.4	5.4	100	0.4	5.4	100	0.2	0.3	515	329	425	368	17.47	11.85	505	304	1.95	7.6
Statistical analysis						No coupling				Analytic estimation				Improvement			
Maximum error (%)						18.76				7.6				11.16			
Average error (%)						13.66				4.44				9.22			

Table 14
Comparison of an out-of-phase transition with SPICE for a three-line coupled system assuming $w_p = 2w_n$

	Circuit parameters											SPICE	No coupling		Analytic	
τ_r (ns)	w_{p1} (μm)	R_1 (Ω)	C_1 (pF)	w_{n2} (μm)	R_2 (Ω)	C_2 (pF)	w_{p3} (μm)	R_3 (Ω)	C_3 (pF)	C_{12} (pF)	C_{23} (pF)	τ_2 (ns)	τ_2 (ns)	δ_2 (%)	τ_2 (ns)	δ_2 (%)
0.2	3.6	80	0.1	3.6	100	0.2	3.6	90	0.1	0.1	0.1	437	422	3.43	443	1.37
0.2	3.6	100	0.1	5.4	100	0.2	3.6	100	0.1	0.1	0.1	225	269	19.56	208	7.56
0.2	3.6	100	0.1	3.6	0.05	100	3.6	100	0.1	0.05	0.05	153	191	24.84	139	9.15
0.2	3.6	100	0.1	3.6	100	0.05	3.6	100	0.1	0.1	0.1	246	323	31.30	226	8.13
0.2	3.6	100	0.1	5.4	100	0.1	3.6	100	0.1	0.1	0.1	165	229	38.79	146	11.51
0.2	7.2	150	0.2	5.4	100	0.1	3.6	100	0.1	0.1	0.1	185	229	23.78	167	9.73
0.2	7.2	150	0.2	5.4	100	0.1	7.2	100	0.2	0.1	0.1	212	229	8.01	196	7.55
0.2	7.2	150	0.2	5.4	100	0.1	7.2	100	0.2	0.15	0.15	307	325	5.87	295	3.91
0.2	7.2	150	0.2	7.2	100	0.1	7.2	100	0.2	0.15	0.15	176	221	25.57	161	8.52
Statistical analysis					No coupling				Analytic estimation				Improvement			
Maximum error (%)					38.79				11.51				27.28			
Average error (%)					20.13				7.49				12.64			

respectively. The delay is estimated based on the intrinsic load capacitances plus two times the coupling capacitance for the *no coupling* condition [3,32,34]. The maximum error under the *no coupling* condition can exceed 18% of SPICE for a two-line coupled system and 35% of SPICE for a three-line coupled system, while the maximum error of the analytic propagation delay model

listed in Table 12 is within 11% of SPICE. The maximum and average improvement of the proposed propagation delay model are about 11% and 9%, and 27% and 12% of SPICE for a two-line and a three-line coupled system, respectively, as listed in Tables 13 and 14.

5. At least one inverter is quiet

For a two-line coupled system, the condition under which one inverter is active and the other is quiet has the highest probability of occuring, $\frac{4}{9}$ (see Table 2). The probability of at least one inverter being quiet is $\frac{18}{27}$ (excluding all three inverters being quiet at the same time) for a three-line coupled system (see Table 3). The propagation delay of an active inverter and the coupling noise voltage at the output of a quiet inverter are discussed in Section 5.1 for a two-line coupled system. A similar analysis of a three-line coupled system is presented in Section 5.2. Analytical estimations are also compared to SPICE in Section 5.3.

5.1. Two-line coupled structure

For either an in-phase or an out-of-phase transition, the coupling capacitance affects the waveform of the output voltage and the propagation delay of each inverter, changing (primarily decreasing) the speed of a CMOS integrated circuit [3–5]. Interconnect coupling capacitances typically degrade the performance of a CMOS integrated circuit. If one inverter is active and the other is quiet, the active transition can induce a voltage change at the output of a quiet inverter through the coupling capacitance. The coupled noise voltage may seriously affect the circuit behavior and related power dissipation characteristics [18–22].

In the following analysis, the output of Inv_1 is assumed to transition from high-to-low while the input of Inv_2 is fixed at V_{dd}. Therefore, the initial voltage of V_1 and V_2 are V_{dd} and ground, respectively. The input voltage of Inv_1 is assumed to be shaped as a rising ramp signal [defined in Ref. (6)]. When the input voltage exceeds V_{TN}, $NMOS_1$ is ON and starts operating in the saturation region. $NMOS_2$ operates in the linear region due to the small voltage change at the output. The differential equations, (1) and (2), become (114) and (115), respectively. There are no tractable solutions to these coupled differential equations, (114) and (115). In order to derive a tractable solution, it is necessary to make certain simplifying assumptions.

5.1.1. Step input approximation

If the transition time of the input signal is small as compared to the propagation delay of a CMOS inverter and the output transition time, the input can be approximated as a step input. Analytical expressions characterizing the output voltage of Inv_1 and the coupling noise voltage at the output of Inv_2 before $NMOS_1$ starts to operate in the linear region are listed in Table 15. The time τ^1_{nsat} when $NMOS_1$ leaves the saturation region can be determined by applying a Newton–Raphson algorithm to (116).

The propagation delay of Inv_1 can be approximated from (116) by also applying a Newton–Raphson iteration technique. Since the current through $NMOS_2$ discharges the capacitor C_1, the propagation delay is less than the estimated delay based on a load of $C_1 + C_c$.

Table 15
One line is active and the other line is quiet in a two-line coupled system

Differential equations ($\tau_n \leqslant t \leqslant \tau_r$)

$$(C_1 + C_c)\frac{dV_1}{dt} - (1 + R_2\gamma_{n2})C_c\frac{dV_2}{dt} = -B_{n1}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n} - R_1 B_{n1}\frac{d((t/\tau_r)V_{dd} - V_{TN})^{n_n}}{dt}$$

$$(1 + R_2\gamma_{n2})(C_2 + C_c)\frac{dV_2}{dt} - C_c\frac{dV_1}{dt} = -\gamma_{n2}V_2$$

Step input approximation ($t \leqslant \tau^1_{nsat}$)

$$V_1 = V_{dd} - \frac{B_{n1}}{C_1 + C_c}(V_{dd} - V_{TN})^{n_n}t + \frac{C_c}{C_1 + C_c}V_2$$

$$V_2 = -\frac{C_c}{(C_1 + C_c)\gamma_{n2}}B_{n1}(V_{dd} - V_{TN})^{n_n}(1 - e^{-\alpha_{n2}t})$$

$$\alpha_{n2} = \frac{(C_1 + C_c)\gamma_{n2}}{(1 + R_2\gamma_{n2})(C_1C_2 + C_c(C_1 + C_2))}$$

Current through $NMOS_2$ is negligible

$\tau_n \leqslant t \leqslant \tau_r$

$$V_1 = V_{dd} - R_1 B_{n1}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n} - \frac{C_2 + C_c}{C_1C_2 + C_c(C_1 + C_2)} \cdot \frac{B_{n1}\tau_r}{(n_n + 1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n + 1}$$

$$V_2 = \frac{C_c}{C_1C_2 + C_c(C_1 + C_2)} \cdot \frac{B_{n1}\tau_r}{(1 + R_2\gamma_{n2})(n_n + 1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n + 1}$$

$\tau_r \leqslant t \leqslant \tau^1_{nsat}$

$$V_1 = V_1(\tau_r) - \frac{B_{n1}}{C_1 + C_c}(V_{dd} - V_{TN})^{n_n}(t - \tau_r) - \frac{C_c(1 + R_2\gamma_{n2})}{C_1 + C_c}(V_2(\tau_r) + V_{2,a})(1 - e^{-\alpha_{n2}(t - \tau_r)})$$

$$V_2 = -V_{2,a} + (V_2(\tau_r) + V_{2,a})e^{-\alpha_{n2}(t - \tau_r)}$$

$$V_{2,a} = \frac{C_cB_{n1}}{(C_1 + C_c)\gamma_{n2}}(V_{dd} - V_{TN})^{n_n}$$

$$\alpha_{n2} = \frac{(C_1 + C_c)\gamma_{n2}}{(1 + R_2\gamma_{n2})(C_1C_2 + C_c(C_1 + C_2))}$$

Polynomial approximation of the drain-to-source current of $NMOS_1$

$\tau_n \leqslant t \leqslant \tau_r$

$$V_1 = V_{dd} - \frac{1}{C_1 + C_c}V_{1,a} - R_1 B_{n1}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n} + \frac{C_c(1 + R_2\gamma_{n2})}{C_1 + C_c}V_2,$$

$$V_2 = B_1\xi + B_2\xi^2 + (1 - B_0)e^{-\alpha_{n2}(t - \tau_n)}$$

$$V_{1,a} = B_{n1}\frac{\tau_r}{(n_n + 1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n + 1}$$

$$B_0 = -\frac{C_c}{(C_1 + C_c)\gamma_{n2}}A_0 + \frac{C_cC_t(1 + R_2\gamma_{n2})}{(C_1 + C_c)^2\gamma^2_{n2}\tau_r}A_1 - 2\frac{C_cC_t^2(1 + R_2\gamma_{n2})^2}{(C_1 + C_c)^3\gamma^3_{n2}\tau_r^2}A_2$$

$$B_1 = 2\frac{C_cC_t(1 + R_2\gamma_{n2})}{(C_1 + C_c)^2\gamma^2_{n2}\tau_r}A_2 - \frac{C_c}{(C_1 + C_c)\gamma_{n2}}A_1$$

$$B_2 = -\frac{C_c}{(C_1 + C_c)\gamma_{n2}}A_2$$

$$C_t = C_1C_2 + C_c(C_1 + C_2)$$

After τ^1_{nsat}, both of the NMOS transistors operate in the linear region. The solutions for the peak voltage can be obtained from the initial values of V_1 and V_2, as described in Appendix A. Note that V_2 decreases exponentially in the linear region. The peak noise occurs at τ^1_{nsat},

$$V_2(\text{peak}) = -\frac{C_c}{(C_1 + C_c)\gamma_{n2}}B_{n1}(V_{dd} - V_{TN})^{n_n}(1 - e^{-\alpha_{n2}\tau^1_{nsat}}). \tag{132}$$

5.1.2. Current through NMOS_2 *is negligible*

The analysis described in this section is based on the assumption that the current through NMOS_2 can be neglected, i.e., $\gamma_{n2}V_2$ is small as compared to $C_c\mathrm{d}V_1/\mathrm{d}t$ in (115). Based on this assumption, the solutions of V_1 and V_2 are (119) and (120), respectively. The effective load capacitance of Inv_1 is

$$C_{1_{\mathrm{eff}}} = \left(C_1 + \frac{C_2}{C_2 + C_c}C_c\right) \leqslant (C_1 + C_c). \tag{133}$$

When the input signal reaches V_{dd} at τ_r, NMOS_1 continues to operate in the saturation region. However, the coupling noise voltage V_2 at τ_r is

$$V_2(\tau_r) = \frac{C_c}{C_1C_2 + C_c(C_1 + C_2)} \frac{B_{n1}\tau_r}{(1 + R_2\gamma_{n2})(n_n + 1)V_{dd}}(V_{dd} - V_{TN})^{n_n+1}. \tag{134}$$

Note that γ_2V_2 cannot be neglected after the input transition is completed since γ_2V_2 may be comparable to $C_c\mathrm{d}V_1/\mathrm{d}t$. Therefore, the γ_2V_2 term in (115) is considered in the derivation once the input transition is completed. After τ_r, the output voltages of V_1 and V_2 are described by (121) and (122), respectively. τ^1_{nsat} (the time when NMOS_1 leaves the saturation region) and $t_{0.5}$ (the time when V_1 reaches $0.5V_{dd}$) are determined from (121) by applying a Newton–Raphson iteration. The peak coupling noise voltage can be approximated at τ^1_{nsat} and is equal to $V_2(\tau^1_{nsat})$ which is determined from (122).

5.1.3. Approximation of the drain-to-source current

A simplification in which the current through NMOS_2 is assumed to be negligible is appropriate when $\gamma_{n2}V_2$ is small as compared to $C_c\mathrm{d}V_1/\mathrm{d}t$ in (115). If $\gamma_{n2}V_2$ is comparable to $C_c\mathrm{d}V_1/\mathrm{d}t$, the current through NMOS_2 cannot be neglected.

In order to derive tractable solutions, the drain-to-source current of NMOS_1 can be approximated using a second order polynomial expansion,

$$B_{n1}\left(\frac{t}{\tau_r}V_{dd} - V_{TN}\right)^{n_n} \approx A_0 + A_1\xi + A_2\xi^2, \tag{135}$$

where $\xi = t/\tau_r - V_{TN}/V_{dd}$ and A_0, A_1, and A_2 are determined from a polynomial expansion of the drain-to-source current of NMOS_1. Solutions of the differential equations represented by (114) and (115) are (125) and (126).

After the input transition is completed, NMOS_1 continues to operate in the saturation region. The analysis after τ_r is the same as the condition under which the current through NMOS_2 is negligible, which is described in Section 5.1.2. V_2 exhibits an exponential decay when both transistors operate in the linear region. Therefore, the peak coupling noise voltage can be approximated at τ^1_{nsat}.

5.1.4. Delay uncertainty of an active logic gate

In the previous analysis, the output of Inv_1 is assumed to transition from high-to-low and the input of Inv_2 is fixed at V_{dd}. Note that the current through NMOS_2 discharges C_1, and the

estimated delay is smaller than the estimated delay based on $C_1 + C_c$. If the input of Inv_2 is at ground and $PMOS_2$ is ON, the coupling capacitance affects the propagation delay of Inv_1 differently.

The effect of the initial state can be demonstrated with a step input signal. If the initial value of both V_1 and V_2 is V_{dd}, and since $NMOS_1$ operates in the saturation region, the output voltages are

$$V_1 = V_{dd} - \frac{B_{n1}}{C_1 + C_c}(V_{dd} - V_{TN})^{n_n} t + \frac{C_c}{C_1 + C_c} V_{p2}, \tag{136}$$

$$V_2 = V_{dd} - \frac{C_c B_{n1}(V_{dd} - V_{TN})^{n_n}}{(C_1 + C_c)\gamma_{p2}}(1 - e^{-\alpha_{p2} t}), \tag{137}$$

where

$$V_{p2} = \frac{C_c}{C_1 + C_c} B_{n1}(V_{dd} - V_{TN})^{n_n}(1 - e^{-\alpha_{p2} t}), \tag{138}$$

$$\alpha_{p2} = \frac{\gamma_{p2}}{1 + R_2 \gamma_{p2}} \frac{C_1 + C_c}{C_1 C_2 + C_c(C_1 + C_2)}. \tag{139}$$

The propagation delay of Inv_1 can be approximated by (136). Since the current through $PMOS_2$ slows down the discharge process, the propagation delay is greater than the delay calculated assuming $C_1 + C_c$ is the load capacitance. The peak coupling noise voltage also occurs at the time when $NMOS_1$ leaves the saturation region.

Undershoots are exhibited when the active inverter transitions from high-to-low and the quiet state is at a logic low (ground). Overshoots may occur when the active inverter transitions from low-to-high and the quiet state is at a logic high (V_{dd}). Overshoots or undershoots may cause carrier injection or collection in the substrate, possibly corrupting a data signal in dynamic logic circuits [27,28].

5.2. Three-line coupled structure

For a three-line coupled system, the probability of two inverters being quiet and the other being active (condition 1) is $\frac{6}{27}$ (see Table 4). If two inverters are quiet and the other inverter is active, the active inverter and the neighboring quiet inverter are equivalent to a system of two coupled interconnect lines. Therefore, the analysis made in Section 5.1 for a two-line coupled structure can be applied to this condition.

The probability of one inverter being quiet and the other two inverters being active (condition 2) is $\frac{12}{27}$ (see Table 4) for a three-line coupled system. However, there are two different cases under condition 2: Inv_2 is quiet while both Inv_1 and Inv_3 are active; and Inv_1 is quiet while both Inv_2 and Inv_3 are active (or Inv_3 is quiet while both Inv_1 and Inv_2 are active). Based on the previous analysis of a two-line coupled system, a three-line coupled system can be simplified to an equivalent two-line coupled system.

5.2.1. Inv_2 is quiet while both Inv_1 and Inv_3 are active

The coupling noise voltage at the output of Inv_2, which is induced by the active transition at the outputs of Inv_1 and Inv_3, is very small as compared to the voltage change at the outputs of Inv_1 and Inv_3. Therefore, the coupling noise voltage can be considered to have a negligible effect on the active transition at the outputs of both Inv_1 and Inv_3. The coupling noise voltage induced by the active transition at the output of Inv_1 is assumed to have no effect on the active transition at the output of Inv_3. The coupling noise voltage is proportional to

$$\frac{C_{12}}{C_1 + C_{12}} \cdot \frac{C_{23}}{C_2 + C_{23}}$$

assuming a step input signal. Similarly, the coupling noise voltage induced by the active transition at the output of Inv_3 is assumed to have no effect on the active transition at the output of Inv_1. The coupling noise voltage is proportional to

$$\frac{C_{23}}{C_3 + C_{23}} \cdot \frac{C_{12}}{C_2 + C_{12}}$$

assuming a step input signal. As shown in Fig. 4, with this assumption, Inv_1 and Inv_2 (and Inv_2 and Inv_3) can be treated as a two-line coupled system. Therefore, a three-line coupled system can be decomposed into two two-line coupled systems. The coupling noise voltage at the output of Inv_2 is a linear superposition of these two individual noise voltages caused by the dynamic transition at the outputs of both Inv_1 and Inv_3. The propagation delay of Inv_1 and Inv_3 can be determined from the analysis of a two-line coupled system as discussed in Section 5.1.

Note that if Inv_1 and Inv_3 have the same dynamic transitions, the coupling noise voltage at the output of Inv_2 is the summation of these two individual noise voltages caused by Inv_1 and Inv_3. This summation is the worst case conditions in terms of producing a high peak noise voltage at the output of Inv_2 (assuming Inv_1 and Inv_3 are triggered close in time with approximately the same input slew rate). If Inv_1 and Inv_3 transition in the opposite directions, the coupling noise voltage at the output of Inv_2 is the difference between the two individual noise voltages induced by Inv_1 and Inv_3. This condition is the best case in terms of minimizing the peak noise voltage at the output of Inv_2 (assuming Inv_1 and Inv_3 are triggered close in time with approximately the same input slew rate).

5.2.2. Inv_1 is quiet while both Inv_2 and Inv_3 are active

For a three-line coupled system as shown in Fig. 4, when Inv_1 is quiet while both Inv_2 and Inv_3 are active, this system can be simplified to an equivalent two-line coupled system as shown in Fig. 7. In this figure, the intrinsic load capacitance at the output of Inv_2 is $C_{2_{\text{eff}}}$ rather than C_2. The effective capacitive load $C_{2_{\text{eff}}}$ is determined based on the signal activity at the outputs of Inv_2 and Inv_3 [(42) or (43) for an in-phase transition and (96) or (97) for an out-of-phase transition], which has been discussed in Sections 3.2 and 4.2, respectively. Therefore, the analysis of a two-line coupled system as described in Section 5.1 can be applied to this simplified three-line coupled system (as illustrated in Fig. 7).

5.3. Comparison with SPICE

For a two-line coupled system, the propagation delay of the active CMOS inverter and the peak coupling noise voltage at the output of the quiet inverter are compared to SPICE in Table 16. The

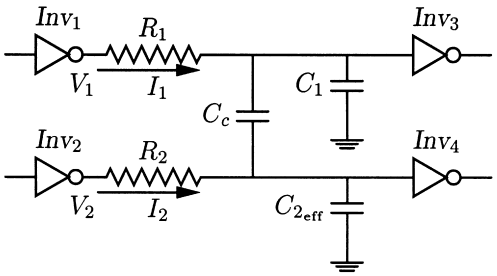

Fig. 7. Simplified circuit diagram of a three-line coupled system when Inv_1 is quiet while Inv_2 and Inv_3 are dynamically transitioning.

Table 16
Comparison of Inv_1 active and Inv_2 quiet with SPICE

	Circuit parameters								Delay of Inv_1					Peak voltage of Inv_2		
									SPICE	No coupling		Analytic		SPICE	Analytic	
τ_r (ns)	W_{n1} (μm)	R_1 (Ω)	C_1 (pF)	W_{n1} (μm)	R_1 (Ω)	C_1 (pF)	C_c (pF)	Initial State of Inv_2	τ_1 (ps)	τ_1 (ps)	δ_1 (%)	τ_1 (ps)	δ_1 (%)	V_2 (V)	V_2 (V)	δ_2 (%)
0.2	1.8	100	0.1	1.8	100	0.1	0.05	0	232	244	5.18	236	1.7	− 0.364	− 0.352	3.30
0.2	1.8	100	0.1	1.8	100	0.1	0.05	1	230	244	6.09	227	1.30	4.54	4.61	7.00
0.2	1.8	100	0.1	1.8	100	0.1	0.1	0	277	315	13.72	284	2.52	− 0.565	− 0.586	3.72
0.2	1.8	100	0.1	1.8	100	0.1	0.1	1	270	315	16.67	264	2.22	4.26	4.42	3.76
0.2	1.8	100	0.1	3.6	100	0.1	0.1	0	289	315	9.00	293	1.38	− 0.313	− 0.327	4.47
0.2	1.8	100	0.1	3.6	100	0.1	0.1	1	284	315	10.92	274	3.52	4.59	4.62	0.65
0.2	3.6	100	0.2	3.6	100	0.2	0.1	0	219	230	5.02	224	2.28	− 0.35	− 0.344	1.71
0.2	3.6	100	0.2	3.6	100	0.2	0.1	1	216	230	6.48	221	2.31	4.56	4.66	2.19

	Delay of Inv_1			
	No coupling	Analytic estimation	Improvement	V_2
Maximum error (%)	16.67	3.52	13.15	7.00
Average error (%)	9.14	2.15	6.99	3.35

propagation delay of the active CMOS inverter is based on the intrinsic capacitance plus the coupling capacitance for the *no coupling* condition, i.e., $C_1 + C_c$ for Inv_1 or $C_2 + C_c$ for Inv_2 [3,32,34]. The maximum error of the propagation delay based on the *no coupling* condition can exceed 15% as compared to SPICE while the maximum error of the proposed delay model is less than 5% as compared to SPICE. The maximum and average improvement of the proposed propagation delay model are 13% and 7% of SPICE, respectively. The peak coupling noise voltage based on these analytical expressions is within 10% as compared to SPICE. Note that as the size of the quiet inverter is increased, the peak noise voltage is reduced, as illustrated by comparing the third and fifth rows listed in Table 16. However, this technique increases the propagation delay of the active CMOS inverter (Inv_1 for this case).

Table 17
Comparison of Inv_2 being quiet while both Inv_1 and Inv_3 being active with SPICE

	Circuit parameters											Action		Noise at Inv_2		
τ_r	w_{p1}	R_1	C_1	w_{n2}	R_2	C_2	w_{p3}	R_3	C_3	C_{12}	C_{23}	Inv_1	Inv_3	SPICE	Analytic	
(ns)	(μm)	(Ω)	(pF)	(μm)	(Ω)	(pF)	(μm)	(Ω)	(pF)	(pF)	(pF)			(V)	(V)	(%)
0.2	1.8	100	0.1	1.8	100	0.1	1.8	100	0.1	0.05	0.05	1/0	1/0	−0.63	−0.71	12.70
0.2	1.8	100	0.1	1.8	100	0.1	1.8	100	0.1	0.05	0.05	1/0	0/1	0.016	0.0	N/A
0.2	1.8	100	0.1	1.8	100	0.1	1.8	100	0.1	0.05	0.05	0/1	0/1	0.74	0.68	8.11
0.2	1.8	100	0.1	1.8	100	0.1	1.8	100	0.1	0.1	0.1	1/0	1/0	−1.05	−1.17	11.42
0.2	1.8	100	0.1	1.8	100	0.1	1.8	100	0.1	0.1	0.1	1/0	0/1	0.020	0.0	N/A
0.2	1.8	100	0.1	1.8	100	0.1	1.8	100	0.1	0.1	0.1	0/1	0/1	1.18	1.08	8.47
0.2	1.8	100	0.1	3.6	100	0.1	1.8	100	0.1	0.1	0.1	1/0	1/0	0.60	0.62	3.33
0.2	1.8	100	0.1	3.6	100	0.1	1.8	100	0.1	0.1	0.1	1/0	0/1	0.014	0.0	N/A
0.2	1.8	100	0.1	3.6	100	0.1	1.8	100	0.1	0.1	0.1	0/1	0/1	0.67	0.63	5.97
Statistical analysis									Noise voltage V_2							
Maximum error (%)									12.70							
Average error (%)									8.33							

For a three-line coupled system, when Inv_2 is quiet and the other two lines are active, the peak coupling noise voltage at the output of Inv_2 is compared to SPICE in Table 17. The analytical prediction for this condition is within 13% of SPICE using a linear superposition method based on summing the effects of two two-line coupled systems, as described in Section 5.2.1. Note that when Inv_1 and Inv_3 both transition in-phase, the coupling noise voltage at Inv_2 is greater than the peak coupling voltage when Inv_1 and Inv_3 transition out-of-phase. Moreover, if Inv_1 and Inv_3 are similarly sized, these two individual noise voltages may compensate (or negatively resonate) in an out-of-phase transition, making the coupling noise voltage at Inv_2 almost negligible (assuming the two signal transitions occur close in time).

6. Minimizing coupling effects

Delay uncertainty can be minimized or even eliminated when both inverters and load capacitances are approximately the same, i.e., $B_{n1} \approx B_{n2}$ and $C_1 \approx C_2$. For example, the coupling capacitance can be eliminated from the effective load capacitance under the condition of an in-phase transition. To reduce the propagation delay of a CMOS logic gate in a coupled system, the probability of an out-of-phase transition should be minimized because of the increased effective load capacitance. In order to minimize any delay uncertainty, all of these circuit elements should therefore be designed to be as similar to each other as possible.

However, if an out-of-phase transition cannot be avoided, the size of each transistor within a coupled system can be adjusted to optimize the propagation delay within a critical path by "transferring" some signal delay (through the effective capacitance) from one circuit branch to another circuit branch, an "advantage" of coupling capacitances. A proper strategy for adjusting

the coupled system depends upon the device parameters, the circuit structure, and the target performance specifications of the various data paths.

The coupling noise voltage is proportional to B_{n1}/γ_{n2} and C_c. If the effective output conductance of the quiet inverter is increased, the peak noise voltage can be reduced. This conclusion suggests that the size of the MOS transistors within the quiet inverter should be increased, contradicting the observation for the propagation delay. Therefore, a tradeoff exists when choosing the appropriate size of the transistors for capacitively coupled inverters. The optimal size of these transistors is also related to the signal activity and other circuit constraints.

7. Conclusions

An analysis of a CMOS inverter driving a coupled resistive–capacitive interconnect is presented in this paper. The uncertainty of the effective load capacitance and the propagation delay is noted for both an in-phase and an out-of-phase transition if the circuit elements are not equally sized or evenly balanced. The coupling noise voltage on the interconnect line at the output of a quiet inverter is also analyzed. A propagation delay model and an expression for estimating the peak coupling noise voltage are presented for analyzing coupling noise at the system level. Some design strategies are also suggested to reduce the noise and propagation delay caused by interconnect coupling capacitances.

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Appendix A. Both transistors operating in the linear region for a two-line coupled system

When both active transistors operate in the linear region, the drain-to-source current of each MOS transistor can be characterized by γV_{DS}, where γ is the effective output conductance of a MOS transistor. For an in-phase transition where the outputs of both inverters transition from high-to-low, the differential equations charactering a system of two coupled CMOS inverters are

$$-\gamma_1 V_1 = (C_1 + C_c)(1 + R_1\gamma_1)\frac{dV_1}{dt} - C_c(1 + R_2\gamma_2)\frac{dV_2}{dt}, \tag{A.1}$$

$$-\gamma_2 V_2 = (C_2 + C_c)(1 + R_2\gamma_2)\frac{dV_2}{dt} - C_c(1 + R1\gamma_1)\frac{dV_1}{dt}. \tag{A.2}$$

The general solutions of these coupled differential equations, (A.1) and (A.1), are

$$V_1 = \frac{1}{2}K_3\left(e^{-\alpha_1 t} + e^{-\alpha_2 t} + \frac{\alpha_c}{\alpha_a}(e^{-\alpha_1 t} - e^{-\alpha_2 t})\right) + K_4\frac{C_c\gamma_2(1 + R_2\gamma_2)}{\alpha_a}(e^{\alpha_1 t} - e^{\alpha_2 t}), \tag{A.3}$$

and

$$V_2 = \frac{1}{2}K_4\left(e^{-\alpha_1 t} + e^{-\alpha_2 t} - \frac{\alpha_c}{\alpha_a}(e^{-\alpha_1 t} - e^{\alpha_2 t})\right) + K_3\frac{C_c\gamma_1(1 + R_1\gamma_1)}{\alpha_a}(e^{-\alpha_1 t} - e^{-\alpha_2 t}), \tag{A.4}$$

where

$$\alpha_1 = \frac{1 + R_1\gamma_1}{1 + R_2\gamma_2}\frac{\alpha_b + \alpha_a}{C_1C_2 + C_c(C_1 + C_2)}, \tag{A.5}$$

$$\alpha_2 = \frac{1 + R_1\gamma_1}{1 + R_2\gamma_2}\frac{\alpha_b - \alpha_a}{C_1C_2 + C_c(C_1 + C_2)}, \tag{A.6}$$

$$\alpha_a = \sqrt{\alpha_c^2 + 4\gamma_1\gamma_2}C_c^2(1 + R_1\gamma_1)(1 + R_2\gamma_2), \tag{A.7}$$

$$\alpha_b = \gamma_1(1 + R_2\gamma_2)(C_2 + C_c) + \gamma_2(1 + R_1\gamma_1)(C_1 + C_c), \tag{A.8}$$

$$\alpha_c = \gamma_1(1 + R_2\gamma_2)(C_2 + C_c) - \gamma_2(1 + R_1\gamma_1)(C_1 + C_c). \tag{A.9}$$

K_3 and K_4 are integration constants which are determined from the initial conditions of V_1 and V_2 when both transistors enter the linear region, and are

$$K_3 = \frac{CV_1(\tau_1) - BV_2(\tau_1)}{AC - BD}, \tag{A.10}$$

$$K_4 = \frac{AV_2(\tau_1) - DV_1(\tau_1)}{AC - BD}, \tag{A.11}$$

where

$$A = \frac{1}{2}\left(e^{-\alpha_1\tau_1} + e^{-\alpha_2\tau_1} + \frac{\alpha_c}{\alpha_a}(e^{-\alpha_1\tau_1} - e^{-\alpha_2\tau_1})\right), \tag{A.12}$$

$$B = \frac{C_c\gamma_2(1 + R_2\gamma_2)}{\alpha_a}(e^{-\alpha_1\tau_1} - e^{-\alpha_2\tau_1}), \tag{A.13}$$

$$C = \frac{1}{2}\left(e^{-\alpha_1\tau_1} + e^{-\alpha_2\tau_1} - \frac{\alpha_c}{\alpha_a}(e^{-\alpha_1\tau_1} - e^{-\alpha_2\tau_1})\right), \tag{A.14}$$

$$D = \frac{C_c\gamma_1(1 + R_1\gamma_1)}{\alpha_a}(e^{-\alpha_1\tau_1} - e^{-\alpha_2\tau_1}). \tag{A.15}$$

τ_1 is the time when both transistors start operating in the linear region. $V_1(\tau_1)$ and $V_2(\tau_1)$ are the initial values of V_1 and V_2 at the time τ_1.

Appendix B. One or more transistors operating in the linear region for a three-line coupled system

For a three-line coupled system, it is assumed that Inv_1 leaves the saturation region first, followed by Inv_3 starting to operate in the linear region, and finally Inv_2 entering the linear region. Therefore, there are three disparate time regions, $\tau_{\text{sat}}^1 \leqslant t \leqslant \tau_{\text{sat}}^3$, $\tau_{\text{sat}}^3 \leqslant t \leqslant \tau_{\text{sat}}^2$, and $\tau_{\text{sat}}^2 \leqslant t$. For a set of equations such as

$$A_1 X + B_1 Y = D_1, \tag{B.1}$$

$$A_2 X + B_2 Y + C_2 Z = D_2, \tag{B.2}$$

$$B_3 Y + C_3 Z = D_3, \tag{B.3}$$

the solution is

$$X = \frac{D_1}{A_1} + \frac{B_1(C_3(A_2 D_1 - A_1 D_2) + A_1 C_2 D_3)}{A_1((A_1 B_2 - A_2 B_1)C_3 - A_1 B_3 C_2)}, \tag{B.4}$$

$$Y = -\frac{C_3(A_2 D_1 - A_1 D_2) + A_1 C_2 D_3}{(A_1 B_2 - A_2 B_1)C_3 - A_1 B_3 C_2}, \tag{B.5}$$

$$Z = \frac{D_3}{A_3} + \frac{B_3(C_3(A_2 D_1 - A_1 D_2) + A_1 C_2 D_3)}{C_3((A_1 B_2 - A_2 B_1)C_3 - A_1 B_3 C_2)}. \tag{B.6}$$

B.1. Only Inv_1 operates in the linear region

When only Inv_1 begins operating in the linear region, the discharge current of Inv_2 and Inv_3 (I_2 and I_3) is a constant, i.e., $\mathrm{d}I_2/\mathrm{d}t = 0$ and $\mathrm{d}I_3/\mathrm{d}t = 0$ (neglecting the Early effect). Therefore, the differential equations, (3)–(5), become

$$(1 + R_1\gamma_{n1})C_{1t}\frac{\mathrm{d}V_1}{\mathrm{d}t} - C_{12}\frac{\mathrm{d}V_2}{\mathrm{d}t} = -\gamma_{n1} V_1, \tag{B.7}$$

$$C_{2t}\frac{\mathrm{d}V_2}{\mathrm{d}t} - (1 + R_1\gamma_{n1})C_{12}\frac{\mathrm{d}V_1}{\mathrm{d}t} - C_{23}\frac{\mathrm{d}V_3}{\mathrm{d}t} = I_2, \tag{B.8}$$

$$C_{3t}\frac{\mathrm{d}V_3}{\mathrm{d}t} - C_{23}\frac{\mathrm{d}V_2}{\mathrm{d}t} = I_3, \tag{B.9}$$

where

$$I_2 = -B_{n2}(V_{dd} - V_{TN})^{n_n}, \tag{B.10}$$

$$I_3 = -B_{n3}(V_{dd} - V_{TN})^{n_n}. \tag{B.11}$$

Defining

$$\psi_1 = t - \tau_{sat}^1, \tag{B.12}$$

substituting t with ψ_1, and applying a Laplace transform to (B.7), (B.8), and (B.9), a solution of the output voltages, $V_1(s)$, $V_2(s)$, and $V_3(s)$, is produced. These expressions maintain the same formulation as (B.4)–(B.6). However, the coefficients are

$$A_1 = (1 + R_1\gamma_{n1})C_{1t}s + \gamma_{n1}, \tag{B.13}$$

$$B_1 = -C_{12}s, \tag{B.14}$$

$$D_1 = (1 + R_1\gamma_{n1})C_{1t}V_{nsat} - C_{12}V_2(\tau_{sat}^1), \tag{B.15}$$

$$A_2 = -(1 + R_1\gamma_{n1})C_{12}, \tag{B.16}$$

$$B_2 = C_{2t}, \tag{B.17}$$

$$C_2 = -C_{23}, \tag{B.18}$$

$$D_2 = \frac{I_2}{s^2}e^{-s\tau_{sat}^1} + \frac{C_{2t}V_2(\tau_{sat}^1)}{s} - \frac{(1 + R_1\gamma_{n1})C_{12}V_{nsat} + C_{23}V_3(\tau_{sat}^1)}{s}, \tag{B.19}$$

$$B_3 = -C_{23}, \tag{B.20}$$

$$C_3 = C_{3t}, \tag{B.21}$$

$$D_3 = \frac{I_3}{s^2}e^{-s\tau_{sat}^1} + \frac{C_{3t}V_3(\tau_{sat}^1) - C_{23}V_2(\tau_{sat}^1)}{s}. \tag{B.22}$$

B.2. Both Inv_1 and Inv_3 operate in the linear region

When both Inv_1 and Inv_2 operate in the linear region, the discharge current of Inv_2 is a constant, i.e., $dI_2/dt = 0$ (neglecting the Early effect). Therefore, the differential equations, (3)–(5), become

$$(1 + R_1\gamma_{n1})C_{1t}\frac{dV_1}{dt} - C_{12}\frac{dV_2}{dt} = -\gamma_{n1}V_1, \tag{B.23}$$

$$C_{2t}\frac{dV_2}{dt} - (1 + R_1\gamma_{n1})C_{12}\frac{dV_1}{dt} - (1 + R_3\gamma_{n3})C_{23}\frac{dV_3}{dt} = I_2, \tag{B.24}$$

$$(1 + R_3\gamma_{n3})C_{3t}\frac{dV_3}{dt} - C_{23}\frac{dV_2}{dt} = -\gamma_{n3}V_3, \tag{B.25}$$

where

$$I_2 = -B_{n2}(V_{dd} - V_{TN})^{n_n}. \tag{B.26}$$

Defining

$$\psi_2 = t - \tau^3_{sat}, \tag{B.27}$$

substituting t with ψ_2, and applying a Laplace transform to (B.23)–(B.25), a solution of the output voltages, $V_1(s)$, $V_2(s)$, and $V_3(s)$, is produced. These expressions maintain the same formulation as (B.4)–(B.6). The coefficients are

$$A_1 = (1 + R_1\gamma_{n1})C_{1t}s + \gamma_{n1}, \tag{B.28}$$

$$B_1 = -C_{12}s, \tag{B.29}$$

$$D_1 = (1 + R_1\gamma_{n1})C_{1t}V_1(\tau^3_{sat}) - C_{12}V_2(\tau^3_{sat}), \tag{B.30}$$

$$A_2 = -(1 + R_1\gamma_{n1})C_{12}, \tag{B.31}$$

$$B_2 = C_{2t}, \tag{B.32}$$

$$C_2 = -(1 + R_3\gamma_{n3})C_{23}, \tag{B.33}$$

$$D_2 = \frac{I_2}{s^2}e^{-s\tau^3_{sat}} + \frac{C_{2t}V_2(\tau^3_{sat})}{s} - \frac{(1 + R_1\gamma_{n1})C_{12}V_1(\tau^3_{sat}) + (1 + R_3\gamma_{n3})C_{23}V_{nsat}}{s}, \tag{B.34}$$

$$B_3 = -C_{23}s, \tag{B.35}$$

$$C_3 = (1 + R_3\gamma_{n3})C_{3t}s + \gamma_{n3}, \tag{B.36}$$

$$D_3 = (1 + R_3\gamma_{n3})C_{3t}V_{nsat} - C_{23}V_2(\tau^3_{sat}). \tag{B.37}$$

B.3. Inv_1, Inv_2, and Inv_3 all operate in the linear region

When Inv_1, Inv_2, and Inv_3 all operate in the linear region, the differential equations, (3)–(5), become

$$(1 + R_1\gamma_{n1})C_{1t}\frac{dV_1}{dt} - C_{12}\frac{dV_2}{dt} = -\gamma_{n1}V_1, \tag{B.38}$$

$$(1 + R_2\gamma_{n2})C_{2t}\frac{dV_2}{dt} - (1 + R_1\gamma_{n1})C_{12}\frac{dV_1}{dt} - (1 + R_3\gamma_{n3})C_{23}\frac{dV_3}{dt} = -\gamma_{n2}V_2, \tag{B.39}$$

$$(1 + R_3\gamma_{n3})C_{3t}\frac{dV_3}{dt} - C_{23}\frac{dV_2}{dt} = -\gamma_{n3}V_3. \tag{B.40}$$

Defining

$$\psi_3 = t - \tau^2_{sat}, \tag{B.41}$$

substituting t with ψ_3, and applying a Laplace transform to (B.38)–(B.40), a solution of the output voltages, $V_1(s)$, $V_2(s)$, and $V_3(s)$, is produced. These expressions maintain the same formulation as (B.4)–(B.6). The coefficients are

$$A_1 = (1 + R_1\gamma_{n1})C_{1t}s + \gamma_{n1}, \tag{B.42}$$

$$B_1 = -C_{12}s, \tag{B.43}$$

$$D_1 = (1 + R_1\gamma_{n1})C_{1t}V_1(\tau_{sat}^2) - C_{12}V_2(\tau_{sat}^2), \tag{B.44}$$

$$A_2 = -(1 + R_1\gamma_{n1})C_{12}s, \tag{B.45}$$

$$B_2 = (1 + R_2\gamma_{n2})C_{2t}s + \gamma_{n2}, \tag{B.46}$$

$$C_2 = -(1 + R_3\gamma_{n3})C_{23}s, \tag{B.47}$$

$$D_2 = (1 + R_2\gamma_{n2})C_{2t}V_{nsat} - (1 + R_1\gamma_{n1})C_{12}V_1(\tau_{sat}^2) - (1 + R_3\gamma_{n3})C_{23}V_3(\tau_{sat}^2), \tag{B.48}$$

$$B_3 = -(1 + R_2\gamma_{n2})C_{23}s, \tag{B.49}$$

$$C_3 = (1 + R_3\gamma_{n3})C_{3t}s + \gamma_{n3}, \tag{B.50}$$

$$D_3 = (1 + R_3\gamma_{n3})C_{3t}V_3(\tau_{sat}^2) - (1 + R_2\gamma\gamma_{n2})C_{23}V_{nsat}. \tag{B.51}$$

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