Substrate Coupling and Interconnect Noise in Mixed-Signal and High Speed Digital ICs

Eby G. Friedman

Department of Electrical and Computer Engineering
University of Rochester

IEEE CAS Workshop on Mixed-Signal Integrated Circuit Design

December 2, 1999

Presentation Outline

- Introduction to noise in high speed CMOS integrated circuits
- Substrate coupling in mixed-signal integrated circuits
- On-chip inductance
- Peak noise estimation of coupled lossy transmission lines
- On-chip simultaneous switching noise voltage in the power distribution network
- Repeater insertion for driving RLC interconnect
- Conclusions

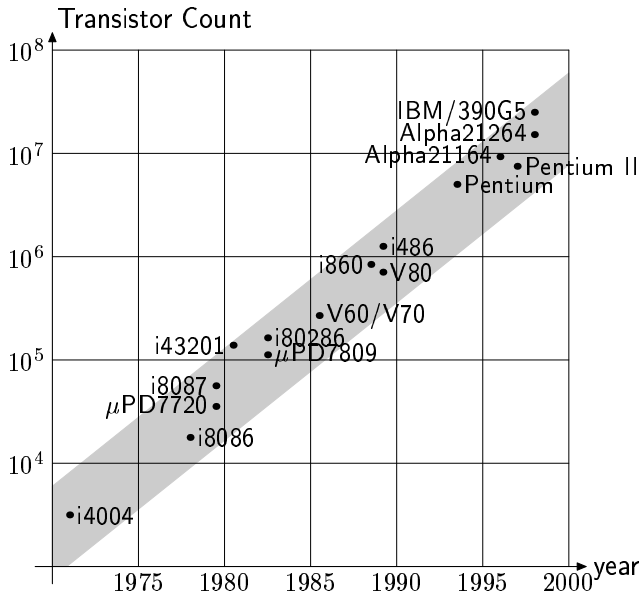
Presentation Outline

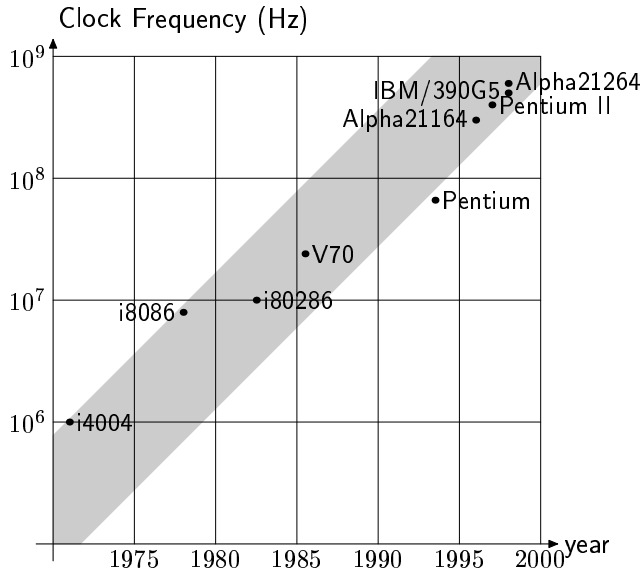
⇨ Introduction to noise in high speed CMOS integrated circuits

- Substrate coupling in mixed-signal integrated circuits
- On-chip inductance
- Peak noise estimation of coupled lossy transmission lines
- On-chip simultaneous switching noise voltage in the power distribution network
- Repeater insertion for driving RLC interconnect
- Conclusions

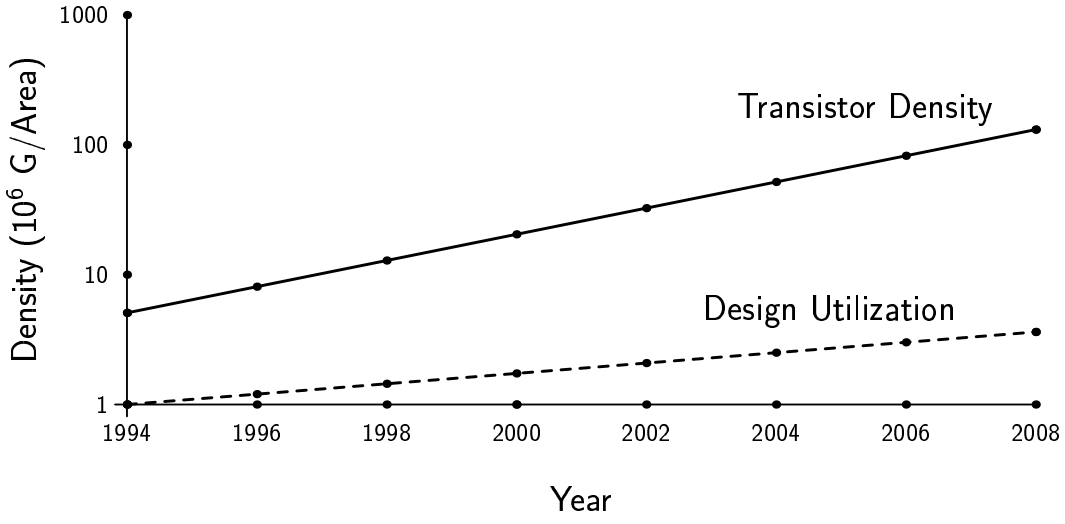
Design Challenge in VDSM CMOS ICs

- Moore's law – exponential increase in circuit integration and clock frequency





- Gap between design productivity and semiconductor manufacturing capability



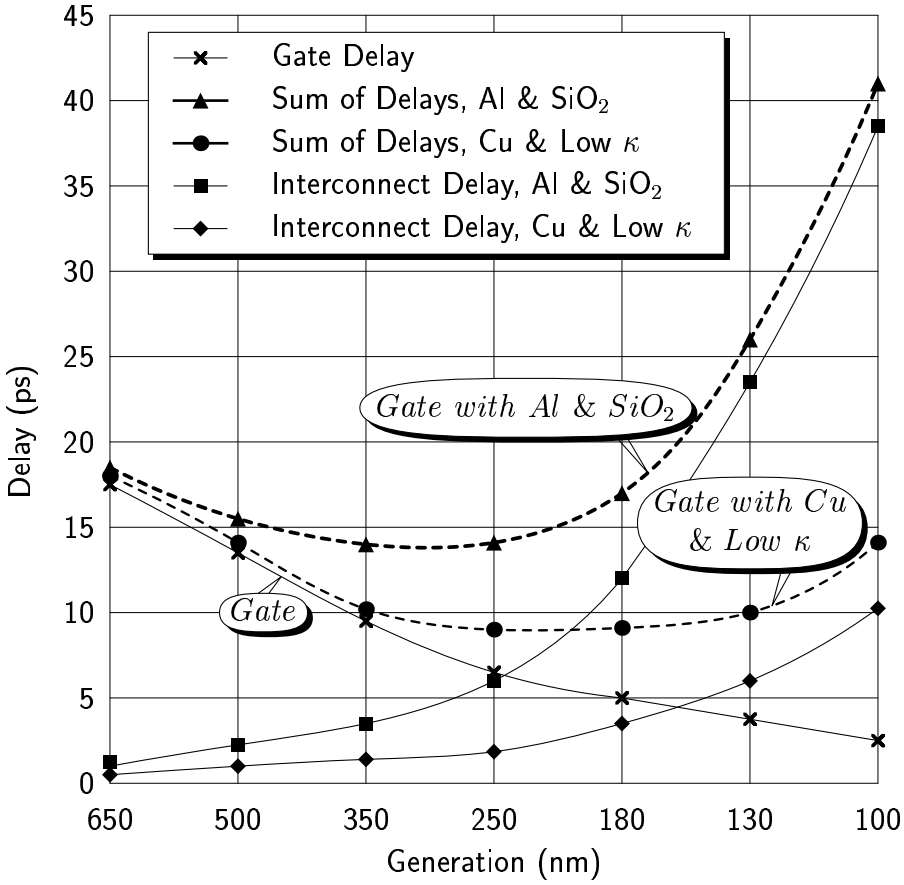
National Technology Roadmap for Semiconductor'97

Technology Characteristics

Year of First Product Shipment	1997	1999	2001	2003	2006	2009	2012
Dense Lines (DRAM half pitch) (nm)	250	180	150	130	100	70	50
Isolated Lines (MPU gates) (nm)	200	140	120	100	70	50	35
Integration Density (transistors/cm^2)							
high volume MPU	3.7 M	6.2 M	10 M	18 M	39 M	84 M	180 M
low volume ASIC	8 M	14 M	16 M	24 M	40 M	64 M	100 M
Chip Frequency (MHz)							
On-chip-local high performance	750	1,250	1,500	2,100	3,500	6,000	10,000
On-chip-across chip high performance	750	1,200	1,400	1,600	2,000	2,500	3,000
Chip Size (mm^2)							
DRAM	280	400	445	560	790	1120	1580
MPU	300	340	385	430	520	620	750
ASIC	480	800	850	900	1000	1100	1300
Supply Voltage V_{dd} (V)	1.8-2.5	1.5-1.8	1.2-1.5	1.2-1.5	0.9-1.2	0.6-0.9	0.5-0.6
Power (W)							
High performance with heatsink	70	90	110	130	160	170	175
Battery handled	1.2	1.4	1.7	2.0	2.4	2.8	3.2

Speed/Performance Issue – Technical Problem

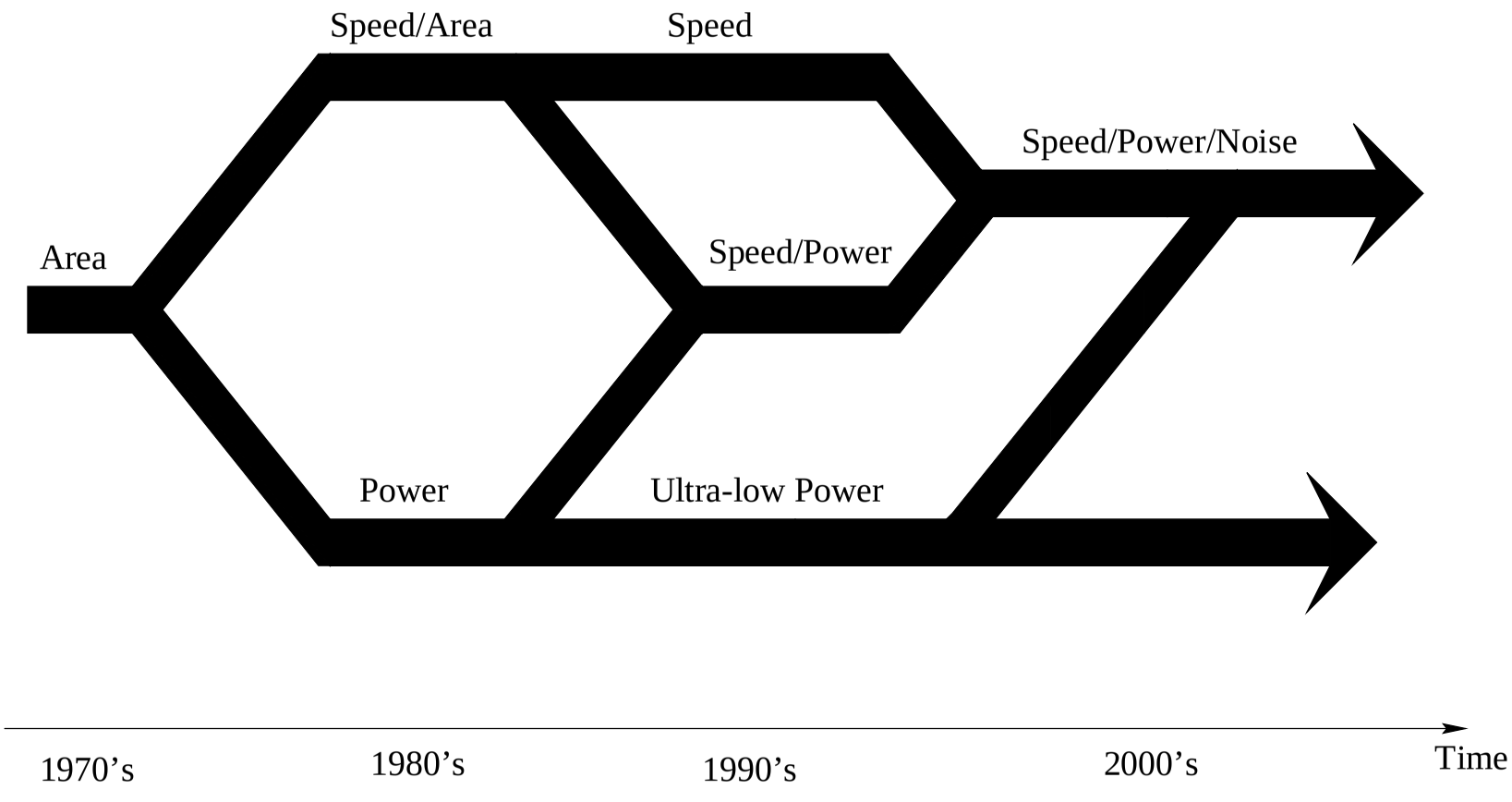
Gate and interconnect delay versus technology generation



Al	$3.0\,\mu\Omega$ -cm
Cu	$1.7\,\mu\Omega$ -cm
SiO_2	$\kappa = 4.0$
Low κ	$\kappa = 2.0$
Al & Cu	$0.8\,\mu$ Thick
Al & Cu Line	$43\,\mu$ Long

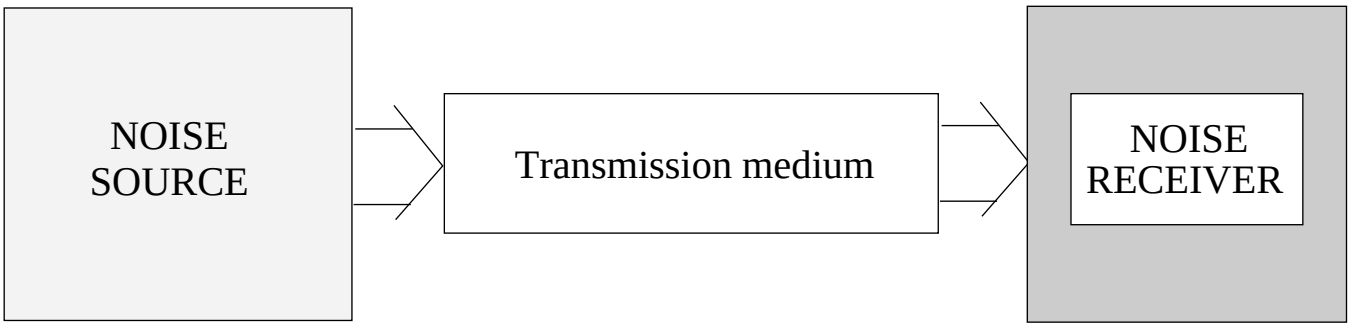
The National Technology Roadmap for Semiconductors, 1997

Design Goals in CMOS Integrated Circuits



Noise Coupling – The General Case

- Noise



  - Generation
  - Transmission
  - Reception

- General applications
  - Digital Influencing Digital
  - Analog Influencing Analog

- Mixed-signal applications
  - Digital Influencing Analog
  - Analog Influencing Digital

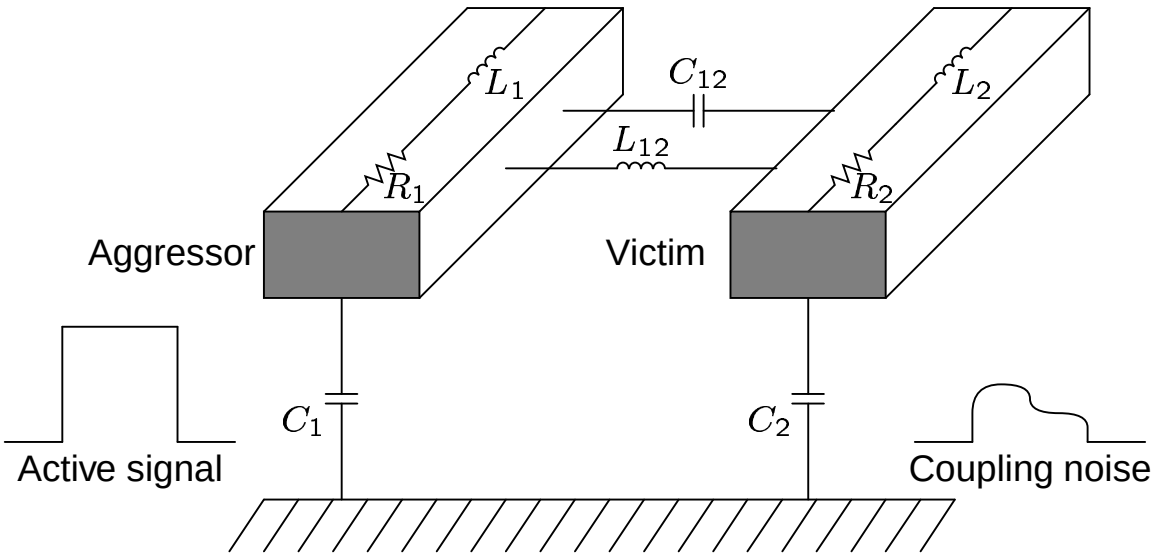
Concept of Noise in Digital CMOS ICs

- Definition of noise

> "The word *noise* in the context of digital circuits means *unwanted variation of voltages and currents at the logic nodes*."
>
> — Jan Rabaey, UC Berkeley

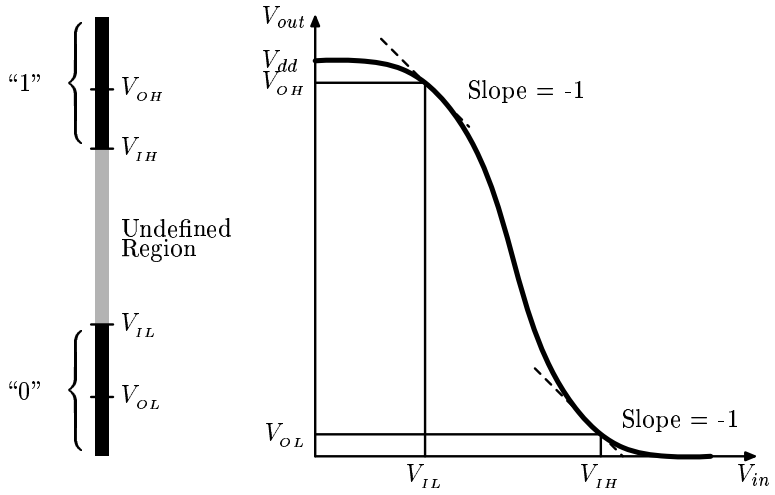
> "Noise in a digital CMOS VLSI chip is predominantly due to coupling from other digital nodes, and not caused by *intrinsic* noise generated by FETs or by any other active devices."
>
> — Masakazu Shoji, AT&T Bell Labs

- Aggressor and victim interconnects

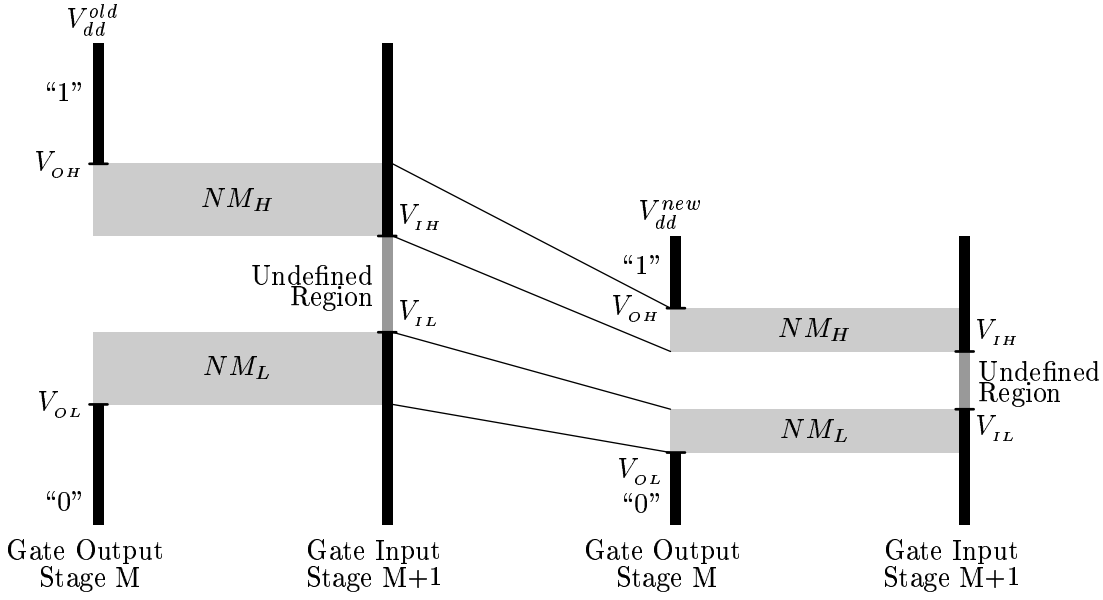


Noise Margins in CMOS Digital Circuits

- Noise margin of a CMOS inverter



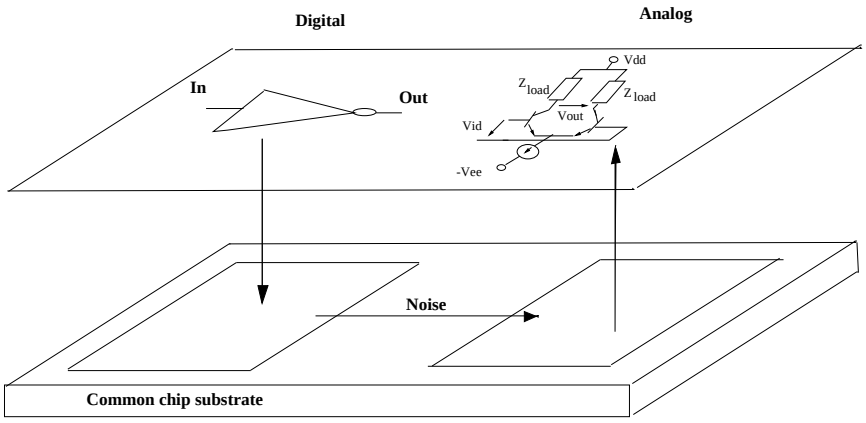
- Decreasing noise margins



Noise in Mixed-Signal Integrated Circuits

Digital Influences Analog

- Analog circuits and signals

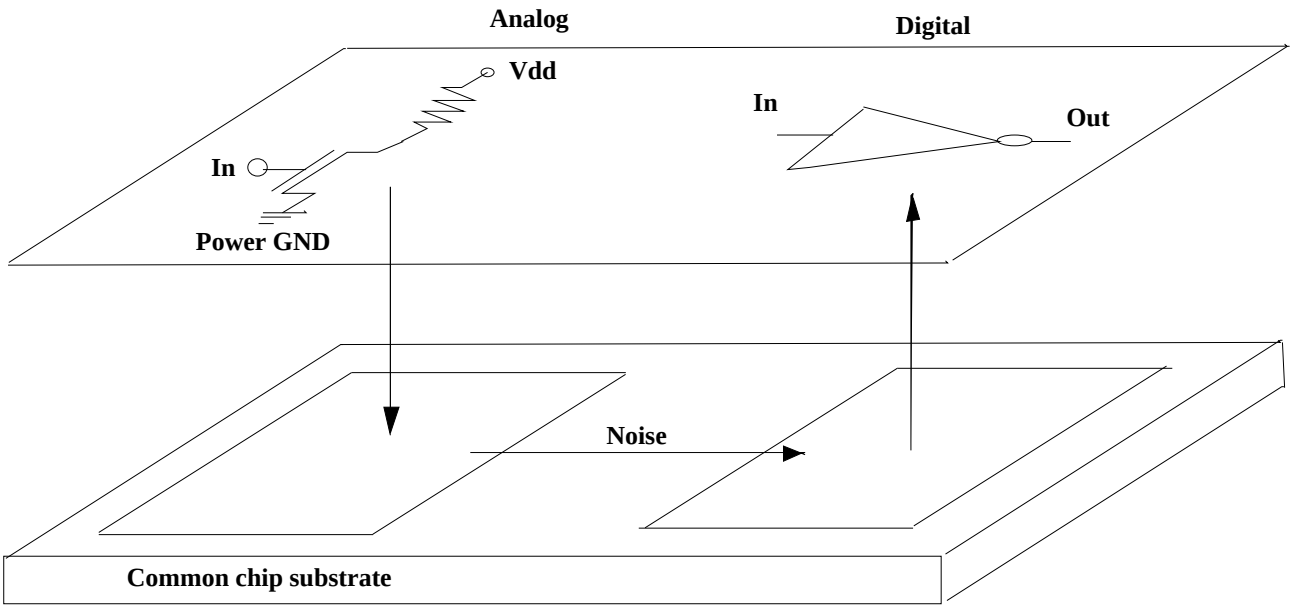


  - Sensitive analog circuits can be highly susceptible to noise
- Digital circuits and signals
  - More tolerant to noise
  - The noise threshold is the noise that induces a change of logical state
- Typical examples
  - Digital to Analog Converters
  - Analog to Digital Converters

Noise in Mixed-Signal Integrated Circuits

Analog Influences Digital

- In smart-power circuits
  - High substrate noise levels are present
  - A noise threshold can be surpassed



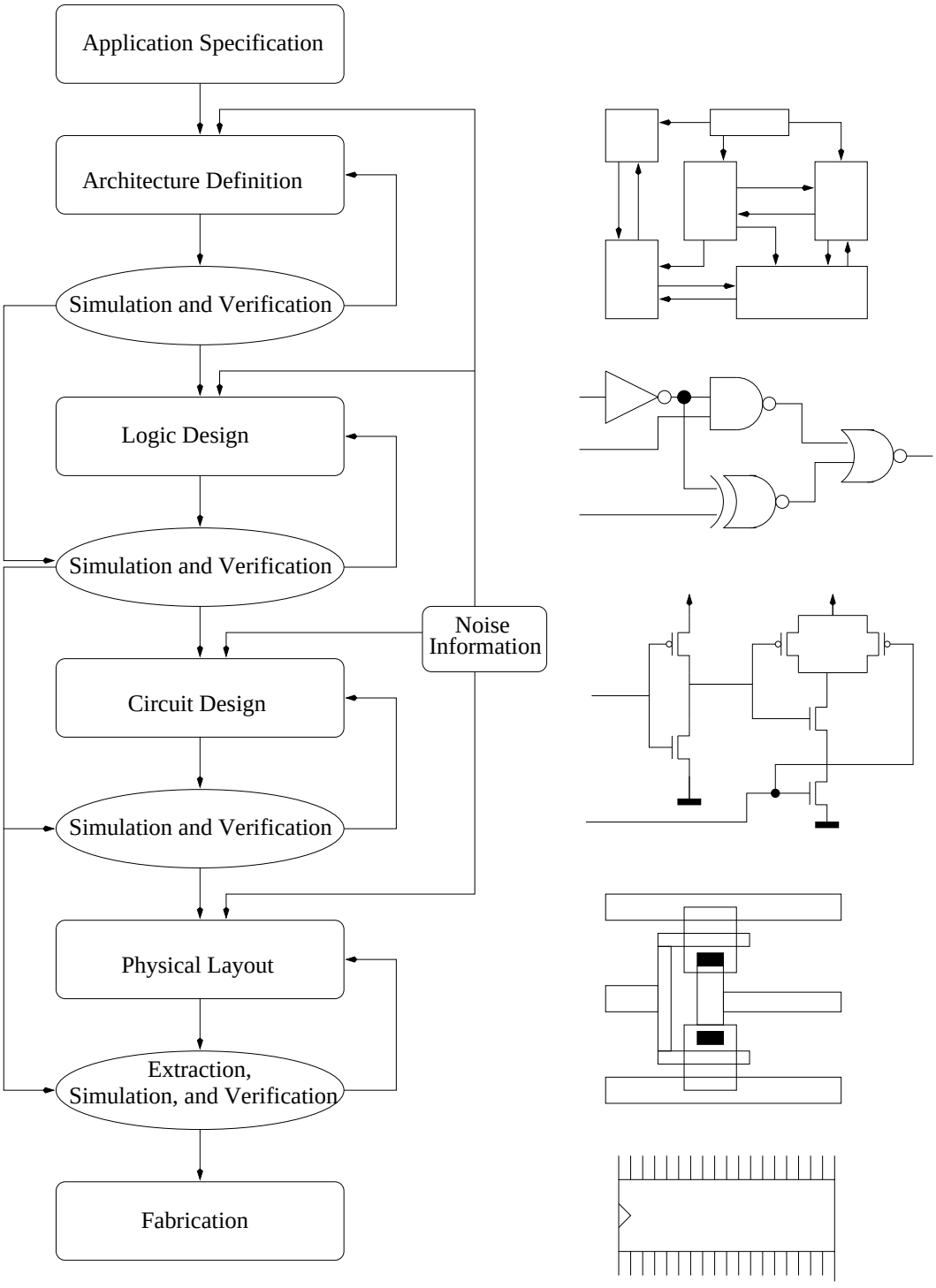
On-Chip Noise Sources in Integrated Circuits

- Substrate coupling noise (substrate crosstalk)
- Interconnect related coupling noise
  - On-chip inductance
    - degradation of signal quality
  - RC/RLC transmission lines
    - reflections due to impedance mismatch
  - Capacitively and inductively coupled interconnect
- On-chip and off-chip simultaneous switching noise
- Transient IR drops in the power distribution network
- Device related noise
  - inherent to the FETs

Design for Noise (DFN)

- **Overall objective:**
  - Incorporate substrate and interconnect noise into the design process
- Provide a capability for estimating noise at the system (or chip) level
- Develop design strategies to reduce substrate and on-chip interconnect noise

Integrate Noise Information into the IC Design Flow



Presentation Outline

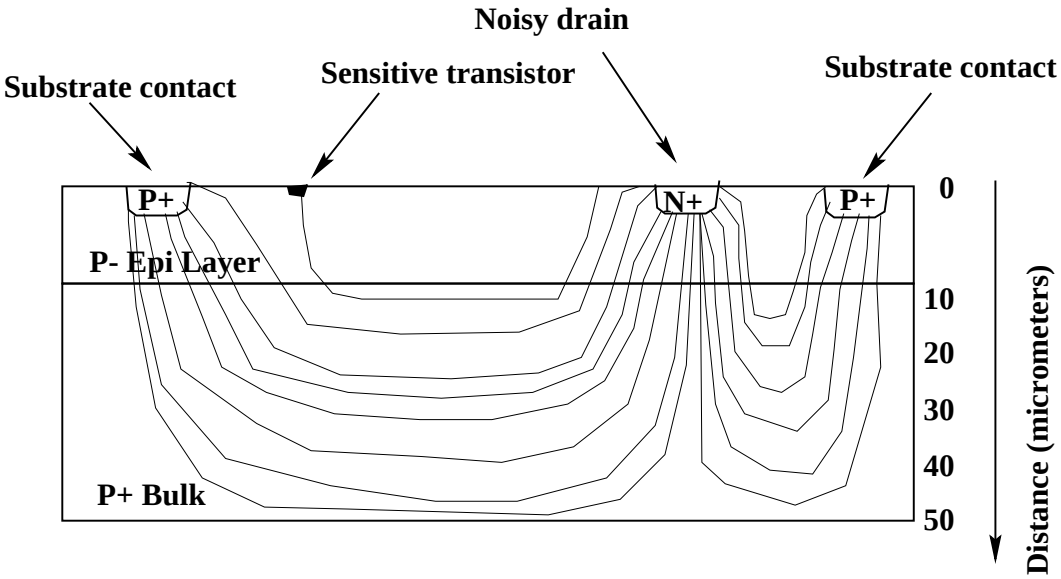
- Introduction to noise in high speed CMOS integrated circuits

⇨ Substrate coupling in mixed-signal integrated circuits

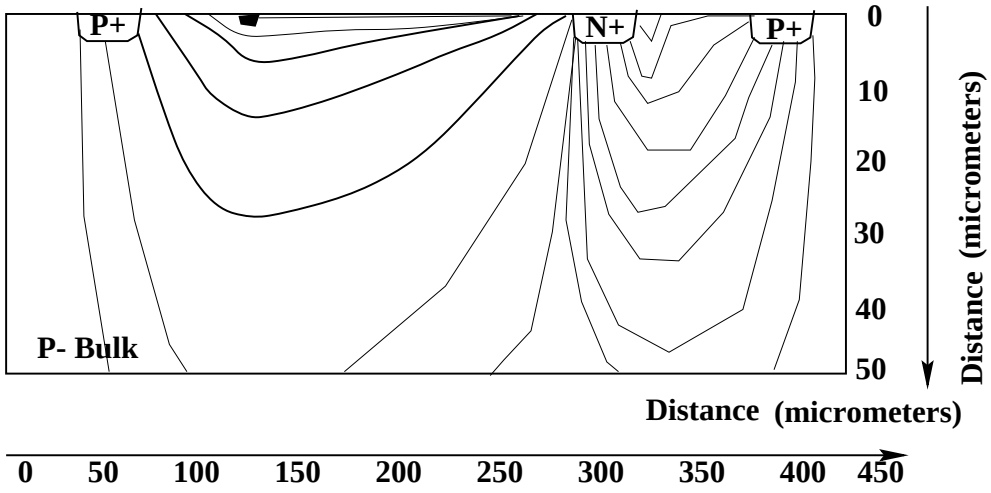
- On-chip inductance
- Peak noise estimation of coupled lossy transmission lines
- On-chip simultaneous switching noise voltage in the power distribution network
- Repeater insertion for driving RLC interconnect
- Conclusions

Noise Flow Within Substrate

- Substrate current flow in a highly doped substrate

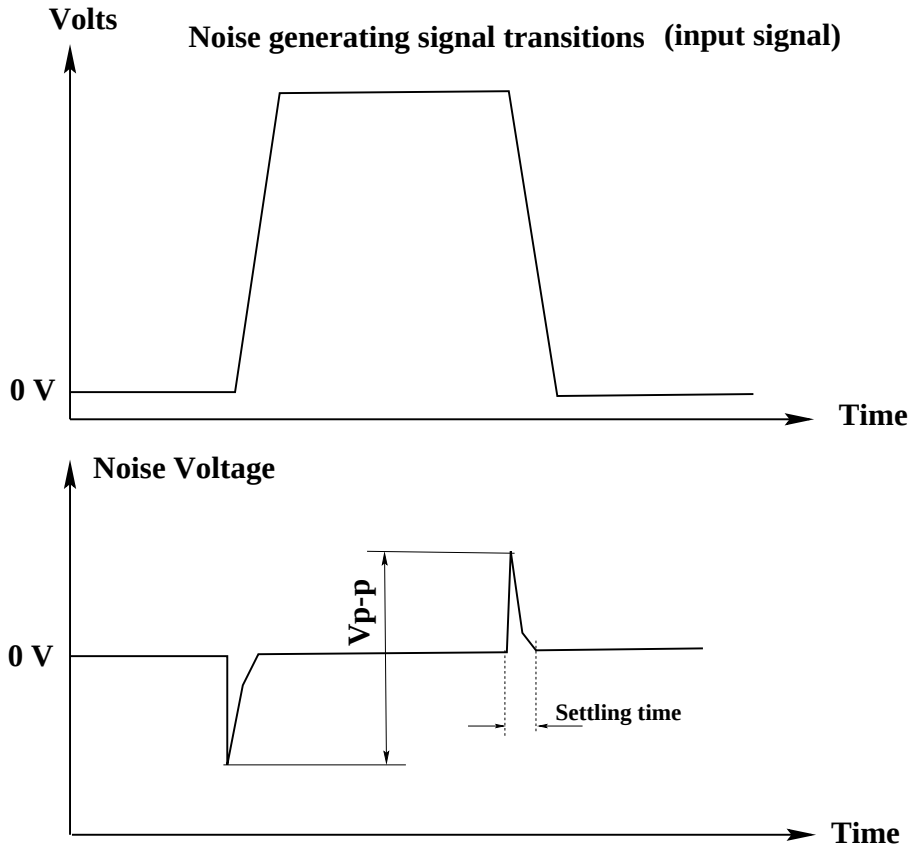


- Substrate current flow in a lightly doped substrate



* Wooley – IEEE JSSC'93

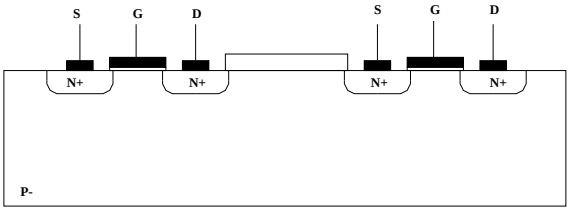
Classic Substrate Noise Waveforms



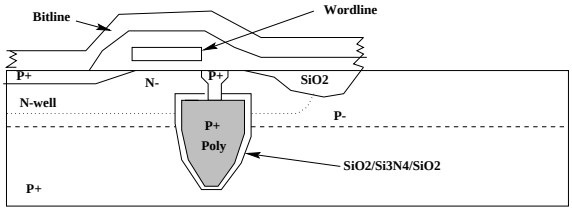
- Influence of
  - Technology
  - Process variables
  - Physical layout
  - Circuit design

* Wooley – IEEE JSSC'93
Rubio – IEE PCDS'95
Masui – IEEE IS VLSI'92
Wooley – IEEE IEDM'96
Fukuda – IEEE JSSC'96

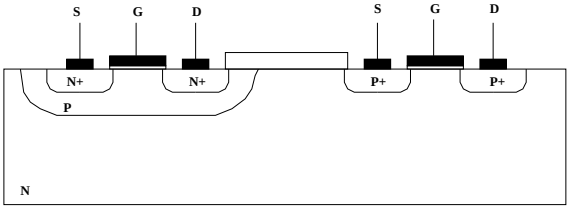
Semiconductor Technologies



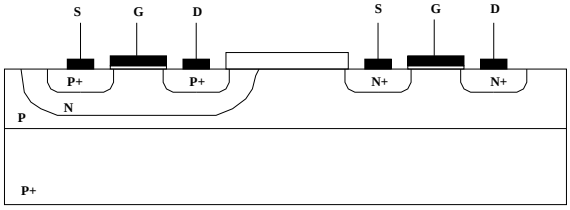
NMOS (PMOS)



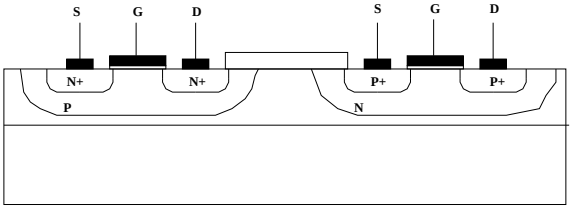
DRAM Technology



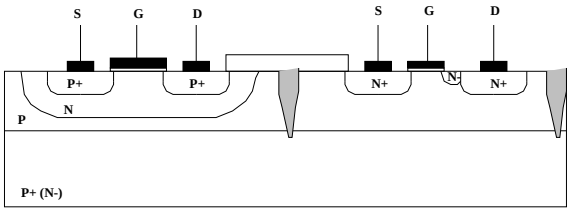
CMOS P-well, no-epi



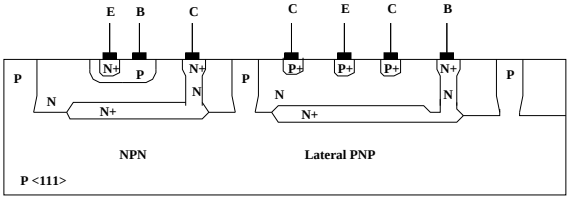
CMOS N-well, epi layer



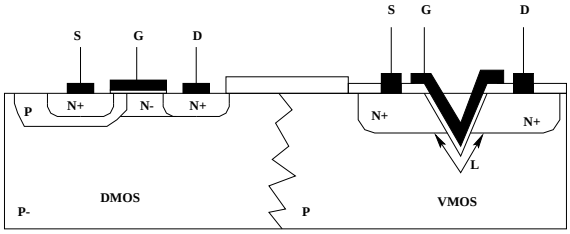
CMOS double-well



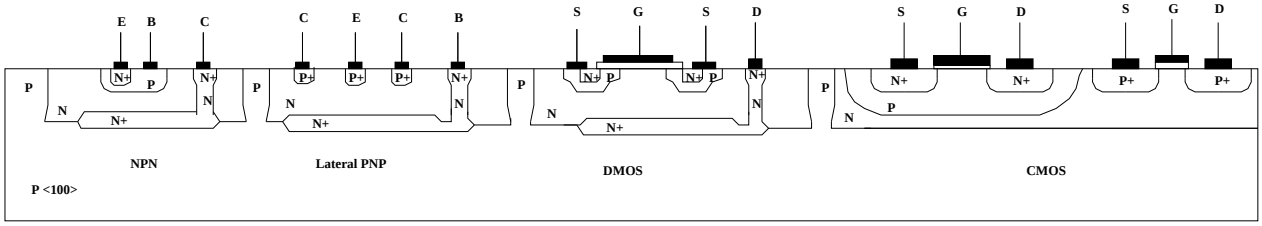
High-Voltage CMOS



Bipolar technologies



DMOS, VMOS technologies



BCD - Bipolar, CMOS, DMOS technologies

Process Variables

- Process variables
  - Substrate doping
    [Wooley1, Rubio]
  - Noise reduction techniques
    [Wooley1, Rubio, Masui, Allstot]
  - Substrate (epitaxial layer) thickness
    [Rubio]
  - Backplane substrate contact
    [Wooley1, Rubio, Masui, Wooley2, Allstot]
  - Bonding wires and number of pads
    [Wooley1, Rubio, Masui, Allstot]

* Wooley1 – IEEE JSSC'93
Rubio – IEE PCDS'95
Masui – IEEE IS VLSI'92
Wooley2 – IEEE IEDM'96
Allstot – IEEE JSSC'94

Circuit and Physical Design

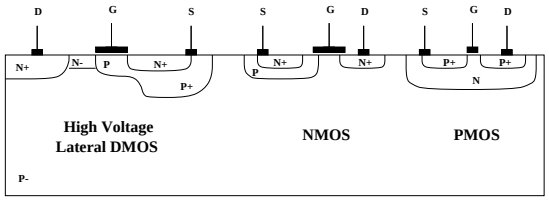
- Circuit design
  - Switching speed and transition times
    [Wooley1, Rubio, Wooley2]
  - Interaction among different types of transistors
    [Rubio]
  - Size of the logic circuits
    [Wooley2]

- Physical layout
  - Distance between the noise source and receiver
    [Wooley1, Rubio, Lewis, Troutman]
  - Placement of the substrate contacts
    [Wooley2]
  - Routing of power lines
    [Allstot1, Vulih]
  - Relative placement of the logic and analog blocks
    [Rubio, Allstot2]

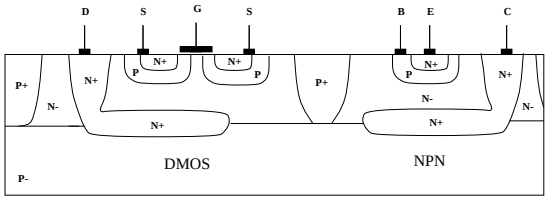
* Wooley1 – IEEE JSSC'93
Rubio – IEE PCDS'95
Wooley2 – IEEE IEDM'96
Lewis – IEEE IEDM'86
Troutman – IEEE IEDM'84
Allstot1 – IEEE JSSC'94
Vulih – IEEE CICC'87
Allstot2 – IEEE CICC'94

Applying Classic Noise Reduction Techniques

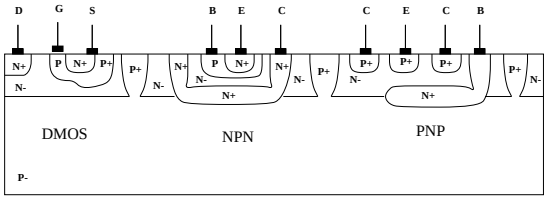
- Specially optimized technologies with increased isolation [Bierman, Korec, Lanca, Baliga]



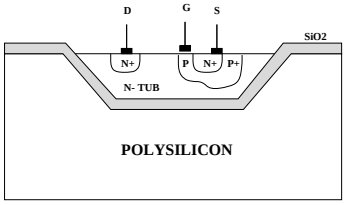
The self-isolation technique



The thick epitaxial layer junction isolation technique



RESURF junction isolation technique



Dielectric isolation technique

* Bierman – Electronics'85
Korec – SSMAT'95
Lanca – ISIE'97
Baliga – IEEE TED'86

Approach for System on a Chip (SOC)

- Constituent blocks of an SOC
  - Digital circuit blocks
  - Analog circuit blocks
  - Smart-power circuit blocks

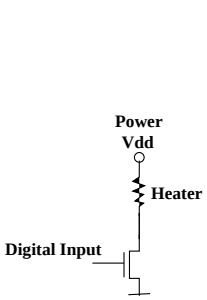
- Presently, special technologies are used to mitigate noise in mixed-signal applications

- Primary research objectives:
  - Eliminate the need for specialized technologies
  - Permit low cost monolithic SOC integration with high performance
  - Develop
    - Circuit and physical design solutions to improve circuit noise immunity
  - Create
    - Low cost smart-power circuitry

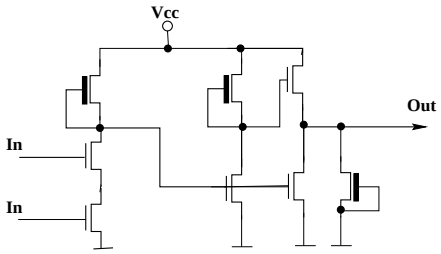
Circuit Characteristics

- NMOS implementation - Thermal Ink Jet (TIJ) printer
  - An analog high-power noise source
  - A digital noise receptor

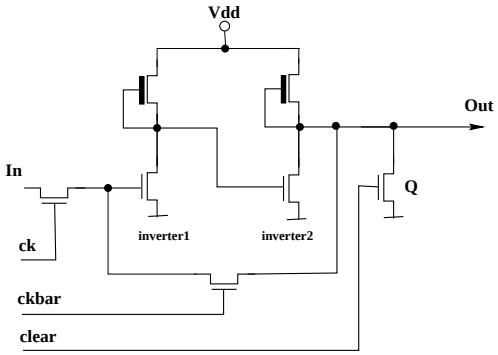
    [Verdonckt-Vandebroek – IEEE CDM'97]



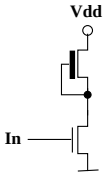
NMOS power driver



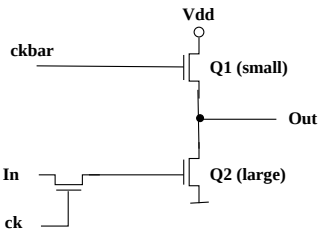
13 volt predriver



NMOS static slave latch



NMOS Inverter



NMOS dynamic latch

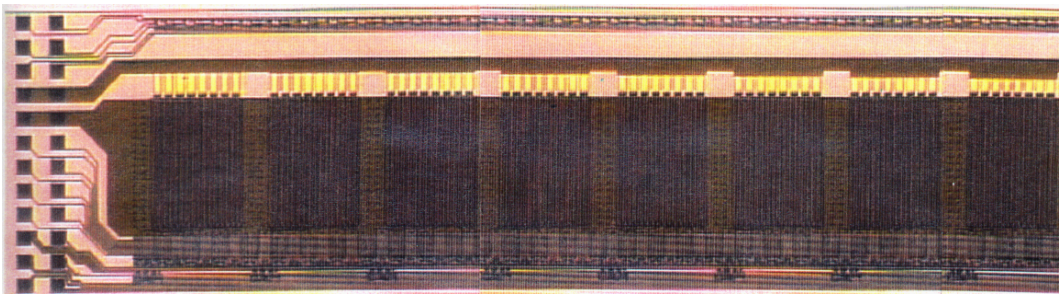
Test circuits

- 50 NMOS test circuits have been fabricated in a 3.5 μm technology to analyze the influence of
  - *Digital influencing analog* issues [Wooley1, Rubio Wooley2, Allstot1, Lewis, Troutman, Vulih, Allstot2]
    - Distance
    - Noise reduction techniques
    - Placement of substrate contacts
    - Switching speed and transition times
    - Interaction among different transistors
    - Routing of the power lines
    - Logic blocks placement and orientation
  - *Smart-power specific* issues
    - Power driver supply voltage and current
    - Size of the noise source
    - Clock and signal conditioning
    - Power drivers “on-off” timing with respect to register clocking
    - Duration of noise pulse
    - Chip temperature

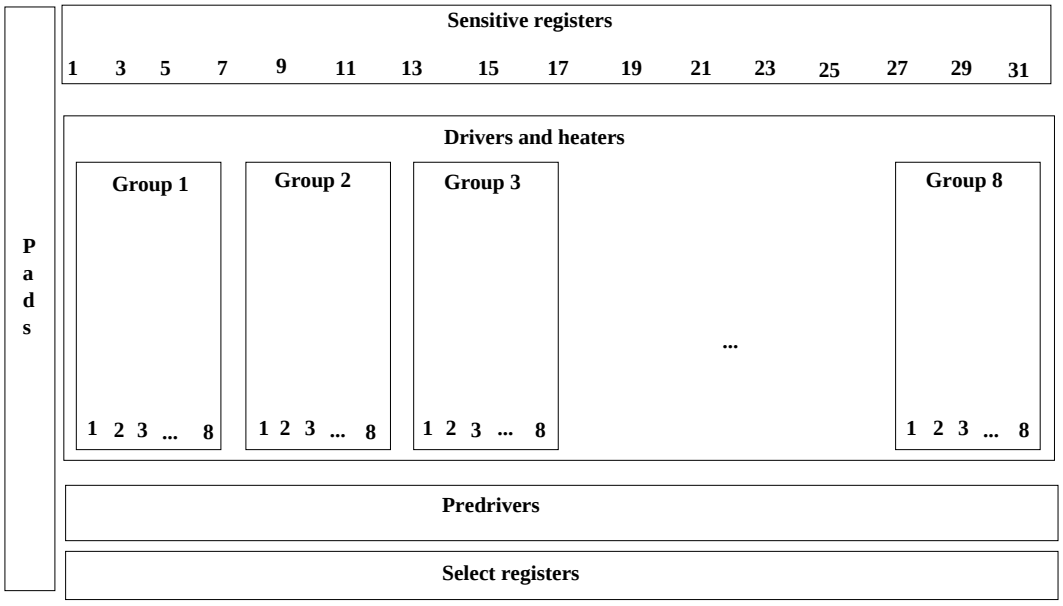
* Wooley1 – IEEE JSSC’93
Rubio – IEE PCDS’95
Wooley2 – IEEE IEDM’96
Allstot1 – IEEE JSSC’94
Lewis – IEEE IEDM’86
Troutman – IEEE IEDM’84
Vulih – IEEE CICC’87
Allstot2 – IEEE CICC’94

Physical Layout of Test Circuits

- Microphotograph of test circuit used to evaluate effect of noise in digital registers from high-power analog drivers

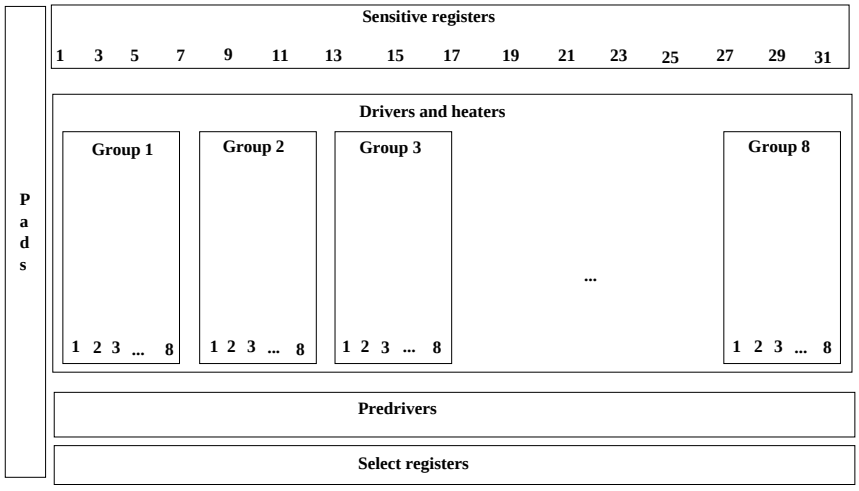


- Floorplan



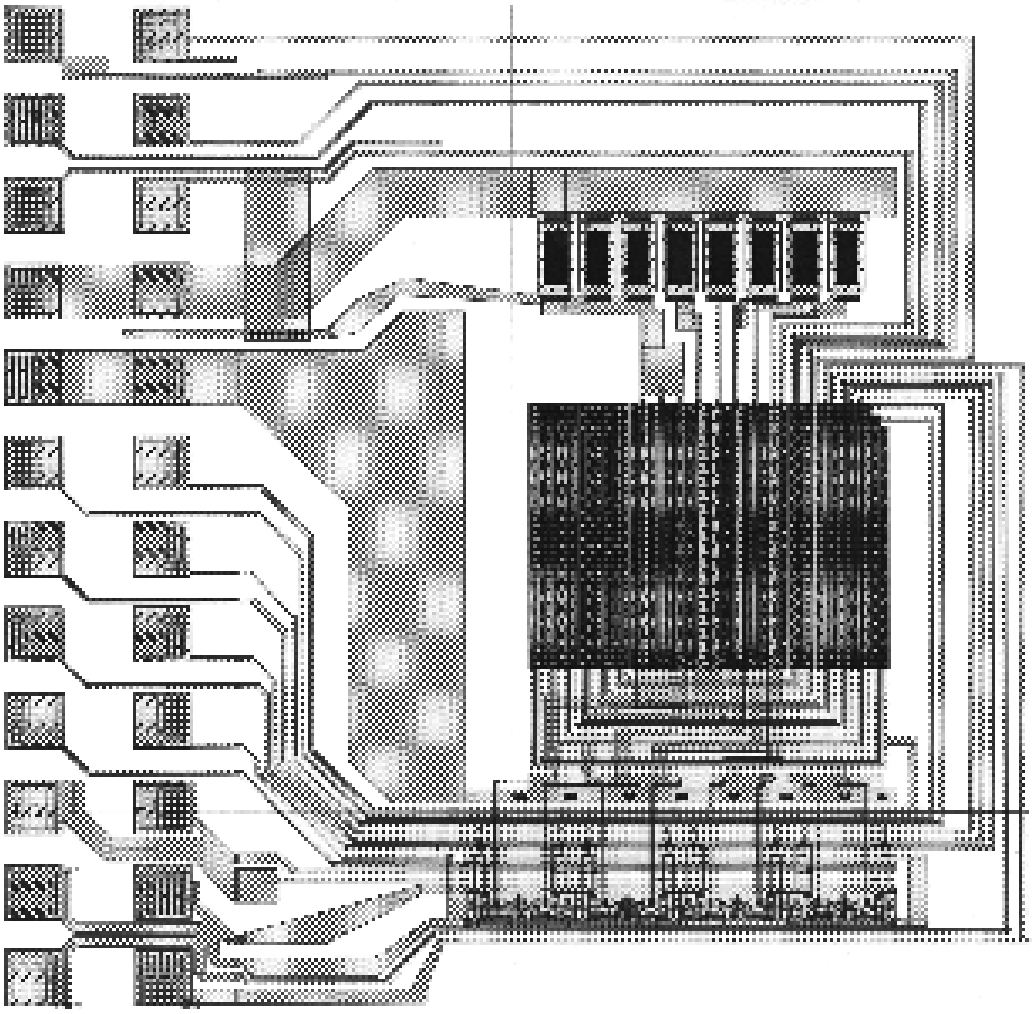
Architectural Aspects

- Noise source
  - High voltage and high current power drivers
- Noise medium
  - Common substrate region
- Noise receptor
  - Static and dynamic latches



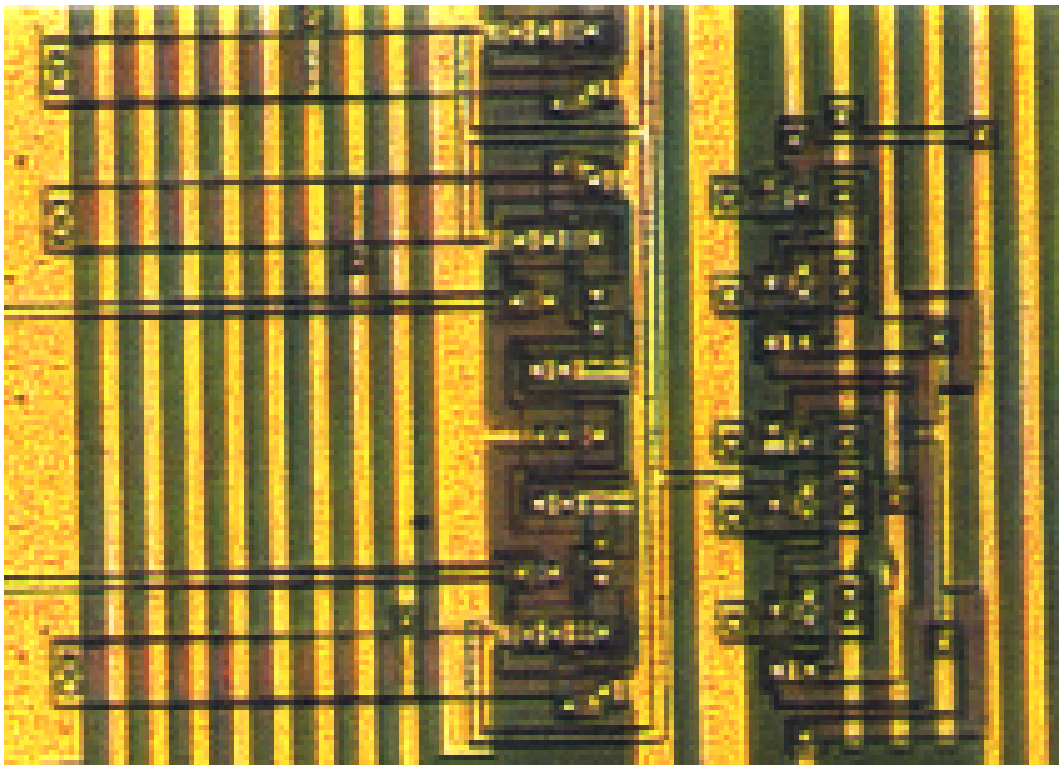
Physical Layout of Test Circuits

- Test circuit used to evaluate noise waveforms within the substrate



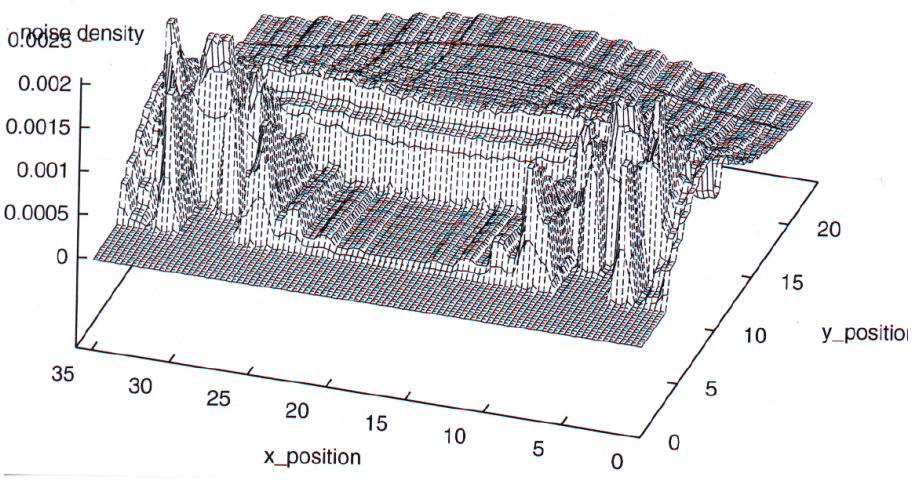
Physical Layout Detail

- Microphotograph of the latch-predriver-driver interface

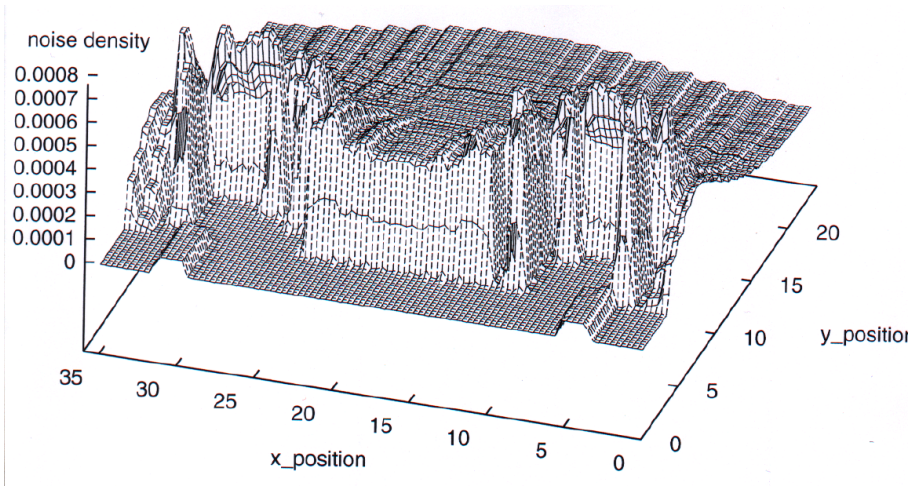


Noise Distributions for Epi and Non-Epi Technologies

- Distributions for Epi technologies



- Distributions for Non-Epi technologies

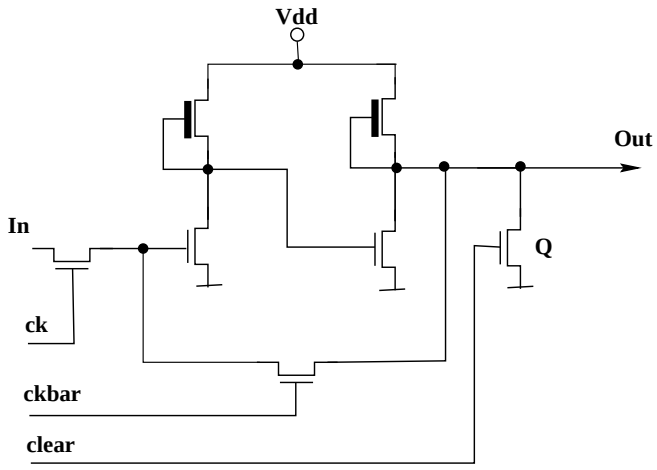


Issues Specific to Noise Coupling

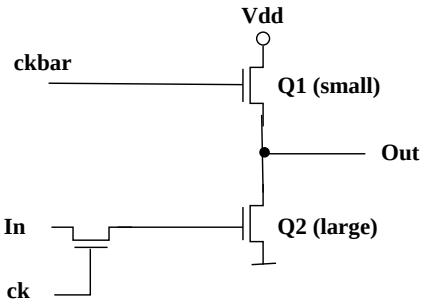
- Technology
  - Substrate doping
  - Substrate (epitaxial layer) thickness
  - Backplane substrate contact
- Physical Design
  - **Distance between the noise source and receiver**
  - **Noise reduction techniques**
    - **Rings**
    - **Substrate contacts**
  - **Placement of the substrate contacts**
  - **Routing of the high current power lines**
  - **Relative placement of the logic and analog blocks**
- Circuit Design
  - Switching speed and transition times
  - Interaction among different types of transistors
  - Size of the logic circuits
  - **Static vs. dynamic registers**

Dependence of Noise on the Input Data

- A parasitic transition is induced at the register output
  - For static master-slave registers
    - Only if input data is logic high
  - For dynamic registers
    - For both input logic high and logic low
    - Input low is more sensitive than input high



NMOS Static Slave Latch

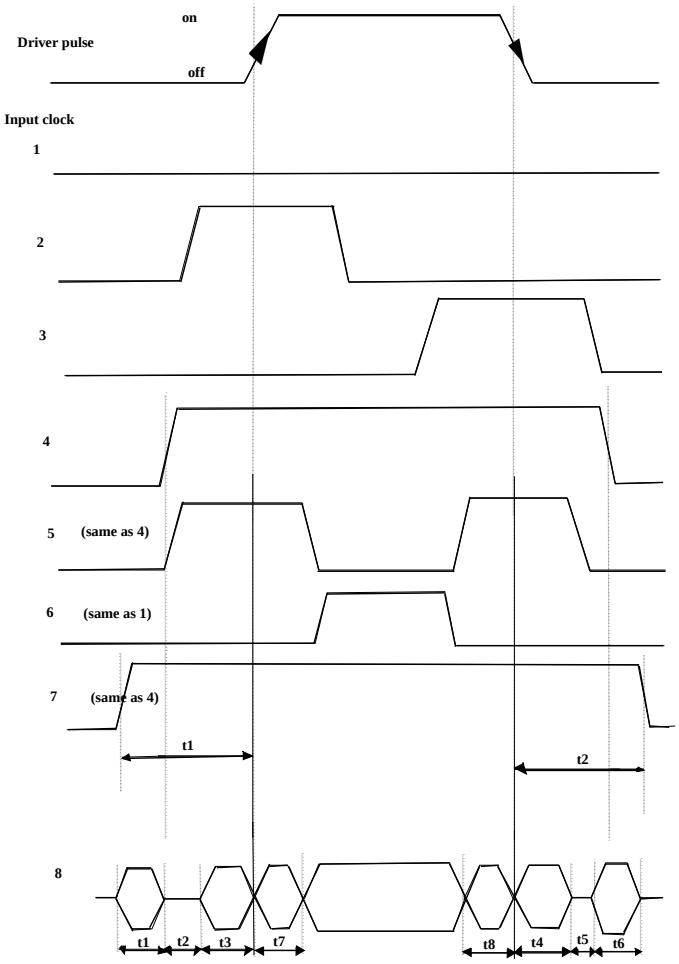


NMOS Dynamic Latch

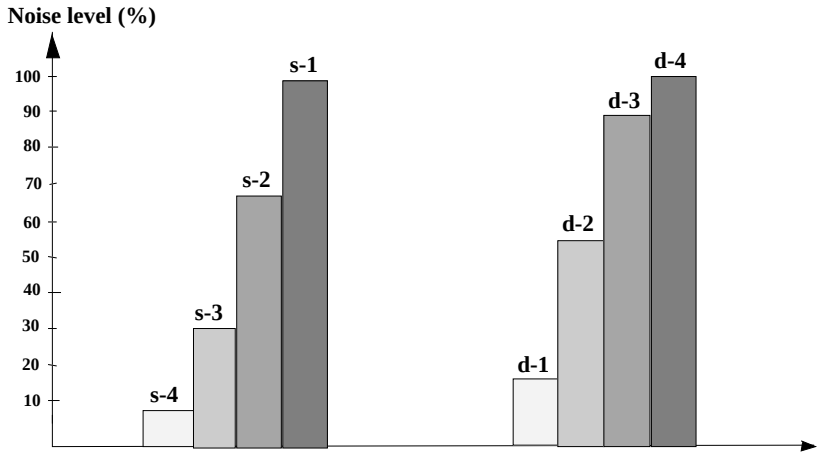
Dependence of Noise on Register Clocking

- Static registers
  - 4, 3, 2, 1 where 4 = best, 1 = worst

- Dynamic registers
  - 1, 2, 3, 4 where 1 = best, 4 = worst

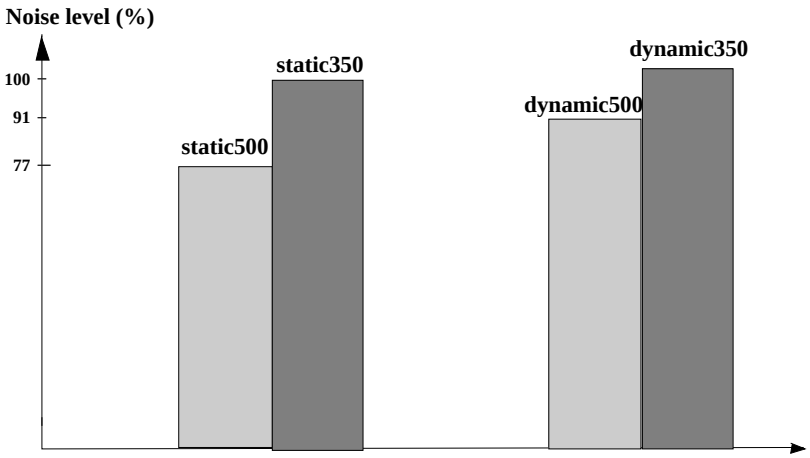


Dependence of Noise on Register Clocking (Cont.)



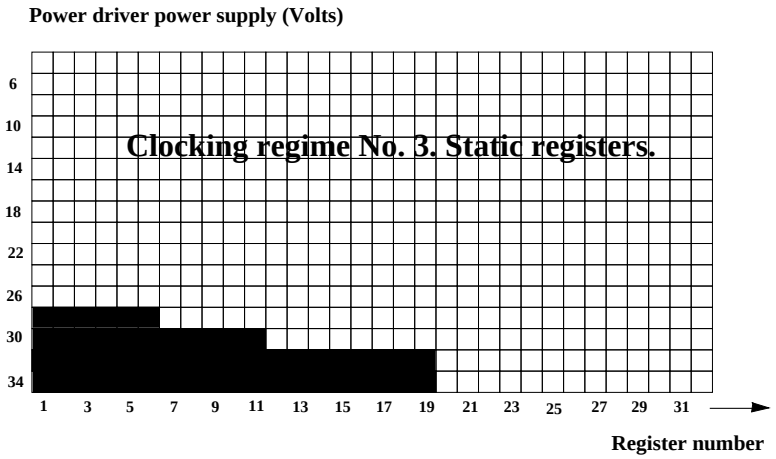
- Relative dependency shown in number of affected registers
- The number of affected dynamic registers (d-4) is 1.3X larger than the number of affected static registers (s-1)
- Noise tolerance further improved with
  - Substrate contact placement
  - Ground routing
  - Register orientation
    - Depletion transistors placed closer to the noise source

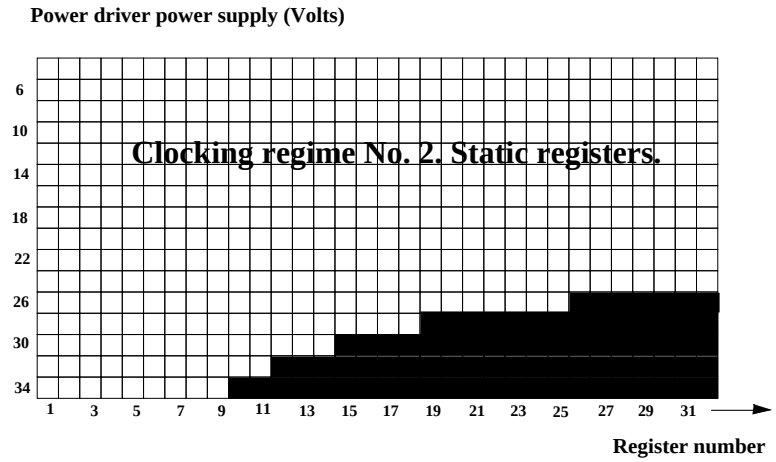
Dependence of Noise on Distance



- Relative dependency shown in number of affected registers
- The number of affected dynamic registers (dynamic350) is 1.15X larger than the number of affected static registers (static350)
- Two distances evaluated
  - 350 μm
  - 500 μm

Noise Spreading Effects

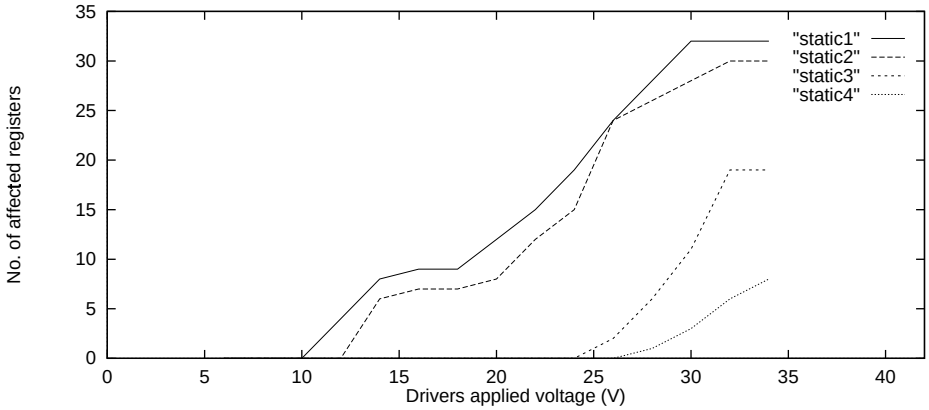




- Specific registers are affected depending on
  - Clocking regime
  - Ground bias
  - Active power driver group

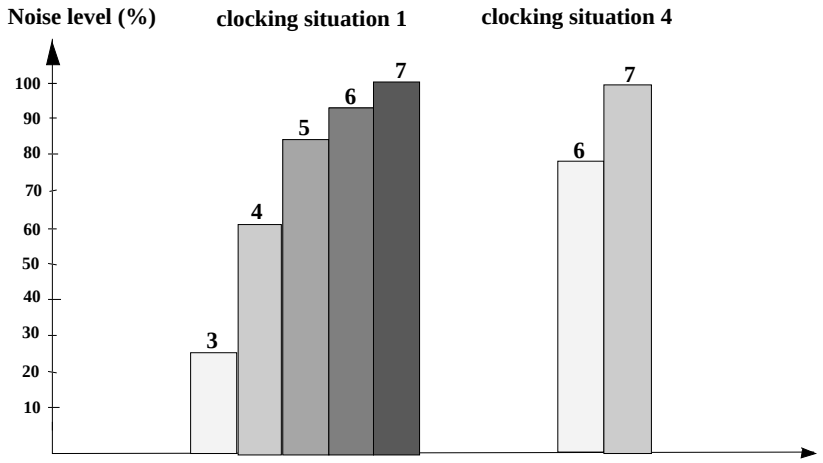
Influence of Analog Power Supply

- More registers are affected as
  - The driver power supply increases
  - The clocking regime changes
  - The noise pulse duration increases



- Slight dependency with chip temperature is noted
  - Less than 5% for a 25^{o} to 55^{o}C temperature sweep range

Influence of the Size of the Noise Source



- Relative dependency shown in number of affected registers
- The number of registers is 30X smaller for clocking regime 4 (seven active drivers) than for clocking regime 1 (seven active drivers)
- The noise tolerance improves for on-chip connected digital and analog ground lines

Related Publications on Substrate Coupling

- R. M. Secareanu, S. Warner, S. Seabridge, C. Burke, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, “Substrate Noise Distribution and Placement of Substrate Contacts to Alleviate Substrate Noise in Epi and Non-Epi Technologies,” *Proceedings of the 23rd Annual IEEE EDS/CAS Activities in Western New York Conference*, pp. 10-11, November 1999.

- R. M. Secareanu, I. S. Kourtev, J. Becerra, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, “The Behavior of Digital Circuits under Substrate Noise in a Mixed-Signal Smart Power Environment,” *Proceedings of the IEEE International Symposium on Power Semiconductor Devices and ICs*, pp. 253-256, May 1999.

- R. M. Secareanu, I. S. Kourtev, J. Becerra, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, “Noise Immunity of Digital Circuits in Mixed-Signal Smart Power Systems,” *Proceedings of the IEEE Great Lakes Symposium on VLSI*, pp. 314-317, February 1999.

Presentation Outline

- Introduction to noise in high speed CMOS integrated circuits
- Substrate coupling in mixed-signal integrated circuits

⇨ On-chip inductance

- Peak noise estimation of coupled lossy transmission lines
- On-chip simultaneous switching noise voltage in the power distribution network
- Repeater insertion for driving RLC interconnect
- Conclusions