An NBTI-Aware Digital Low-Dropout Regulator with Adaptive Gain Scaling Control

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***Abstract*—Digital low-dropout voltage regulators (DLDOs) have drawn increasing attention for the easy implementation within nanoscale devices. Despite their various benefits over analog LDOs, disadvantages may arise in the form of negative bias temperature instability (NBTI) induced performance degradation. In this paper, a simple and effective adaptive gain scaling (AGS) technique with a steady-state capture feature is proposed. AGS senses the steady-state output of a DLDO and reduces the gain to the minimum value to obtain a stable output voltage. Moreover, a novel uni-directional barrel shifter is proposed to reduce the aging effect of the DLDO. This uni-directional barrel shifter evenly distributes the load among DLDO output stages to obtain a longer lifetime. The benefits of the proposed techniques are explored and highlighted through extensive simulations. The proposed techniques also have negligible power and area overhead. NBTI-aware design with AGS can reduce the transient response time by 59.5% as compared to aging unaware conventional DLDO and can mitigate the aging effect up to 33%.**

I. Introduction

The semiconductor technology that enables nanoscale integrated circuits advance continuously improve while these circuits demand a higher amount of power per unit area [1]. Implementing voltage regulators on-chip voltage regulators that provide robust power to the integrated circuits have been a challenging design issue. Modern microprocessors and internet of things (IoT) devices require reliable operation and long lifetime of on-chip voltage regulators [2], [3]. Generating and delivering a robust output voltage under highly dynamic workload conditions become even more difficult with the variations in the environmental conditions. These environmental conditions deteriorate the performance and lifetime of the transistors. Integrated circuits also suffer from the abrupt voltage variations in the workload and may experience serious aging phenomenon [2].

Transistor aging mechanisms such as bias temperature instability (BTI), hot carrier injection, and time-dependent dielectric breakdown have become more important with the scaling of transistor size. BTI is the major aging mechanism [4]-[6]. Negative BTI (NBTI) induces performance degradation of PMOS transistors. Various studies have been performed to address the reliability issues of semiconductor devices [7]-[11]. These are BTI-aware sleep transistor sizing algorithms for reliable power gating design [7], the integral impact of BTI and PVT variation [8], and the impact of BTI variations [9]. A conventional DLDO has a bi-directional controller which activates certain transistors frequently and leaves the others unused. This security unaware control scheme makes the performance degradation even worse because the activation pattern of PMOS is concentrated on certain transistors, thus causing heavy electrical stress on these transistors. The over usage of certain transistors degrades the performance significantly. Distributing the electrical stress among all of the transistors can be effective. The primary literature that address the aging effects of on-chip DLDOs include a reliable digitally synthesizable linear drop-out regulator design, a digitally controlled linear regulator for per-core wide-range DVFS of Atom^{TM} cores, and mitigation of NBTI induced performance degradation in on-chip DLDOs [12], [13], [2]. To evenly distribute the workload, a decoding algorithm for DLDO is proposed in [12]. A code roaming algorithm with per-core dynamic voltage and frequency scaling method is proposed in [13]. A uni-directional shifter is proposed in [2] which can decrease the stress on transistors. These techniques need dedicated control algorithms to enhance the reliability of a DLDO. A DLDO without AGS, however, suffers from slow response time due to the large transitions in the load current. The supply voltage should be robust as the operation of all of the on-chip devices are sensitive to the variations at the output of the voltage regulators. Transient performance enhancements and loop stability can be increased by utilizing a barrel shifter as discussed in [15]. A barrel shifter which can perform the switching of two or three transistors at the same clock cycle improves the transient response time significantly. A barrel shifter based DLDO design with a steady load current estimator and dynamic gain scaling control is discussed in [16]. Although there are benefits of these aforementioned techniques, a DLDO with AGS still suffers from performance degradation due to NBTI. A Conventional DLDO with AGS does not consider aging effect. Gain scaling using a bi-directional barrel shifter in [14] may not be directly applicable to add gain scaling capability for a reliability enhanced DLDO. Therefore, further research should be performed on AGS DLDO to mitigate performance degradation due to NBTI. A novel aging aware DLDO with AGS and a steady-state

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detection circuit to obtain fast transient response under abrupt changes in the load current are proposed in this paper.

The main contributions of this paper are threefold. First, an NBTI-aware DLDO with AGS is proposed. Second, a simple and effective steady state, overshoot and undershoot detection circuit is proposed and verified. Third, extensive simulations verify that the proposed circuit works effectively.

The rest of this paper is organized as follows. Background information regarding conventional DLDOs, DLDOs with AGS, barrel shifters, and NBTI is discussed in Section II. NBTI induced performance degradation is discussed in Section III. The proposed NBTI-aware DLDO with AGS is discussed in Section IV. Evaluation of the proposed technique and simulation results are discussed in Section V. Concluding remarks are given in Section VI.

II. Background

In this section, working principles of conventional DLDOs, barrel shifters, a uni-directional digital controller, and adaptive gain scaling are discussed.

A. Conventional DLDO

The schematic of a conventional DLDO [3] is shown in Fig. 1 and its operation principle is described in Fig. 2. The V_{ref} and clk are the input and V_{out} is the output of the conventional DLDO. The digital controller activates each Q_i based on Fig. 1. The DLDO is composed of N parallel PMOS transistors and a feedback control to adjust the output voltage. A bi-directional shift register is implemented in conventional DLDOs. M_i is PMOS and Q_i is the logic output of the digital controller. i denotes the activation stage of the digital controller. The bi-directional shift register switches one of the power transistors according to V_{cmp} at rising edge of each clock cycle. Q_n is the output signal of the digital controller, as shown in Fig. 1. At step k+1, Q_{n+1} (Q_n) is turned on (off) when V_{cmp} is high (low) and the bi-directional shift register shifts right (left), as shown in Fig. 2 where k is the activation stage of the digital controller [2]. Each Mn is connected to Q_n. Since the activation schema is two directional and the limit cycle oscillation at the steady-state are on certain transistors, this scheme leads to heavy usage of M_1 to M_n; thus, performance degradation can occur. Limit cycle oscillation is related to the oscillation of V_{cmp} signal at the steady-stage and this oscillation is observed at the waveform of V_{out}.

Most practical applications need less than average power, which leads to heavy utilization of certain transistors within conventional DLDOs. The undamped voltage output of DLDO causes large swings at the voltage waveform which leads to heavy use of certain transistors. The operation of the regulator causes the heavy use of M_1 to M_m and less or even no use of M_{m+1} to M_N. Certain transistors are always active. This activation scheme can induce serious non-symmetric degradation of PMOS due to NBTI.

B. Barrel shifter

A simple schematic for a barrel shifter is shown in Fig. 3. A barrel shifter can activate multiple power transistors at the same clock cycle. For example, it can shift -3, -2, -1, 0, 1, 2, 3 stages at the same clock cycle. The magnitude of the shift in a barrel shifter serves as a gain control knob in the forward activation pattern of a DLDO. The barrel shifter in Fig. 3, is implemented using two levels of signal multiplexing followed by a flip-flop. A is the output of D flip flop and B is the output of the first level of MUX. The first level of MUX gives 0, 2, -2 and second level of MUX gives 0, 1, -1 shifts to obtain -3, -2, -1, 0, 1, 2, 3 shifts at the output of the barrel shifter. The positive values mean a shift to the right and negative values to the left. $MUX1$ and $MUX2$ are used to control the barrel shifter as an output of up to three shifts. The first stage leads the input signals to the output of the 4:1 mux. D is the comparator output which determines the direction of the activation schema. n is the stages of the barrel shifter. $n-1$ determines previous stage and $n+1$ determines forward stage similarly. The combination of D, $MUX1$, and $MUX2$ determines the gain of the barrel shifter and direction of the barrel shifter output activation schema.

A bi-directional barrel shifter is proposed in [15] where the details can be seen in Fig. 3. This barrel shifter operates by switching a maximum of three transistors at the same clock cycle. 2N number of muxes and N number of D flip-flops are housed in the barrel shifter. The operation is maintained by adjusting the gain which can be adapted by selecting the logic inputs of the muxes. The work in [16] improves the operation of conventional DLDOs by introducing a bi-directional barrel shifter with steady-state load current estimator and a dynamic bi-directional shift register gain scaling control which adjusts the barrel shifter to obtain fast transient time. Steady-state load current estimator senses the load current and adjusts the frequency of the digital controller to get damped behavior of the voltage waveform. Dynamic bi-directional shift register gain scaling control automates the eight different gain according to the predetermined conditions which are studied in [16].

C. Uni-directional shift register

The activation pattern of pass transistors in a conventional DLDO is typically designed to serve bidirectional. This deactivation and activation of the PMOS scheme can be observed in Fig. 4. The one-directional activation pattern can be observed in Fig. 4 (3-a) and (3-b). The M_i represents the PMOS transistors. In the first stage, all PMOS is deactivated. In the second stage, when the digital controller reaches the k stage, the controller determines the output pattern according to $Vout$ value. In Fig. 4 (3-a), the gain is one which leads to activation of one transistor at the right boundary of the activation schema. In Fig. 4 (3-b), the activation of PMOS is at the left boundary of activation schema. Similarly, in Fig. 4 (3-c) and (3-d), the gain is two which activates two PMOS transistors at the same clock cycle. In Fig. 4 (3-e) and (3-f), the gain is three and causes the activation of three PMOS at the same clock cycle within the defined boundaries. This activation pattern should be modified to mitigate the NBTI induced performance degradation. Evenly distributing the electrical stress to all of the transistors can decrease the degradation in the current

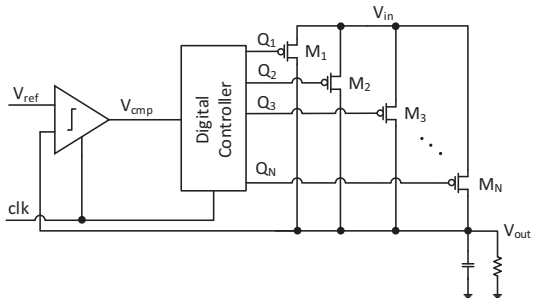


Fig. 1. Schematic of conventional DLDO.

Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	...	...	Q_{N-1}	Q_N
(1) Initialize: all M_is turned off										
1	1	1	1	1	1	1	...	...	1	1
(2) Step k										
0	0	0	0	0	1	1	...	...	1	1
(3-a) Step k+1, if Vcmp is High: Shift right ➡										
0	0	0	0	0	0	1	...	...	1	1
(3-b) Step k+1, if Vcmp is Low: Shift left ⬅										
0	0	0	0	1	1	1	...	...	1	1

Fig. 2. Operation of bi-directional shift register.

supply capacity of PMOS. Under transient loading, a uni-directional DLDO can activate and deactivate the PMOS due to the increased load current.

Previous works do not consider a method to address the reliability and NBTI induced performance degradation for DLDOs with AGS because certain power transistors are heavily overloaded and the rest may not be frequently used. This is the first paper which designs a novel uni-directional barrel shifter with AGS control.

NBTI increases the $|V_{th}|$ leading to slower response times and this increase in the $|V_{th}|$ decreases the load capacity of the DLDO. The increase in $|V_{th}|$ is related to the traps generated in Si/SiO_2 interface at the gate when there is a negative gate voltage [17]. ΔV_{th} formula is given in (1) where C_{ox}, k, T, α, and t are the oxide capacitance, Boltzmann Constant, temperature, the fraction of time, and time respectively. K_{lt} and E_a are the fitting parameters to comply with the experimental data [5].

$$\Delta V_{th} = K_{lt}\sqrt{C_{ox}(|V_{gs}| - |V_{th}|)}e^{-E_a/kT}(\alpha t)^{1/6} \quad (1)$$

In this article, a new NBTI-aware DLDO with uni-directional barrel shifter with AGS is implemented. Therefore, the performance mitigation due to NBTI is maintained low and a good improvement in the transient response time has been achieved.

III. Proposed NBTI-Aware DLDO with AGS

DLDO has a slow transient response under large load current changes. A trade-off exists between steady-state stability, transient response, and performance degradation due to NBTI. A new architecture is designed to reduce the NBTI induced stress and to speed up the transient response.

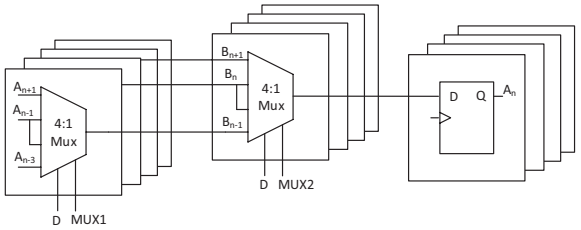


Fig. 3. Schematic of bi-directional barrel shifter.

Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	...	Q_{N-1}	Q_N
(1) Initialize: all M_i turned off										
1	1	1	1	1	1	1	1	...	1	1
(2) Step k										
1	0	0	0	0	1	1	1	...	1	1
(3-a) Step k+1, if Vout < Vref & mux1=L, gain=1 shift ➡										
1	0	0	0	0	0	1	1	...	1	1
(3-b) Step k+1, if Vout > Vref & mux1=L, gain=1 shift ➡										
1	1	0	0	0	1	1	1	...	1	1
(3-c) Step k+1, if Vout < Vref and Vout > Vref - Δ, gain=2 shift ➡										
1	0	0	0	0	0	0	1	...	1	1
(3-d) Step k+1, if Vout > Vref and Vout < Vref + Δ, gain=2 shift ➡										
1	1	1	0	0	1	1	1	...	1	1
(3-e) Step k+1, if Vout < Vref - Δ, gain=3 shift ➡										
1	0	0	0	0	0	0	0	...	1	1
(3-f) Step k+1, if Vout > Vref + Δ, gain=3 shift ➡										
1	1	1	1	0	1	1	1	...	1	1

Fig. 4. Operation of uni-directional barrel shifter with AGS.

Rotating the load stress among the power transistors enables the distribution of the loading evenly and reduces the NBTI induced performance degradation. Furthermore, due to the steady-state gain control, settling time after the overshoots and undershoots are reduced. The transient loading effects are also minimized. As compared to a conventional DLDO, the transient loading response is improved.

A uni-directional DLDO with a barrel shifter is implemented within the proposed AGS. An enhanced AGS control manages all of the power transistors in a way that shortens settling time under severe transient loading and reduced aging for longer operation times have been achieved as compared to a conventional DLDO. The V_{cmp}, $mux1$, and $mux2$ are the control signals generated by the AGS. The details are depicted in Fig. 6.

A. Uni-Directional NBTI-Aware DLDO with Barrel Shifter

The uni-directional barrel shifter is shown in Fig. 5. The schematic and operation of the proposed architecture are shown in Fig. 6 and Fig. 4. The Comparator in adaptive gain scaling control produces the signal of V_{cmp}, $mux1$, and $mux2$ which controls the uni-directional barrel shifter as the steady-state, gain 2 and gain 3 regions are operated. The elementary D flip-flop (DFF) and multiplexer within bi-directional shift register are replaced with T flip-flop and simple logic gates within the proposed uni-directional shift register. A multiplexer and simple logic gates are designed for uni-directional barrel shifter. A multiplexer and logic

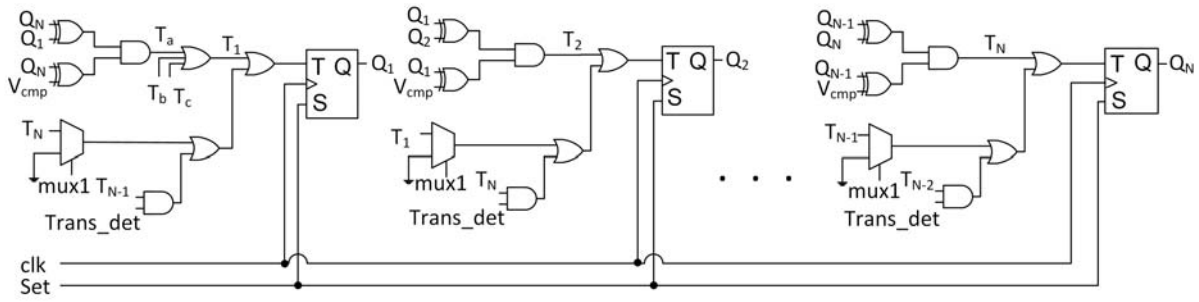


Fig. 5. Proposed uni-directional NBTI-aware DLDO with barrel shifter.

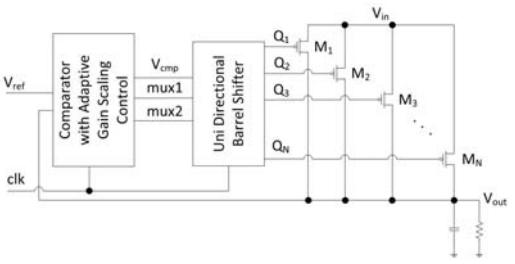


Fig. 6. Proposed DLDO.

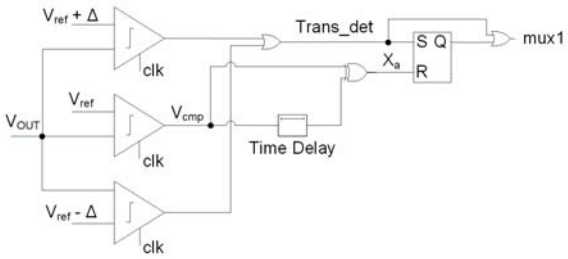


Fig. 7. Three stage adaptive gain scaling with steady state capture.

gates are added to get barrel shifter behavior in the uni-directional controller. This controller is designed to toggle a maximum of three gates at a single clock cycle, and it is the first time implementation of the uni-directional barrel shifter controller. The parallel gates remain unchanged, and uni-directional barrel shifter and AGS are added. The idea is to balance the loading of each power transistors under all load current conditions. The Q_i and Q_{i-1} are gated using XOR gate to equate the output signal switched consequently. V_{cmp} is gated with Q_{i-1} together with other Q_i to determine the logic T_i. Therefore, when V_{cmp} is high (low), inactive (active) power transistors at the right (left) boundary is turned ON (OFF). A uni-directional barrel shift register is realized through this activation/deactivation scheme, as demonstrated in Fig. 4. T_b and T_c are added at the logic to prevent the conflicting situations. $T_b = Q_1 \times Q_2 \times ... \times Q_N \times V_{cmp}$ and $T_c = \overline{Q_1 + Q_2 + ... + Q_N + V_{cmp}}$ [2]. During transient state, three signals V_{cmp}, $mux1$, and $Trans\_det$ are generated to adjust the gain of the barrel shifter where $mux1$ is a steady-state indicator signal that is generated by a novel steady-state detection circuit. After the system enters the steady-state, the system adjusts the gain to one. For barrel shifter, one mux and three additional gates are used in Fig. 7. Area overhead can be determined by counting the additional transistors and compared to the conventional DLDO per control stage. According to the previous definition, there is only a 4.5% area overhead. As the bi-directional shift register consumes a few μW power, the uni-directional shift register power overhear is also negligible [2], [5]. Additional controllers consume low current, thus the power overhead is negligible for the proposed design.

B. Three Stage AGS with Steady-State Detection Circuit

The schematic of a three-stage AGS with steady-state capture is shown in Fig. 7. There are three voltage comparators, two OR gates, one XOR gate, one-time delay, and one SR latch. There are two inputs and two outputs which are V_{ref}, V_{out}, $mux1$, and $Trans\_det$, respectively, for this circuit. Two comparators provide overshoot and undershoot detection. One comparator senses the changes in the V_{out}. Half cycle time delayed V_{cmp} is XORed with V_{cmp} to determine the steady-state operation. AGS senses the changes in V_{cmp} during steady-state operation. The operation of uni-directional barrel shifter starts to control the oscillation at the output of DLDO due to limit cycle oscillation. When V_{cmp} starts to oscillate during the steady-state operation, X_a, the output of XOR gate X_a is high, leading to the reset of SR latch. The X_a signal can be observed in Fig. 8. Thus, the output $mux1$ is low to enter a steady-state region. The variation at the output of DLDO is minimum when the gain is one because the voltage change of one PMOS activation is lower than two or more PMOS activation. If the number of parallel PMOS increases, according to Kirchhoff's voltage law, the drop-out voltage decreased. When the DLDO enters out of the steady-state region, V_{cmp} and time-delayed V_{cmp} are XORed giving logic low at X_a. Following the output of the XOR gate, SR latch's output is high which makes $mux1$ high and the gain scaling circuit operates out of steady-state mode.

The circuit operates in three different modes in three different regions. The first region is the highest gain area in which the circuit operates to provide high in $mux1$ and $Trans\_det$

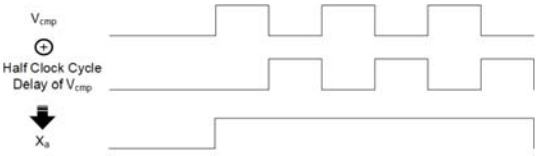


Fig. 8. V_{cmp} and half clock cycle delay of V_{cmp} XORed.

and the gain is three, which means that barrel shifter switches three consecutive power transistors at the rising edge of a single clock cycle. Within the second region, the gain is two such that two power transistors will be turned on/off at the same time. This region is for fast settling of the output voltage. The third region is the gain one region where the steady state voltage variation is achieved at the output by changing the minimum amount of power transistor. For steady state operation $mux1$ and $Trans\_det$ are logic low.

C. Operation of the Proposed NBTI-Aware DLDO with AGS Capability

The NBTI-aware uni-directional controller with AGS capability is shown in Fig. 4. When V_{out} is lower than V_{ref}, the barrel shifter activates the power transistors at the right boundary. Similarly, when V_{out} is higher than V_{ref}, the barrel shifter deactivates the power transistors at the left boundary of the inactive/active power transistor region. Depending on the value of gain, a maximum of three active (inactive) power transistors switch inactive (active) power transistors at the boundary. The uni-directional barrel shifter always toggles the power transistors at the right of the boundary. The switching of the power transistors is always in one direction (right shift). Therefore, the stress on the power transistors evenly distributed because the operation load of each PMOS is distributed equally among each transistor. Furthermore, as compared to conventional DLDO, the steady-state performance does not change and the transient response time is decreased. During the design of the DLDO, being aware of NBTI induced performance degradation is important. The reliability of DLDO can be enhanced by implementing the method in this article. This work improves the performance of AGS with respect to other works in Table I since the AGS has three modes. The first mode is aggressive gain scaling. The second mode is slow settling and the third mode is steady-state mode.

1) Steady-State Operation: In the steady-state mode, the number of active and passive PMOS is changing dynamically. Limit cycle oscillation leads to output voltage ripple at steady-state. The number of active/inactive transistors are the same for both NBTI-aware DLDO with AGS and conventional DLDO but the gain is different while transient state resulting in faster settling time. In Fig. 4 (3-a) and (3-b), the operation of steady-state operation can be observed. The PMOS at the right boundary changes its activity one transistor at each clock cycle.

2) Slow Settling Operation: In the slow settling mode, the barrel shifter gain is two, meaning that PMOS transistors change their activity two transistors at each clock cycle. The operation is quite different from conventional DLDO since the gain of conventional DLDO is one in every loading case. The advantage of this mode is that it reduces the overshooting and undershooting under transient loading. In Fig. 4 (3-c) and (3-d), the slow settling operation can be observed. The PMOS at the boundary changes its activity two transistors at each clock cycle. Depending on V_{out}, the transistors at the left boundary or at the right boundary change their operation from inactive to active.

3) Aggressive Gain Scaling: In the aggressive gain scaling mode, the barrel shifter gain is three. The advantage of this operation is that it reduces the settling time significantly. Under transient loading, the load current changes significantly. In Fig. 4 (3-e) and (3-f), the operation of aggressive gain scaling can be observed. The active PMOSs (shaded region) change their operation to inactive depending on the V_{out}. The consecutive three transistors change their operation in the same clock cycle.

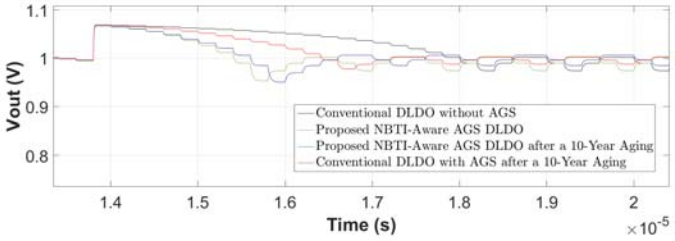
IV. Evaluation of the Proposed Circuit

In order to validate the effectiveness of the 1.1 V to 1.0 V DLDO, this on-chip circuit is designed in a 32 nm standard CMOS process. The proposed DLDO can supply a maximum of 124 mA current. The transient output voltage waveform from 20 mA to 60 mA step load change and comparison of the results of the conventional DLDO without AGS, the proposed NBTI-aware DLDO with AGS, the proposed NBTI-aware DLDO with AGS after 10-year aging and the conventional DLDO with AGS after 10-year aging are shown in Fig. 9. 1 MHz clock frequency is applied and aging induced degradation is evaluated under $100°C$. The settling time after load decrease is 4.5 μs and the settling time after load increase is 4.2 μs for the conventional DLDO without AGS. The proposed NBTI-aware AGS DLDO has 2.4 μs settling time after an overshoot and 1.7 μs settling time after an undershoot. The proposed NBTI-aware DLDO with AGS after 10-year aging has 2.8 μs settling time after an overshoot and 2.1 μs settling time after an undershoot. The conventional DLDO with AGS after a 10-year aging has 3.4 μs settling time after overshoot and 2.8 μs settling time after undershoot. The results for conventional DLDO with AGS without aging is the same as the results of proposed NBTI-aware DLDO with AGS. There is 46.7% decrease in the settling time of overshoot of the proposed DLDO with AGS as compared to the conventional DLDO. There is also a 59.5% decrease in the settling time of undershooting of the proposed DLDO with AGS as compared to the conventional DLDO. Furthermore, the settling time for the proposed DLDO with AGS after 10-year aging is decreased by 59.5% as compared to the conventional DLDO with AGS after 10-year aging.

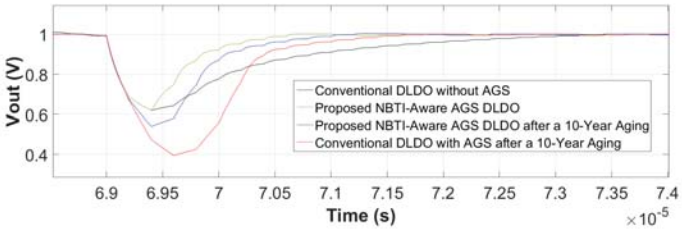
Previous works are compared with this work in Table I. The power overhead in [12] is negligible since added decoders have little power consumption with respect to power PMOS. Similarly, the power overhead in [13] and [2] is negligible because the modifications add negligible power consumption. The works in [12] and [13] have AGS capability.

TABLE I
COMPARISON WITH PREVIOUS AGING-AWARE ON-CHIP DLDOS

	[12]	[13]	[2]	This work
Year	2015	2017	2018	2019
Broad load range	Yes	Yes	Yes	Yes
Additional controller	Yes	Yes	No	No
Added overhead	Multiple decoders	Decoder	Modification of original controller	Modification of conventional DLDO
Topology	Row rotation scheme	Code roaming algorithm	Uni-directional shift controller	Uni-directional shift controller with barrel shifter
Adaptive gain scaling capability	Yes	Yes	No	Yes



(a) Comparison of overshoot.



(b) Comparison of undershoot.

Fig. 9. Comparison of transient loading among aging-aware and aging-unaware DLDOs.

V. CONCLUSION

In this paper, an NBTI-aware DLDO with the AGS control is proposed to diminish the aging effect and to reduce the settling time. The settling time is reduced by 46.7% and 59.5% for overshoot and undershoot without aging aware design, respectively. The proposed circuit is NBTI-aware, thus, performance degradations due to NBTI are reduced. A novel uni-directional shift register with barrel shifter is proposed to distribute the electrical stress among the power transistors evenly. The proposed NBTI-aware DLDO with AGS control is efficient because the settling time is reduced by 33% after 10-year aging.

ACKNOWLEDGMENT

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