Selçuk Köse
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Research Interests

- **Research interests:** VLSI; Interconnect design methodologies; On-chip clocking and power delivery; Power management; Hardware security

Work Experience

- **University of Rochester** Rochester, NY
  Associate Professor, Electrical and Computer Engineering Department *January 2019 - Current*
- **University of South Florida** Tampa, FL
  Associate Professor, Electrical Engineering Department *August 2018 - January 2019*
- **University of South Florida** Tampa, FL
  Assistant Professor, Electrical Engineering Department *August 2012 - August 2018*
- **University of Rochester** Rochester, NY
  Research Assistant, High Performance Integrated Circuit Design Laboratory *September 2007 - June 2012*
- **Freescale Semiconductor** Tempe, AZ
  Graduate Intern, Microwave and Mixed-Signal Laboratory *May 2010 - August 2010*
- **Eastman Kodak Company** Rochester, NY
  Graduate Intern, CMOS Image Sensors R&D Laboratory *May 2009 - June 2009*
- **Intel Corporation** Santa Clara, CA
  Graduate Intern, Central Technology and Special Circuits Team *Summers of 2007 and 2008*

Education

- **University of Rochester** Rochester, NY
  Doctor of Philosophy in Electrical and Computer Engineering *March 2008 - June 2012*
- **University of Rochester** Rochester, NY
  Master of Science in Electrical and Computer Engineering *September 2006 - March 2008*
- **Bilkent University** Ankara, Turkey
  Bachelor of Science in Electrical and Electronics Engineering *September 2001 - May 2006*

Awards

- USF Faculty Outstanding Research Achievement Award, 2017
  – The most prestigious award for research achievements at USF. Only 17 researchers (out of over 1700 faculty members) received this prestigious university-wide award in 2017
- USF Outstanding Faculty Award, 2016
  – Only 10 researchers (out of over 1700 faculty members) received this prestigious university-wide award in 2016
- Cisco Research Award, 2015, 2016 & 2017
- National Science Foundation CAREER Award, 2014
  – National Science Foundation's most prestigious award in support of junior faculty who exemplify the role of teacher-scholars through outstanding research, excellent education and the integration of education and research within the context of the mission of their organizations
- USF College of Engineering Outstanding Junior Research Achievement Award, 2014
  – Only one assistant professor received this prestigious award in 2014

- Turkiye Is Bankasi *Golden Youth Award* for outstanding success in University Entrance Exam
  - **12**th over 1.5 million candidates, Turkey, 2001
- Full scholarship and stipend awarded by Bilkent University, Ankara, Turkey, 2001-2006
- Awarded with Abroad Undergraduate Education Fellowship by Turkish Government, Turkey, 2001

Sponsored Research

- **SRC extension of the STARSS award (sole PI)** — $40,000
  SaTC: STARSS: Small: Combined Side-channel Attacks and Mathematical Foundations of Combined Countermeasures — *2020 - 2021*
- **NSF/SRC joint SaTC/STARSS award (sole PI)** — $370,000
  SaTC: STARSS: Small: Combined Side-channel Attacks and Mathematical Foundations of Combined Countermeasures — *2017 - 2020*
- **Cisco Research Award (PI: Kose & Co-PI: Chen)** — $80,000*
  Reconfigurable Voltage Regulation for Security and Efficiency — *2017 - 2018*
  *Cisco also covers the fabrication cost of a test chip at 28 nm FDSOI technology.
- **I4 Corridor Matching Grant (sole PI)** — $50,000
  On-Chip Voltage Regulation in an Advanced Technology — *2016 - 2017*
- **Cisco Research Award (PI: Kose & Co-PI: Chen)** — $80,000**
  On-Chip Voltage Regulation in an Advanced Technology — *2016 - 2017*
  **Cisco also covers the fabrication cost of a test chip at 28 nm FDSOI technology.
- **Florida Center for Cybersecurity (FC^2) Seed Grant (PI: Kose & Co-PI: DeMara)** — $50,000
  Trusted IoT using Cross-layer Leveraging of Reconfigurable Device Signatures — *2016 - 2017*
- **Cisco Research Award (sole PI)** — $30,000
  On-Chip Voltage Regulation in an Advanced FDSOI Process — *2015 - 2016*
- **Florida Center for Cybersecurity (FC^2) Seed Grant (PI: Kose & Co-PI: DeMara)** — $50,000
  Aging-Aware Hardware-Trojan Detection at Runtime — *2015 - 2016*
- **National Science Foundation CAREER award (sole PI)** — $450,000
  CAREER: Regulator-Gating (ReGa): A New On-Chip Power Delivery Architecture — *2014 - 2019*

Publications

Books

B1. I. Vaisband, R. Jakushokas, M. Popovich, A. V. Mezhiba, **S. Köse**, and E. G. Friedman, *On-Chip Power Delivery and Management, Fourth Edition*, Springer, 2016, ISBN # 978-3319293936.

B2. R. Jakushokas, M. Popovich, A. V. Mezhiba, **S. Köse**, and E. G. Friedman, *Power Distribution Networks with On-Chip Decoupling Capacitors, Second Edition*, Springer, 2011, ISBN # 978-1-4419-7870-7.

– Chinese translation by China Machine Press, 2014, Chinese ISBN # 978-7-111-44929-4

Book chapters

B1. L. Wang, S. Seckiner, and **S. Köse**, *Reliability Enhanced Digital Low-Dropout Regulator with Improved Transient Performance*, in Metzler C., Gaillardon PE., De Micheli G., Silva-Cardenas C., Reis R. (eds) VLSI-SoC: New Technology Enabler. VLSI-SoC 2019. IFIP Advances in Information and Communication Technology, Springer 2020, ISBN # 978-3-030-53273-4.

Journals

J1. F. Amsaad and **S. Köse**, "A Secure Hardware-Assisted AMI Authentication Scheme for Smart Cities," *IEEE Consumer Electronics Magazine*, (accepted).

J2. B. Peköz, M. Hafez, **S. Köse** and H. Arslan, "Reducing Precoder/Channel Mismatch and Enhancing Secrecy in Practical MIMO Systems Using Artificial Signals," *IEEE Communications Letters*, Vol. 24, No. 6, pp. 1347 – 1350, June 2020.

J3. B. Peköz, **S. Köse** and H. Arslan, "Extensionless Adaptive Transmitter and Receiver Windowing of Beyond 5G Frames," *IEEE Transactions on Vehicular Technology*, Vol. 69, No. 2, pp. 1888 – 1902, February 2020.

J4. B. Peköz, Z. E. Ankaralı, **S. Köse** and H. Arslan, "Non-Redundant OFDM Receiver Windowing for 5G Frames and Beyond," *IEEE Transactions on Vehicular Technology*, Vol. 69, No. 1, pp. 676 – 684, January 2020.

J5. R. Kuttappa, **S. Köse** and B. Taskin, "FOPAC: Flexible On-Chip Power and Clock," *EEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 66, No. 12, pp. 4628 – 4636, December 2019.

J6. A. F. Demir, B. Peköz, **S. Köse** and H. Arslan,, "Innovative Telecommunications Training through Flexible Radio Platforms," *EEE Communications Magazine*, Vol. 57, No. 11, pp. 27 – 33, November 2019.

J7. L. Wang, S. K. Khatamifard, U. R. Karpuzcu, and **S. Köse** , " Exploring On-Chip Power Delivery Network Induced Analog Covert Channels," *IEEE TC on Cyber-Physical Systems Newsletter*, Vol. 4, No. 1, pp. 15 – 18, February 2019.

J8. L. Wang, S. K. Khatamifard, U. R. Karpuzcu, and **S. Köse** , "Exploiting Algorithmic Noise Tolerance for Scalable On-Chip Voltage Regulation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 27, No. 1, pp. 229 – 242, January 2019.

J9. S. K. Khatamifard, L. Wang, **S. Köse**, and U. R. Karpuzcu, "A New Class of Covert Channels Exploiting Power Management Vulnerabilities," *IEEE Computer Architecture Letters (CAL)*, Vol. 17, No. 2, pp. 201 – 204, July-December 2018.

J10. W. Yu, Y. Chen, **S. Köse**, and J. Chen, "Exploiting Multi-Phase On-Chip Voltage Regulators as Strong PUF Primitives for Securing IoT," *Journal of Electronic Testing*, Vol. 34, No. 5, pp. 587 – 598, October 2018.

J11. M. Azhar, F. Amsaad, and **S. Köse**, "Duty Cycle-based Controlled Physical Unclonable Function," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 26, No. 9, pp. 1647 – 1658, September 2018.

J12. F. Amsaad, M. Niamat, A. Dawoud, and **S. Köse**, "Reliable Delay based Algorithm to Boost PUF Security against Modeling Attacks," *Information*, Vol. 9, No. 9, pp. 1 – 15, September 2018.

J13. W. Yu and **S. Köse**, "Exploiting Voltage Regulators to Enhance Various Power Attack Countermeasures," *IEEE Transactions on Emerging Topics in Computing*, Vol. 6, No. 2, pp. 244 – 257, April-June 2018.

J14. S. A. Sadat, M. Canbolat, and **S. Köse**, "Optimal Allocation of LDOs and Decoupling Capacitors within a Distributed On-Chip Power Grid," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol 23, No. 4, pp. 49:1 – 49:15, May 2018.

J15. M. H. Yilmaz, E. Guvenkaya, H. M. Furqan, **S. Köse**, and H. Arslan , "Cognitive Security of Wireless Communication Systems in the Physical Layer," *Wireless Communications and Mobile Computing*, Vol. 2017, pp. 1 – 9, December 2017.

J16. M. H. Yilmaz, **S. Köse**, N. Chamok, M. Ali, and H. Arslan , "Partially Overlapping Filtered Multitone with Reconfigurable Antennas in Uncoordinated Networks," *Physical Communication*, Vol. 25, No. 1, pp. 249 – 258, December 2017.

J17. W. Yu and **S. Köse**, "False Key-Controlled Aggressive Voltage Scaling: A Countermeasure Against LPA Attacks," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 36, No. 12, pp. 2149 – 2153, December 2017.

J18. L. Wang, S. K. Khatamifard, O. A. Uzun, U. R. Karpuzcu, and **S. Köse** , "Efficiency, Stability, and Reliability Implications of Unbalanced Current Sharing among Distributed On-Chip Voltage Regulators," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 25, No. 11, pp. 3019 – 3032, November 2017 .

J19. W. Yu and **S. Köse**, "A Lightweight Masked AES Implementation for Securing IoT Against CPA Attacks," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 64, No. 11, pp. 2934 – 2944, November 2017.

J20. W. Yu and **S. Köse**, "Security-Adaptive Voltage Conversion as a Lightweight Countermeasure Against LPA Attacks," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 25, No. 7, pp. 2183 - 2187, July 2017.

J21. W. Yu and **S. Köse**, "A Voltage Regulator-Assisted Lightweight AES Implementation Against DPA Attacks," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 63, No. 8, pp. 1152 - 1163, August 2016.

J22. W. Yu and **S. Köse**, "Charge-Withheld Converter-Reshuffling (CoRe): A Countermeasure Against Power Analysis Attacks," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 63, No. 5, pp. 438 - 442, May 2016.

J23. W. Yu and **S. Köse**, "Security Implications of Simultaneous Dynamic and Leakage Power Analysis Attacks on Nanoscale Cryptographic Circuits," *IET Electronics Letters*, Vol. 52, Issue 6, pp. 466 - 468, March 2016.

– Featured as the *Interview* article of the March issue of the IET Electronics Letters.

J24. W. Yu and **S. Köse**, "Time-Delayed Converter-Reshuffling: An Efficient and Secure Power Delivery Architecture," *IEEE Embedded Systems Letters*, Vol. 7, No. 3, pp. 73 - 76, September 2015.

J25. I. Vaisband,B. Price, **S. Köse**, Y. Kolla, E. G. Friedman, and J. Fischer, "Distributed Power Delivery with 28 nm Ultra-Small LDO Regulator," *Analog Integrated Circuits and Signal Processing*, Vol. 83, Issue 3, pp. 295 - 309, March 2015.

J26. I. Vaisband, M. Azhar, E. G. Friedman and **S. Köse**, "Digitally Controlled Pulse Width Modulator for On-Chip Power Management," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 22, No. 12, pp. 2527 - 2534, December 2014.

J27. O. Uzun and **S. Köse**, "Converter-Gating: A Power Efficient and Secure On-Chip Power Delivery System," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol. 4, No. 2, pp. 169 - 179, June 2014.

J28. **S. Köse**, S. Tam, S. Pinzon, B. McDermott, and E. G. Friedman, "Active Filter Based Hybrid On-Chip DC-DC Converters for Point-of-Load Voltage Regulation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 21, No. 4, pp. 680 - 691, April 2013.

J29. I. Savidis, **S. Köse**, and E. G. Friedman, "Power Noise in TSV-Based 3-D Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 48, No. 2, pp. 587 - 597, February 2013.

J30. **S. Köse** and E. G. Friedman, "Distributed On-Chip Power Delivery," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol. 4, No. 4, pp. 704 - 713, December 2012.

J31. **S. Köse** and E. G. Friedman, "Efficient Algorithms for Fast IR Drop Analysis Exploiting Locality," *Integration, the VLSI Journal*, Vol. 45, No. 2, pp. 149 - 161, March 2012.

J32. **S. Köse** and E. G. Friedman, "Effective Resistance of a Two Layer Mesh," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 58, No. 11, pp. 739 - 743, November 2011.

J33. **S. Köse**, E. Salman, and E. G. Friedman, "Shielding Methodologies in the Presence of Power/Ground Noise," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 19, No. 8, pp. 1458 - 1468, August 2011.

Conferences

C1. L. Wang and **S. Köse**, "Approximate Voltage Regulation for Energy Efficient Error Tolerable Applications," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2020.

C2. A. Khanna, E. Elmitwalli, S. Dutta, S. Deng, S. Datta, **S. Köse**, and K. Ni, "A Bias and Correlation Free True Random Number Generator Based on Quantized Oscillator Phase under Sub-Harmonic Injection Locking," *IEEE Symposia on VLSI Technology and Circuits*, June 2020.

C3. F. Amsaad and **S. Köse**, "A Trusted Authentication Scheme for IoT-Based Smart Grid Applications," *IEEE World Forum of Internet of Things (WF-IoT)*, April 2020.

C4. L. Wang and **S. Köse**, "Startup Aware Reliability Enhancement Controller for On-Chip Digital LDOs," *Government Microcircuit Applications and Critical Technology Conference*, March 2020.

C5. S. Seçkiner, L. Wang and **S. Köse**, "An NBTI-Aware Digital Low-Dropout Regulator with Adaptive Gain Scaling Control," *Proceedings of the IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, October 2019.

C6. L. Wang, R. Kuttappa, B. Taskin, and **S. Köse**, "Distributed Digital Low-Dropout Regulators with Phase Interleaving for On-Chip Voltage Noise Mitigation," *Proceedings of the ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP)*, June 2019.

C7. M. A. Vosoughi, L. Wang, and **S. Köse**, "Bus-Invert Coding as a Low-Power Countermeasure Against Correlation Power Analysis Attack," *Proceedings of the ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP)*, June 2019.

C8. M. A. Vosoughi and **S. Köse**, "Combined Distinguishers to Enhance the Accuracy and Success of Side Channel Analysis," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2019.

C9. M. A. Vosoughi and **S. Köse**, "Leveraging On-Chip Voltage Regulators Against Fault Injection Attacks," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI)*, May 2019.

C10. L. Wang and **S. Köse**, "Reliability Enhanced On-Chip Digital LDO with Limit Cycle Oscillation Mitigation," *Government Microcircuit Applications and Critical Technology Conference*, March 2019.

C11. S. K. Khatamifard, L. Wang, A. Das, **S. Köse**, and U. R. Karpuzcu, "POWERT Channels: A Novel Class of Covert Communication Exploiting Power Management Vulnerabilities," *Proceedings of the IEEE International Symposium on High Performance Computer Architecture (HPCA)*, February 2019.

C12. L. Wang and **S. Köse**, "When Hardware Security Moves to the Edge and Fog," *Proceedings of the IEEE International Conference on Digital Signal Processing (DSP'18)*, November 2018.

C13. M. Azhar and **S. Köse**, "Process, Voltage, and Temperature-stable Adaptive Duty Cycle based PUF," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018.

C14. L. Wang and **S. Köse**, "Reliable On-Chip Voltage Regulation for Sustainable and Compact IoT and Heterogeneous Computing Systems," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI)*, May 2018.

C15. L. Wang, S. K. Khatamifard, U. R. Karpuzcu, and **S. Köse**, "Mitigation of NBTI Induced Performance Degradation in On-Chip Digital LDOs," *Proceedings of the IEEE Design, Automation and Test in Europe Conference and Exhibition (DATE)*, pp. 803 - 808, March 2018.

C16. A. W. Khan, T. Wanchoo, G. Mumcu, and **S. Köse**, "Implications of Distributed On-Chip Power Delivery on EM Side-Channel Attacks," *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, November 2017.

C17. B. Pekoz, **S. Köse**, and H. Arslan, "Adaptive Windowing of Insufficient CP for Joint Minimization of ISI and ACI Beyond 5G," *Proceedings of the IEEE Annual International Symposium on Personal, Indoor, and Mobile Radio Communications (PIMRC)*, October 2017.

C18. A. Roohi, R. Demara, L. Wang, and **S. Köse**, "Secure Intermittent-Robust Computation for Energy Harvesting Device Security and Outage Resilience," *Proceedings of the IEEE Conference on Advanced and Trusted Computing (ATC)*, August 2017.

C19. S. K. Khatamifard, L. Wang, W. Yu, **S. Köse**, and U. R. Karpuzcu, "ThermoGater: Thermally-Aware On-Chip Voltage Regulation," *Proceedings of the IEEE International Symposium on Computer Architecture (ISCA)*, pp. 120 - 132, June 2017.

C20. W. Yu and **S. Köse**, "A Lightweight AES Implementation Against Bivariate First-Order DPA Attacks," *Proceedings of the ACM Hardware and Architectural Support for Security and Privacy (HASP)*, pp. 1 - 7, June 2017.

C21. **S. Köse**, "Efficient and Secure On-Chip Reconfigurable Voltage Regulation for IoT Devices," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 369 - 374, May 2017.

C22. V. T. Alaparthy and **S. Köse**, "An Adaptive Senior Design Course with an Emphasis on Undergraduate Course Curriculum," *Proceedings of the IEEE International Conference on Microelectronics System Education*, pp. 59 - 62, May 2017.

C23. W. Yu and **S. Köse**, "Implications of Noise Insertion Mechanisms of Different Countermeasures Against Side-Channel Attacks," *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2017.

C24. **S. Köse**, L. Wang, and R. F. DeMara, "On-Chip Sensor Circle Distribution Technique for Real-Time Hardware Trojan Detection," *Government Microcircuit Applications and Critical Technology Conference (GOMACHTech)*, March 2017.

C25. W. Yu, O. A. Uzun, and **S. Köse**, "Leveraging On-Chip Voltage Regulators as a Countermeasure Against Side-Channel Attacks," *Proceedings of the IEEE/ACM Design Automation Conference (DAC)*, pp. 1 - 6, June 2015.

C26. M. E. Belviranli, W. Yu, and **S. Köse**, "Ultra-Fine Grain Power Management at Datapath-Level: Fact or Fiction," *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS) WACI Session*, March 2015.

C27. O. Uzun and **S. Köse**, "Regulator-Gating Methodology With Distributed Switched Capacitor Voltage Converters," *Proceedings of the IEEE Computer Society Annual Symposium on VLSI*, pp. 13 - 18, July 2014.

C28. **S. Köse**, "Thermal Implications of On-Chip Voltage Regulation: Upcoming Challenges and Possible Solutions," *Proceedings of the IEEE/ACM Design Automation Conference (DAC)*, pp. 1 - 6, June 2014.

C29. M. Azhar and **S. Köse**, "An Enhanced Pulse Width Modulator with Adaptive Duty Cycle and Frequency Control," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 958 - 961, June 2014.

C30. **S. Köse**, "Regulator-Gating: Adaptive Management of On-Chip Voltage Regulators," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 105 - 110, May 2014.

C31. **S. Köse**, I. Vaisband, and E. G. Friedman, "Digitally Controlled Wide Range Pulse Width Modulator for on-Chip Power Supplies," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2251 - 2254, May 2013.

C32. **S. Köse**, R. M. Secareanu, O. Hartin, and E. G. Friedman, "Current Profile of a Microcontroller to Determine Electromagnetic Emissions" *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2650 - 2653, May 2013.

C33. **S. Köse** and E. G. Friedman, "Distributed Power Delivery for Energy Efficient and Low Power Systems," *Asilomar Conference on Signals, Systems, and Computers*, November 2012, **(invited paper)**.

C34. **S. Köse** and E. G. Friedman, "Design Methodology to Distribute On-Chip Power in Next Generation Integrated Circuits," *IEEE 27-th Convention of Electrical and Electronics Engineers in Israel*, November 2012, **(invited paper)**.

C35. **S. Köse** and E. G. Friedman, "Power Delivery in Heterogeneous Integrated Circuits," *IEEE CAS-FEST Workshop (in conjunction with ISCAS2012)*, May 2012, **(invited talk)**.

C36. **S. Köse**, S. Tam, S. Pinzon, B. McDermott, and E. G. Friedman, "An Area Efficient On-Chip Hybrid Voltage Regulator," *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, pp. 398 - 403, March 2012.

C37. **S. Köse** and E. G. Friedman, "Fast Algorithms for IR Voltage Drop Analysis Exploiting Locality," *Proceedings of the IEEE/ACM Design Automation Conference (DAC)*, pp. 996 - 1001, June 2011.

C38. **S. Köse** and E. G. Friedman, "Distributed Power Network Co-Design with On-Chip Power Supplies and Decoupling Capacitors," *Proceedings of the ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP)*, June 2011.

C39. I. Savidis, **S. Köse**, and E. G. Friedman, "Power Grid Noise in TSV-Based 3-D Integrated Systems," *Government Microcircuit Applications and Critical Technology Conference (GOMACHTech)*, pp. 129 - 132, March 2011.

C40. **S. Köse** and E. G. Friedman, "Simultaneous Co-Design of Distributed On-Chip Power Supplies and Decoupling Capacitors," *Proceedings of the IEEE International SoC Conference*, pp. 15 - 18, September 2010.

C41. **S. Köse** and E. G. Friedman, "An Area Efficient Fully Monolithic Hybrid Voltage Regulator" *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2718 - 2721, May/June 2010.

C42. **S. Köse** and E. G. Friedman, "Fast Algorithms for Power Grid Analysis Based on Effective Resistance," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 3661 - 3664, May/June 2010.

C43. **S. Köse** and E. G. Friedman, "On-Chip Point-of-Load Voltage Regulator for Distributed Power Supplies," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 377 - 380, May 2010.

C44. **S. Köse**, E. Salman, and E. G. Friedman, "Shielding Methodologies in the Presence of Power/Ground Noise," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2277 - 2280, May 2009.

C45. **S. Köse**, E. Salman, Z. Ignjatovic, and E. G. Friedman, "Pseudo-Random Clocking to Enhance Signal Integrity," *Proceedings of the IEEE International SoC Conference*, pp. 47 - 50, September 2008.

Workshop Presentations

W1. I. Vaisband, **S. Köse**, I. Savidis, and E. G. Friedman, "On-Chip Power Delivery," University Technology Showcase, Rochester, New York, April 6, 2011.

Patents

P1. **S. Köse**, L. Wang, S. K. Khatamifard, and U. R. Karpuzcu, "Reduced Clock Pulse Width Digital Low-dropout Regulator," Provisional Patent Application No. 18B158PR, September 11, 2018.

P2. **S. Köse** and W. Yu, "False Key-controlled Aggressive Voltage Scaling," Non-Provisional Patent Application No. 15/967,171, April 30, 2018.

P3. B. Pekoz, H. Arslan, and **S. Köse**, "Enhancing Performance of Beyond 5G Networks through Adaptive Windowing and CP Alignment," Non-Provisional Patent Application, December 22, 2017.

P4. B. Pekoz, **S. Köse**, and H. Arslan, "Adaptive Utilization of Insufficient Cyclic Prefix (CP) for Joint Minimization of Intersymbol Interference (ISI) and Adjacent Channel Interference (ACI)," Non-Provisional Patent Application, October 6, 2017.

P5. **S. Köse** and W. Yu, "System and Method for Switched-Capacitor based Side-channel Countermeasures," US Patent 10,691,836, June 23, 2020.

P6. **S. Köse** and W. Yu, "Security-adaptive Voltage Conversion as a Lightweight Countermeasure against LPA Attacks," US Patent 10,680,797, June 9, 2020.

P7. B. Pekoz, M. Hafez, **S. Köse**, and H. Arslan, "Using artificial signals to maximize capacity and secrecy of multiple-input multiple-output (MIMO) communication," Us Patent 10,644,711, May 5, 2020.

P8. B. Pekoz, Z. E. Ankarali, **S. Köse**, and H. Arslan, "OFDM reception under high adjacent channel interference while preserving frame structure," US Patent 10,547,489, January 28, 2020.

P9. B. Pekoz, M. Hafez, **S. Köse**, and H. Arslan, "Using artificial signals to maximize capacity and secrecy of multiple-input multiple-output (MIMO) communication," Us Patent 10,516,452, December 24, 2019.

P10. B. Pekoz, **S. Köse**, and H. Arslan, "Network-Aware Adjacent Channel Interference Rejection and Out of Band Emission Suppression," US Patent 10,511,338, December 17, 2019.

P11. B. Pekoz, **S. Köse**, and H. Arslan, "Combined Minimization of Intersymbol Interference (ISI) and Adjacent Channel Interference (ACI)," US Patent 10,476,705, November 12, 2019.

P12. B. Pekoz, **S. Köse**, and H. Arslan, "Combined Minimization of Intersymbol Interference (ISI) and Adjacent Channel Interference (ACI)," US Patent 10,348,530, July 9, 2019.

P13. **S. Köse** and O. A. Uzun, "Secure Converter-Gating, Reconfiguration, and Regulation," US Patent 9,812,954, November 7, 2017.

P14. **S. Köse**, O. A. Uzun, and W. Yu, "Time Delayed Converter Reshuffling," US Patent 9,748,837, August 29, 2017.

P15. **S. Köse** and O. A. Uzun, "System and Method for Distributed Voltage Regulator-Gating," US Patent 9,372,490, June 21, 2016.

P16. **S. Köse** and E. G. Friedman, "A Digitally Controlled Wide Range Pulse Width Modulator," US Patent 9,007,140, April 14, 2015.

P17. **S. Köse** and O. A. Uzun, "System and Method for Voltage Regulator-Gating," US Patent 8,922,272, December 30, 2014.

Invited Talks

- False Key-Controlled Aggressive Voltage Scaling: A Countermeasure Against LPA Attacks, Defense TechConnect Fall Summit and Expo, Tampa, Florida, October 2018.
- Secure and Efficient Design Techniques for Modern Integrated Systems, Bilkent University, Ankara, Turkey, October 2018 (Graduate seminar).
- Secure and Efficient Design Techniques for Modern Integrated Systems, Bogazici University, Istanbul, Turkey, October 2018 (Graduate seminar).
- Secure and Efficient Design Techniques for Modern Integrated Systems, University of New South Wales, Sydney, New South Wales, Australia, April 2018.
- Secure and Efficient Design Techniques for Modern Integrated Systems, University of Massachusetts, Amherst, Amherst, Massachusetts, March 2018.
- Secure and Efficient Design Techniques for Modern Integrated Systems, University of Arizona, Tucson, Arizona, March 2018.
- Secure and Efficient Design Techniques for Modern Integrated Systems, University of Rochester, Rochester, New York, March 2018.
- Secure and Efficient Design Techniques for Modern Integrated Systems, University of Utah, Salt Lake City, Utah, March 2018.
- Security Implications of Reconfigurable Voltage Regulators, Cybersecurity Research Symposium, Tampa, Florida, April 2017.
- Efficient and Secure On-Chip Power Delivery, Cisco Systems, San Jose, California, December 2016.
  – Invited speaker at the Cisco PI Summit
- Efficient and Secure On-Chip Power Delivery, Cukurova University, Adana, Turkey, July 2016.
- Efficient and Secure On-Chip Power Delivery, Istanbul Technical University, Istanbul, Turkey, June 2016.
- Ultra-Fine Grain Power Management at Datapath-Level: Fact or Fiction, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS) WACI Session, Istanbul, Turkey, March 2015.
- Efficient and Secure On-Chip Power Delivery, IEEE Student Branch, University of South Florida, Tampa, Florida, March 2015.
- Design of Efficient and Trustworthy On-Chip Power Delivery Systems, Workshop on Energy-Secure System Architectures (ESSA) (In Conjunction with ISCA'14), Minneapolis, Minnesota, June 2014.
- Converter-Gating: An Efficient On-Chip Power Delivery Architecture, Intel Corporation, Santa Clara, California, June 2014.

- Converter-Gating: An Efficient On-Chip Power Delivery Architecture, Synaptics Austin Design Center, Austin, Texas, May 2014.
- Distributed On-Chip Power Delivery – On-going Research and New Directions, IBM T. J. Watson Research Center, Yorktown Heights, New York, April 2013.
- Distributed Power Delivery for Energy Efficieny and Low Power Systems, Asilomar Conference on Signals, Systems, and Computers, Monterey, California, November 2012.
- High Performance Power Delivery for Nanoscale Integrated Circuits, University of South Florida, Tampa, Florida, February 2012.
- EMMA: A Methodology to Model Current Activity of a Digital Block to Determine Emission Level for a Broad Frequency Range, *RF, Analog, and Sensor Group*, Freescale Semiconductor, Tempe, Arizona, August 2010.
- Simultaneous Co-Design of Clock and Power Distribution Networks, *Central Technology and Special Circuits Team*, Intel Corporation, Santa Clara, California, March 2009.
- Un-Core Clock Distribution of Nehalem-Ex Processor and the De-Skew Machine Operation Principles, *Central Technology and Special Circuits Team*, Intel Corporation, Santa Clara, California, August 2007.

Teaching

- **Instructor** — University of Rochester
  - Digital Logic (ECE112) — Spring 2019, 80+ students

  University of South Florida
  - Emerging Topics in Performance and Security of Modern Integrated Systems — Spring 2017, 6 students
  - Design II (Senior Design Project) — Fall 2016, 40 students
  - Design II (Senior Design Project) — Spring 2016, 45 students
  - Design II (Senior Design Project) — Fall 2015, 40 students
  - Design II (Senior Design Project) — Spring 2015, 45 students
  - Design II (Senior Design Project) — Fall 2014, 40 students
  - Design II (Senior Design Project) — Spring 2014, 54 students
  - High Performance Integrated Circuit Design — Fall 2013, 8 students
  - Introduction to Electrical Systems I (EGN 3373) — Fall 2012, 120+ students
- **Co-Lecturer** — University of Rochester
  - Performance Issues in IC/VLSI Design and Analysis — Fall 2011, 10+ students
- **Teaching Assistant** — University of Rochester
  - VLSI Design Methodologies — Fall 2009, 10+ students
  - Circuits and Signals — Fall 2006, 30+ students
  - Introduction to Signals and Circuits — Spring 2007, 35+ students
- **Teaching Assistant** — Bilkent University, Ankara
  - Analog Electronics — Fall 2004, Fall 2005, 100+ students
  - Microprocessors — Spring 2005, Spring 2006, 100+ students

Graduated Students

- **Berker Pekoz**, PhD, first job Qualcomm — 2020
- **Longfei Wang**, PhD, first job Postdoctoral Researcher at University of Rochester — 2018
- **Mahmood Azhar**, PhD, first job Lead Instructor at South Florida State College — 2018
- **Weize Yu**, PhD, first job Assistant Professor at Old Dominion University — 2017
- **Orhun Aras Uzun**, PhD, first job at Synaptics Corporation — 2017

- **Ahmed Waheed Khan**, MSc, first job at Flex Electronics 2018
- **Tanya Wanchoo**, MSc, first job at Intel Corporation 2016

Current Graduate Students

- **Yerzhan Mustafa**, PhD student Spring 2021 - present
- **Eslam Elmitwalli**, PhD student Fall 2019 - present
- **Haotian Dai**, PhD student Fall 2019- present
- **Soner Seckiner**, PhD student Fall 2018- present

Student Awards

- **Longfei Wang** Cash Prize
  Chih Foundation Research and Publication Award *2018*
- **Longfei Wang** Stipend+Tuition
  University of South Florida Graduate Fellowship *2015 - 2016*
- **Weize Yu** Stipend+Tuition+Travel
  University of South Florida Presidential Doctoral Fellowship *2014 - 2019*

Professional Activities

- Associate editor
  Springer Nature - Computer Science, 2019 – present
  Microelectronics Journal, 2014 – present
  Journal of Circuits, Systems, and Computers (JCSC), 2012 – present
- Committee member
  IEEE VLSI System Application Technical Committee, 2017 – present
- General chair
  ACM/IEEE System Level Interconnect Prediction (SLIP) Workshop, 2019
- Technical track chair
  IEEE International System on Chip Conference (SOCC), 2019-2021
  ACM Great Lakes Symposium on VLSI (GLSVLSI), 2019
  IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), 2018-2019
- Technical program committee member
  ACM/IEEE Design Automation Conference (DAC), 2020-2021
  IEEE Nordic Circuits and Systems Conference (NORCAS), 2019-2021
  IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), 2019
  IEEE International Symposium on Quality Electronic Design (ISQED), 2015-2021
  ACM Great Lakes Symposium on VLSI, 2013-2021
  ACM/IEEE System Level Interconnect Prediction (SLIP) Workshop, 2015-2021
  IEEE International Symposium on Circuits and Systems (ISCAS), 2017-2021
  IEEE Computer Society Annual Symposium on VLSI, 2014-2015
- Special session chair
  IEEE Computer Society Annual Symposium on VLSI, 2021
- Special session organizer
  Machine Learning Based Side Channel Attacks and Countermeasures at DAC'20
  Powering Heterogeneous IoT Systems: Design for Efficiency, Security, and Sustainability at GLSVLSI'18
  Efficient IoT Systems: The Power of Heterogeneous Integration at GLSVLSI'17

- Finance chair
  ACM Great Lakes Symposium on VLSI, 2019
- Tutorial chair
  IEEE International System on Chip Conference (SOCC), 2020
- Student forum chair
  IEEE Computer Society Annual Symposium on VLSI, 2019
- Panel chair
  ACM/IEEE System Level Interconnect Prediction (SLIP) Workshop, 2018
- Publications chair
  ACM/IEEE System Level Interconnect Prediction (SLIP) Workshop, 2017
- Local arrangement chair
  IEEE Computer Society Annual Symposium on VLSI, 2014
- External reviewer
  Journals: *IEEE Journal of Solid-State Circuits (JSSC)*, *IEEE Transactions on Power Electronics (TPEL)*, *ACM Computing Surveys*, *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, *IEEE Transactions on Very Large Scale Integration (VLSI) Circuits (TVLSI)*, *IEEE Transactions Circuits and Systems-I (TCAS-I)*, *IEEE Transactions Circuits and Systems-II (TCAS-II)*, *IEEE Transactions Computer-Aided Design (TCAD)*, *IEEE Electron Device Letters (EDL)*, *ASP Journal of Low Power Electronics (JOLPE)*, *Analog Integrated Circuits and Signal Processing*, *Integration, the VLSI Journal*, *IET Circuits, Devices & Systems*, *Microelectronics Journal*
  Conferences: International Conference on Computer-Aided Design (ICCAD), International Symposium on Quality Electronic Design (ISQED), Design, Automation and Test in Europa (DATE), International Conference on Circuits and Systems (ISCAS), International Conference on Computer Design (ICCD), System-on-Chip Conference (SOCC), Asia Pacific Conference on Circuits and Systems (APCCAS), International Workshop on Power And Timing Modeling, Optimization and Simulation (PATMOS), Asia Symposium on Quality Electronic Design (ASQED), International Symposium on Networks-on-Chip (NOCS), Great Lakes Symposium on VLSI (GLSVLSI), International Conference on Very Large Scale Integration (VLSI-SOC)
- Professional Societies
  Member, IEEE
  Member, ACM
  Member, NAI

Service

International

- External reviewer for Israel Ministry of Science, Technology and Space, 2016
- External reviewer for Israel Science Foundation, 2017

National

- Participant at the "CCC/SIGDA Workshop on Extreme Scale Design Automation" visioning workshop (invitation only), organized by ACM special interest group on design automation (ACM/SIGDA), 02/21-22/2014
- NSF Panelist, 2014, 2015, 2016