Sigma Delta Image Sensor

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SENSORS

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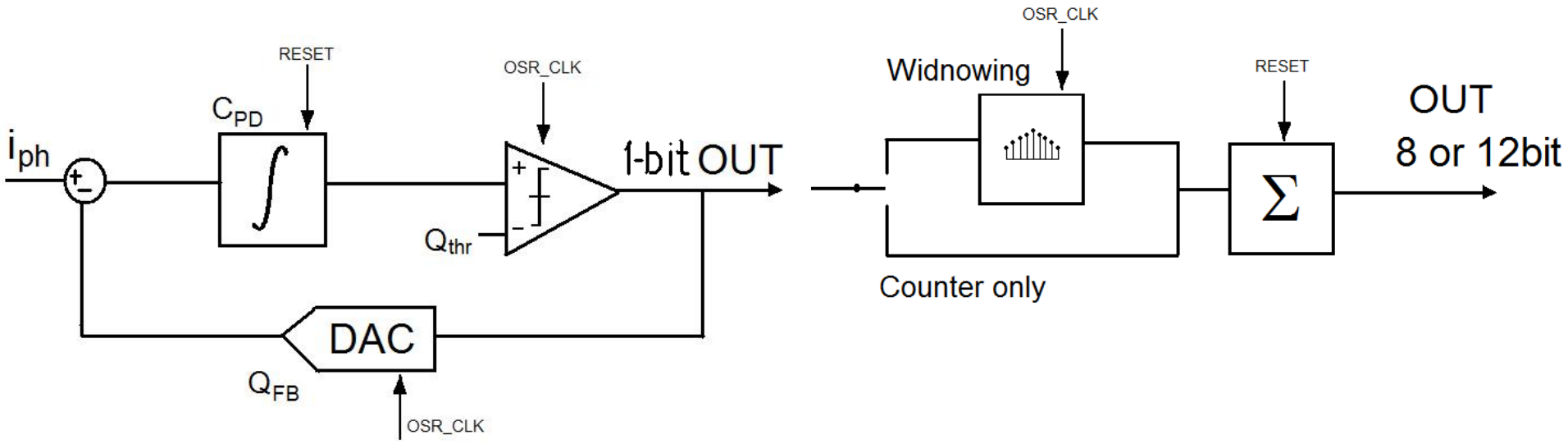
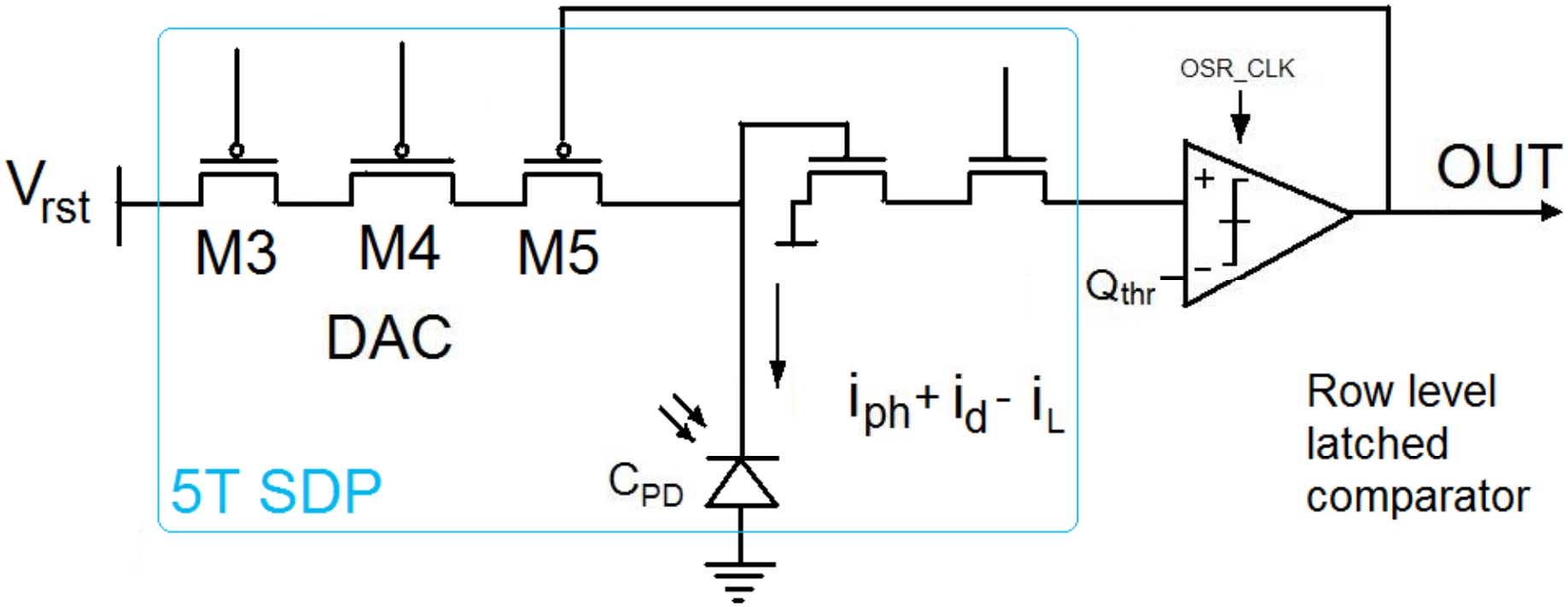
Sigma Delta Pixel (SDP)



5T SDP Implementation



5T SDP 0.35um 10x10um

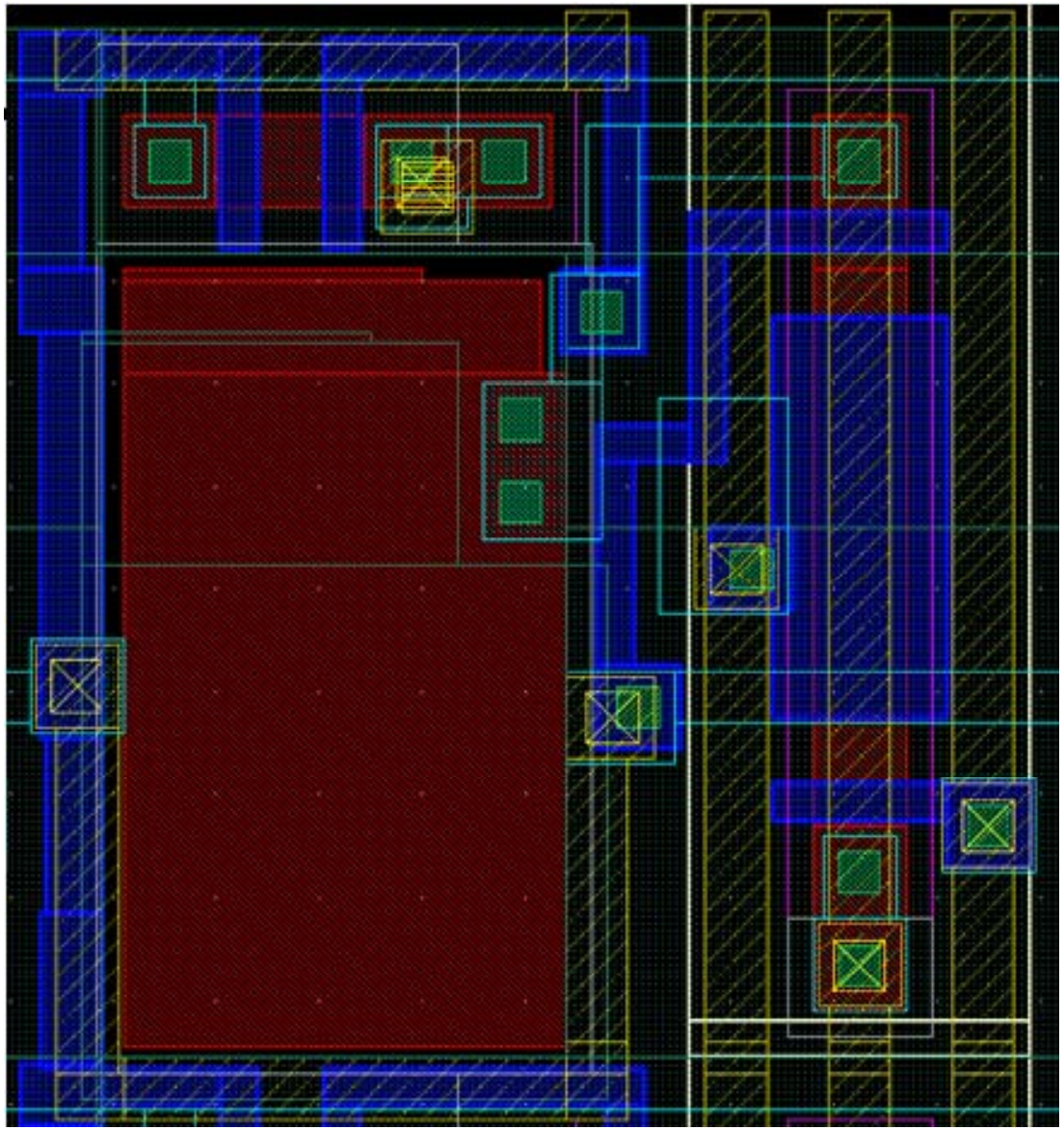
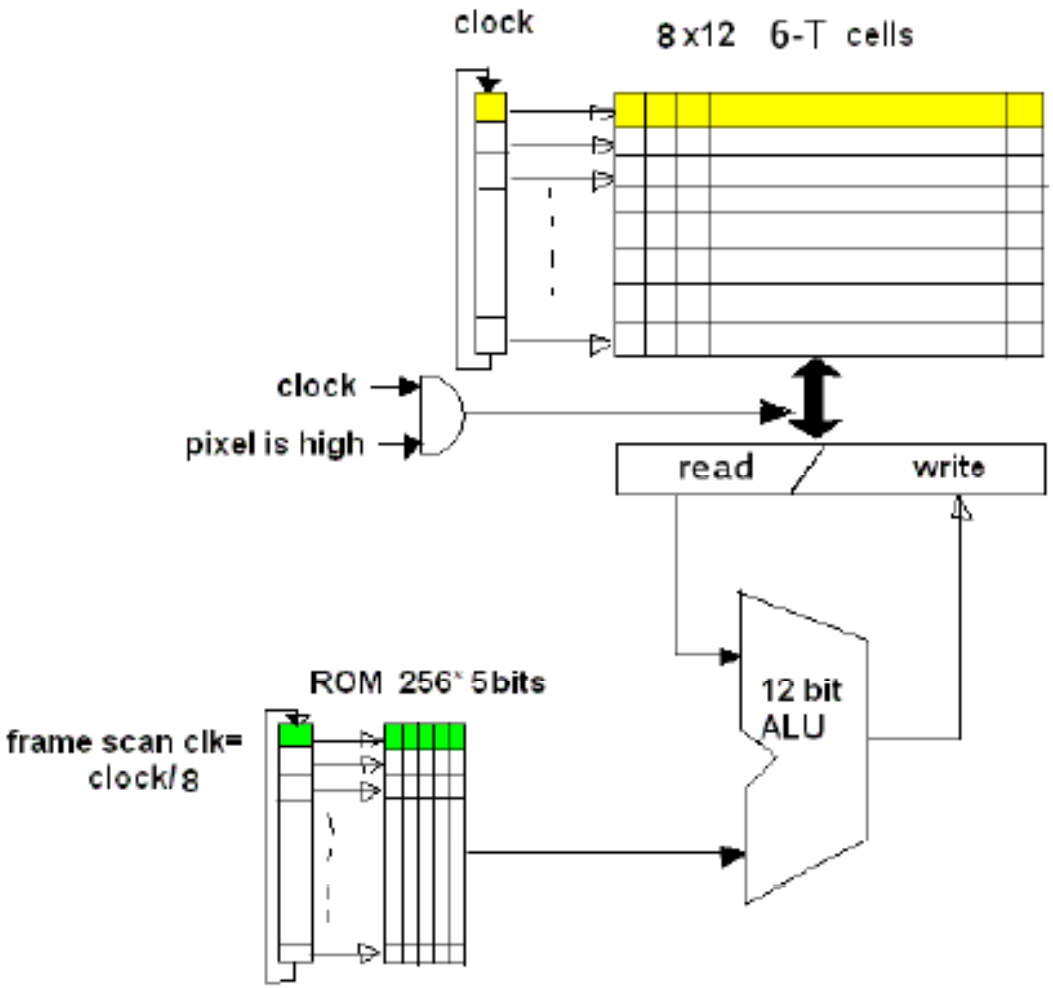
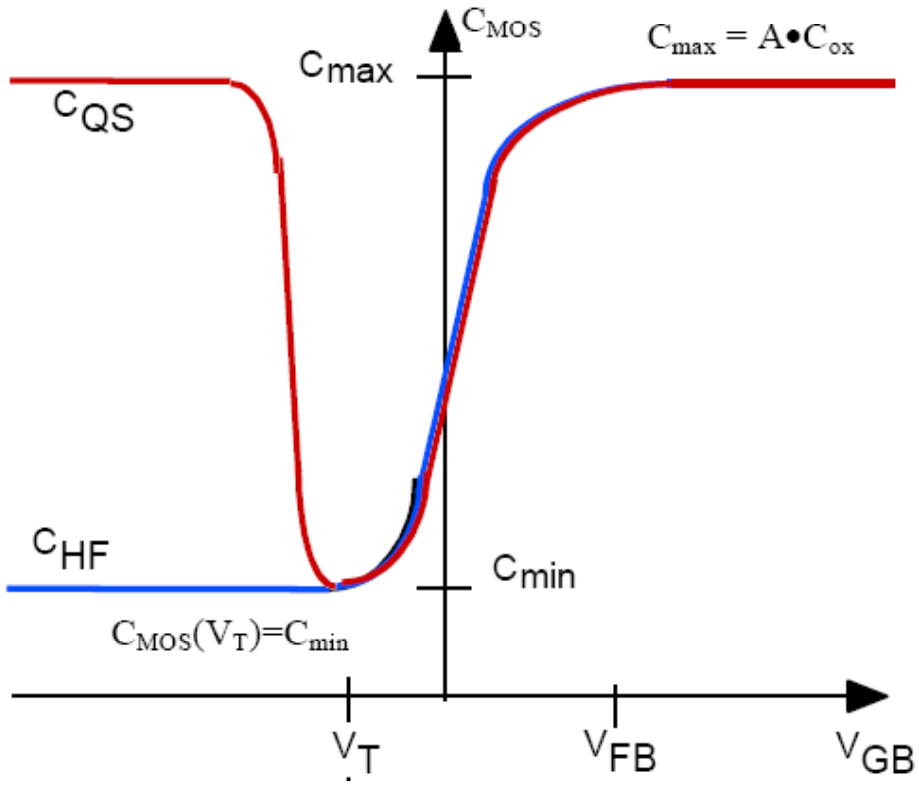


Image Accumulator Architecture (now off-chip on FPGA)



MOSCAP within DAC

DAC gain can not be controlled by Vgs of MOSCAP M4: When Vgs is bellow Vt, high FPN appears



Noise model

$$i_{pd} = i_{ph} + i_d - i_{leak}$$

$$Q_{fb} = V_{reset} C_{moscap}$$

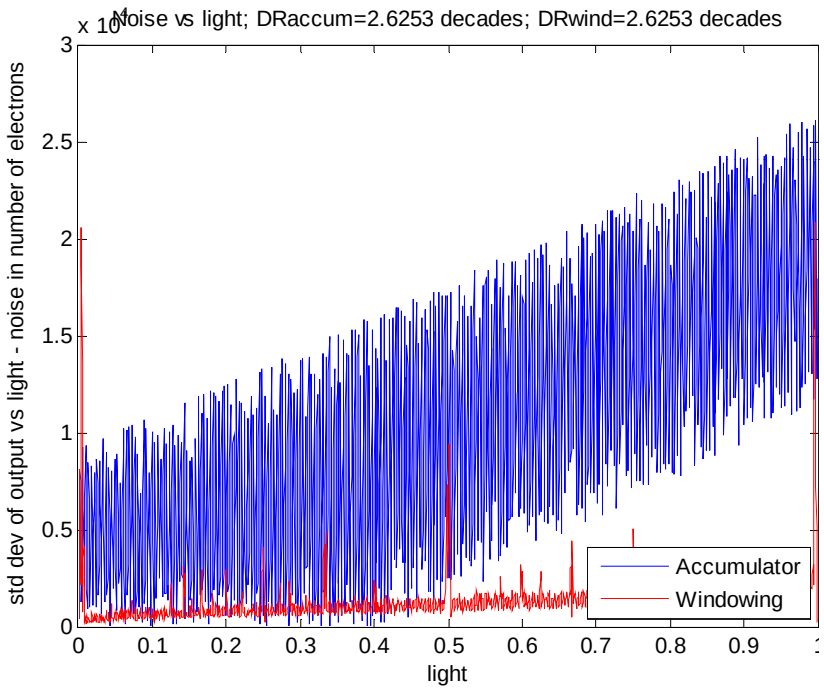
$$\sigma_{fb} = \frac{\sqrt{kTC_{moscap}}}{q}$$

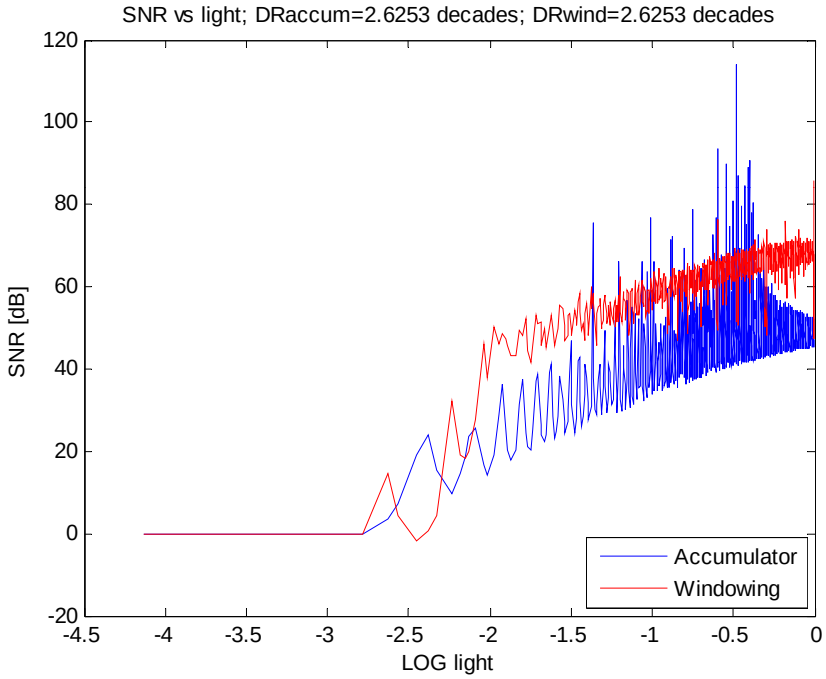
$$\sigma_{reset} = \frac{\sqrt{kTC_{pd}}}{q}$$

$$\sigma_r = \sqrt{\frac{Q_{fb}^2}{12q^2} + n\sigma_{fb}^2 + \sigma_{reset}^2}$$

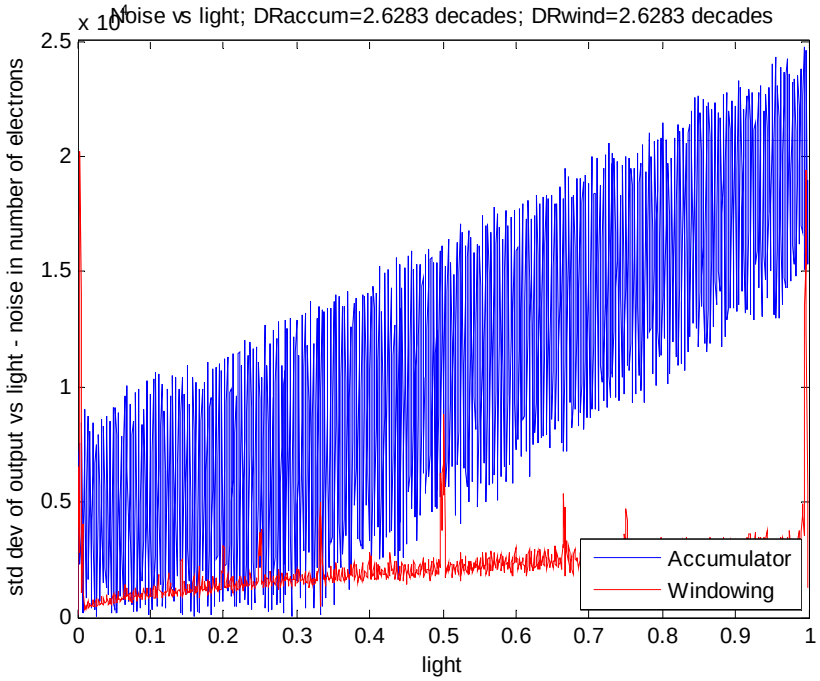
$$SNR = 10log\frac{(i_{pd}t_{exp})^2}{qi_{pd}t_{exp} + (q\sigma_r)^2 + (nq\sigma_{sw})^2}$$

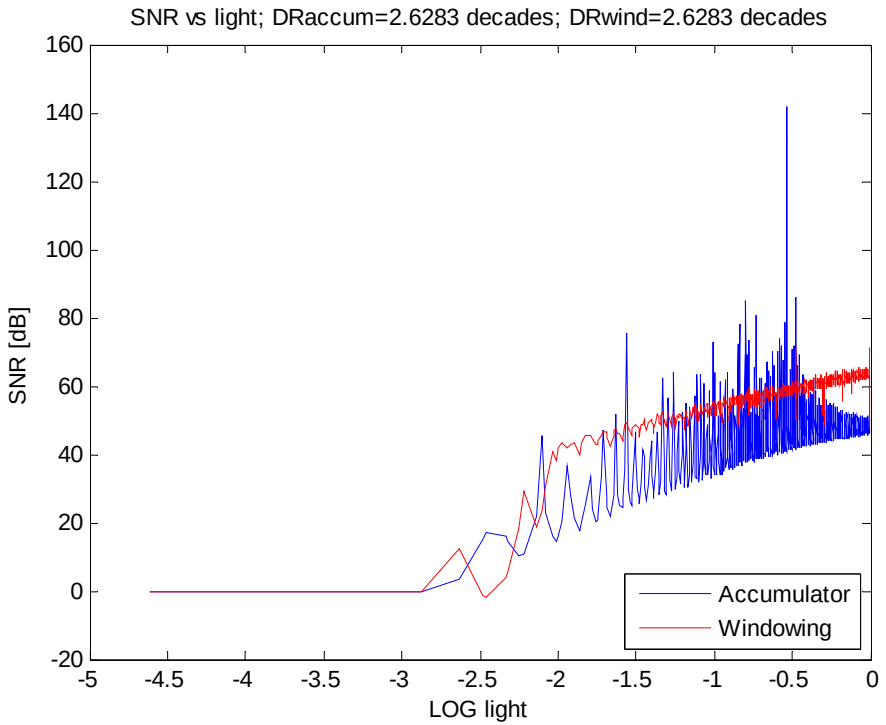
SD quantization noise and kTC noise for kTC=54 e^- OSR=256 and DAC=19000 e^-



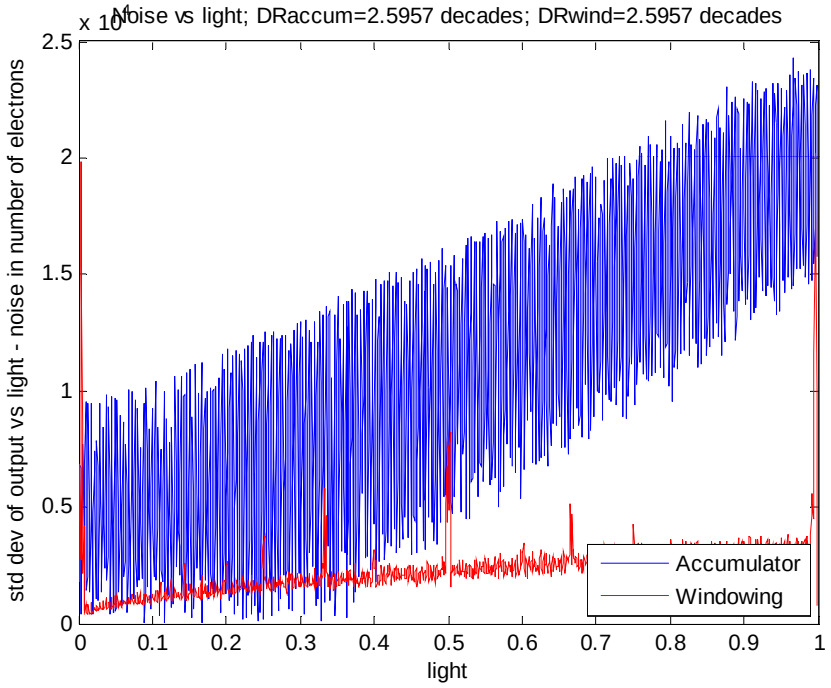


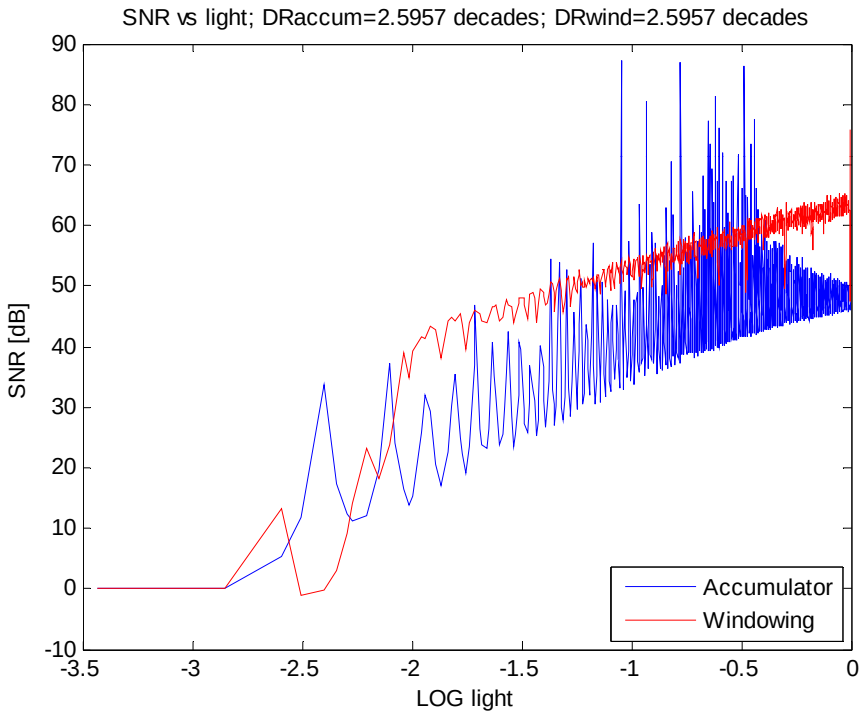
SD quantization noise and Photon shot noise for OSR=256 and DAC=19000 e^-





SD quantization noise, Photon shot noise and kTC noise for kTC=54 e^- OSR=256 and DAC=19000 e^-





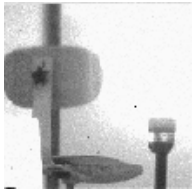
Raw Image 6bit/pixel (OSR=64)

Corrected by frame subtraction

Raw image minus uniform image

Exposure and DAC gain variations

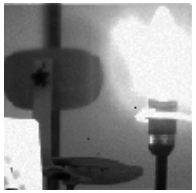
ON08V1over4MHz



ON08V3over4MHz

ON08V7over4MHz

ON1V1over4MHz



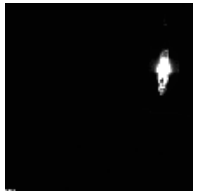
ON1V3over4MHz

ON1V7over4MHz

ON16V1over4MHz

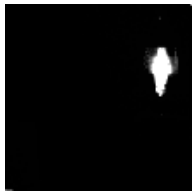
ON16V3over4MHz

ON16V7MHz

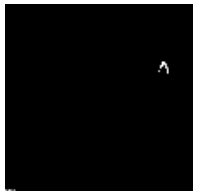


ON33V1over4MHz

ON33V3over4MHz

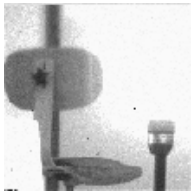


ON37V7MHz



Synthesized HDR images

ON08V1over4MHz

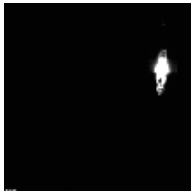


Synthesized WDR image, a1=0.5, a2=0.5

ON1V3over4MHz

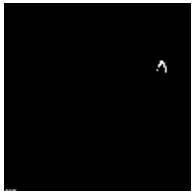
Synthesized WDR image, a1=0.3, a2=0.7

a16V7MHz



Synthesized WDR image, a1=0.25, a2=0.25, a3=0.25, a4=0.25

a37V7MHz



Synthesized WDR image, a1=0.4, a2=0.3, a3=0.2, a4=0.1

Specifications

- DR = 91dB maximum with variations of **DAC gain** (Vrst from 0.8V to 3.7V) and **exposure time** variations from 1ms to 14ms (28ms) per 1-bit frame
- PSNR = 51dB (62 expected with windowing)
- Low power for the imager array 0.88nW/pixel

DR needs improvement

DR can be better if low light responsivity is improved.

To be explored:

- Leakage needs to be reduced (M6 between M5 and PD; Vrst contact to be increased)
- Compensate for leakage by Vthr ramp
- Use image sensor technology for better sensitivity (TSMC35: 0.2V/(Lux*sec))
- DAC charge packet is the ultimate resolution limit (19Ke now) – Test pixels with smaller MOSCAP
- Imager readout needs to be faster then 1ms per 1-bit frame (new comparator) – this would extend DR at high end
- Accumulator needs to be synthesized and fabricated as SoC