Design of a test platform for two dimension arithmetic Fourier transform image sensing in CMOS, redux

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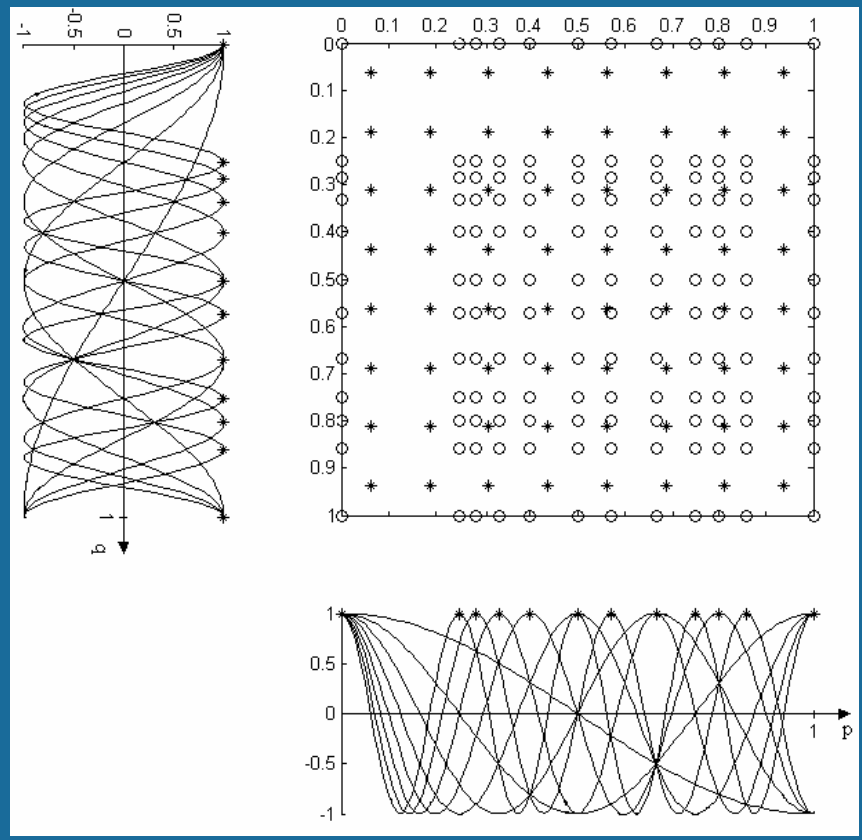
Previously…

- Problem
  - DCT is power hungry because of the multiplications needed
- Solution
  - Use AFT to compute DCT coefficients by using additions (Tufts, 1988)
    - Gains in terms of speed and power consumption

AFT requirements

- Integer scaling
- Non-uniform sampling for 2D AFT
  - Pixels placed at Farey sequence locations
- Compared to conventional DCT, more samples needed

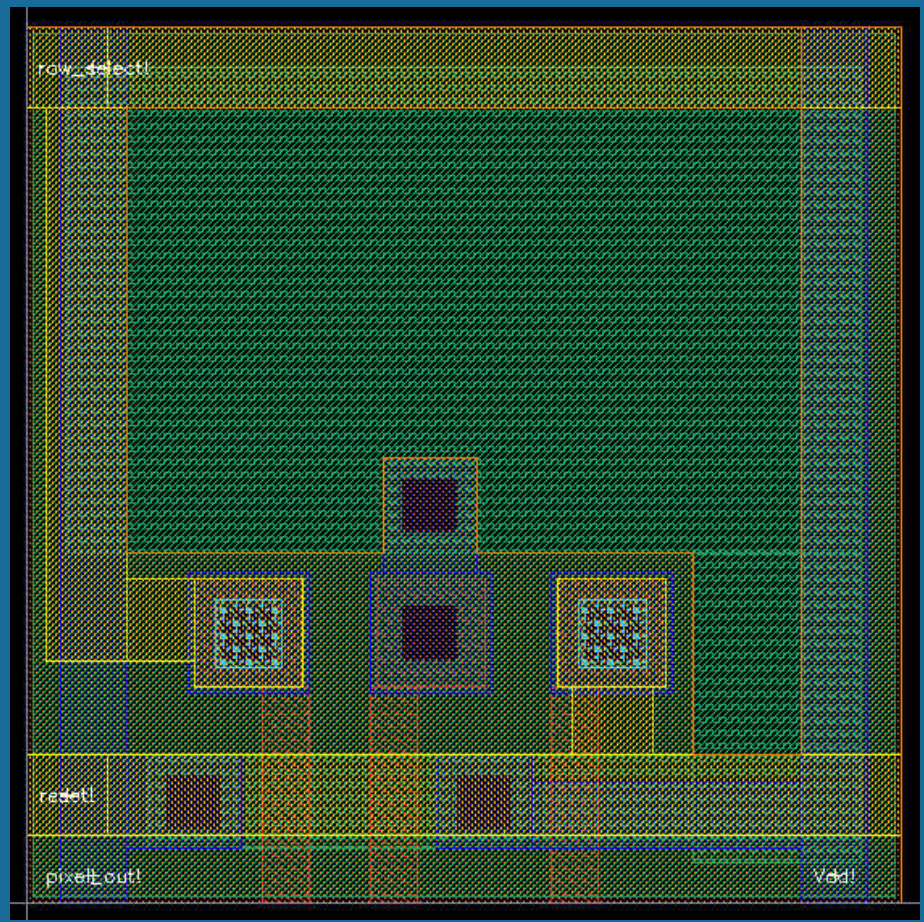


Coroner's findings

- Missing layout layers for TSMC 0.35µm silicide process
- Insufficient, missing nMOS Vss connections in output buffer
- TSMC 0.35µm silicide process does not support double polysilicon
- Digital logic functioning properly

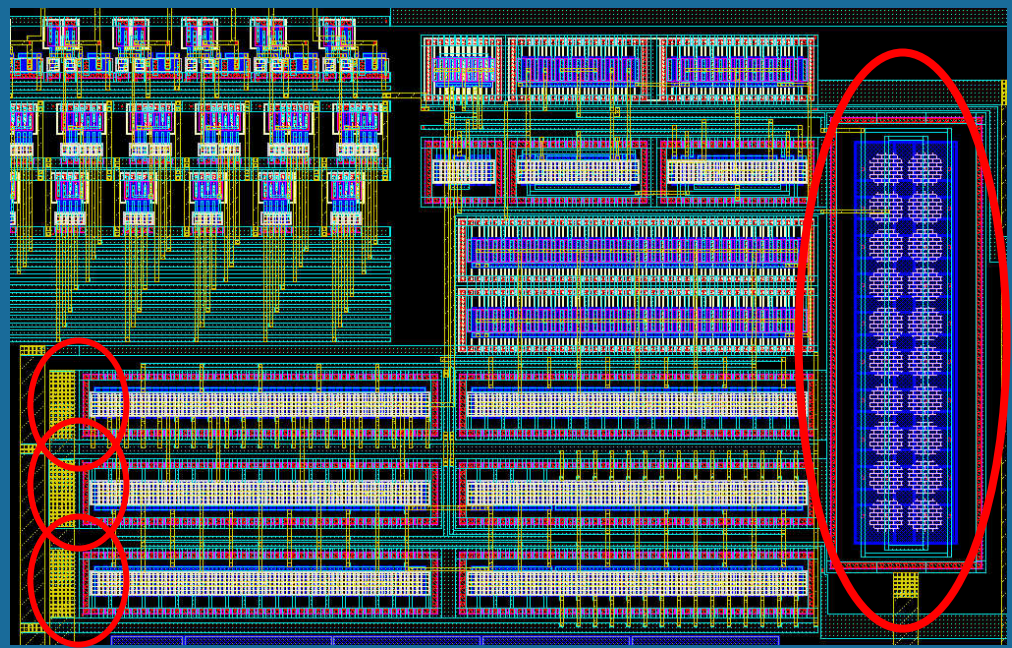
Missing fabrication layers

- Resist protection oxide (RPO)
- 3V N+ implant lightly doped drain (NLDD_3V)



2-stage op amp as output buffer

- nMOS transistor fingers not connected to Vss
- 1pF poly-poly capacitor cannot be fabricated with single poly process



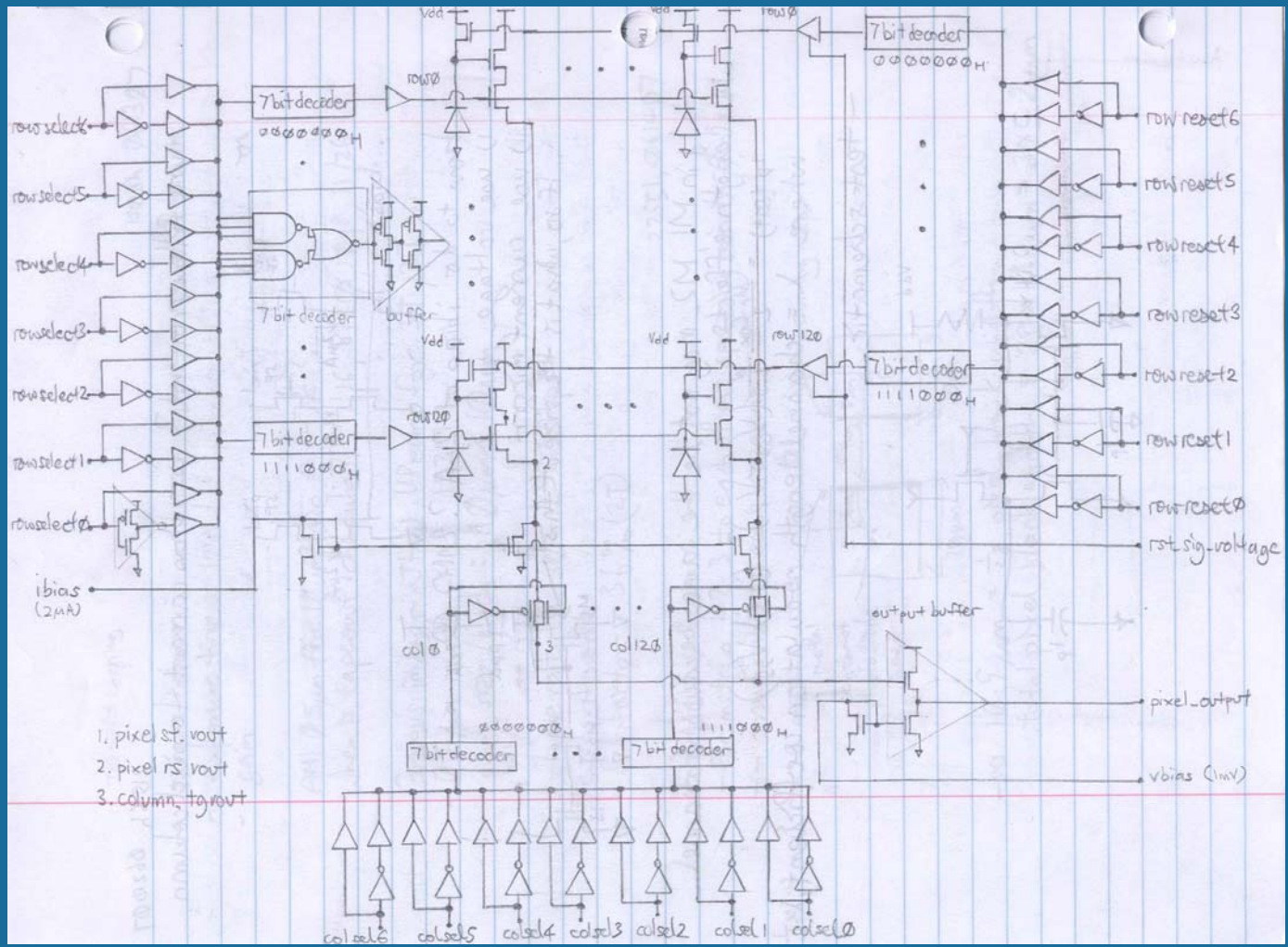
Transistor fingers unconnected to Vss

1pF poly-poly capacittor

Rebuilding

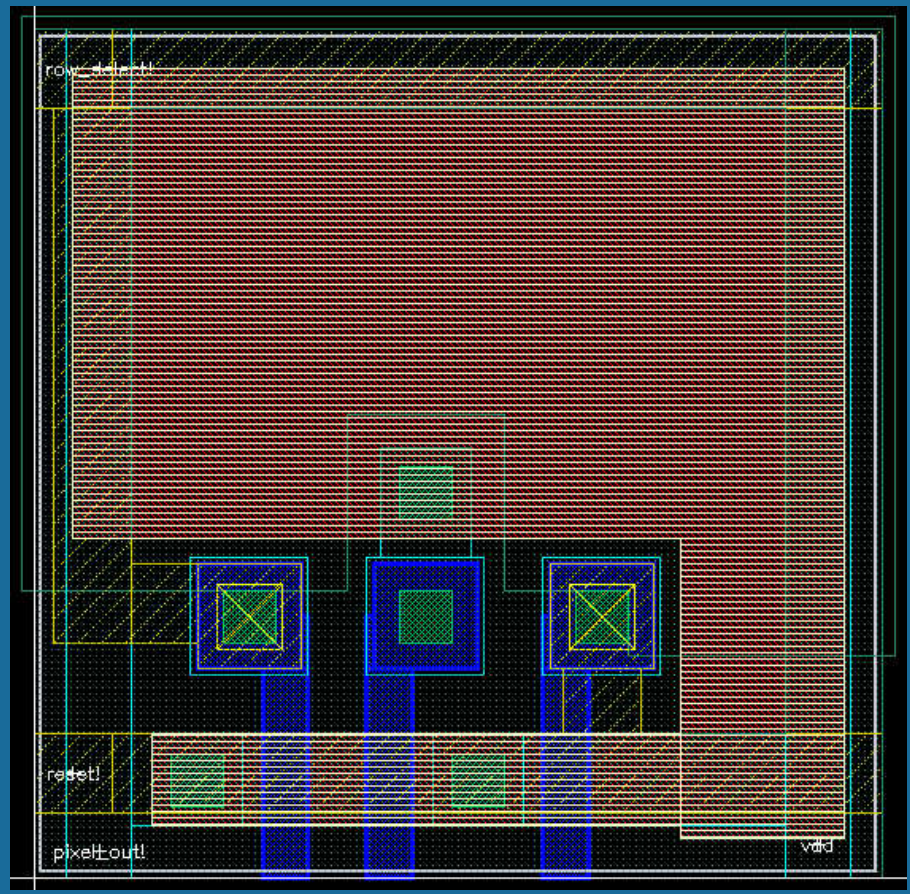
- Add layout layers for TSMC 0.35µm silicide process
- Redesign output buffer
- Redesign pixel source follower bias current
- Add test structures
- Add dummy pixels

Block diagram



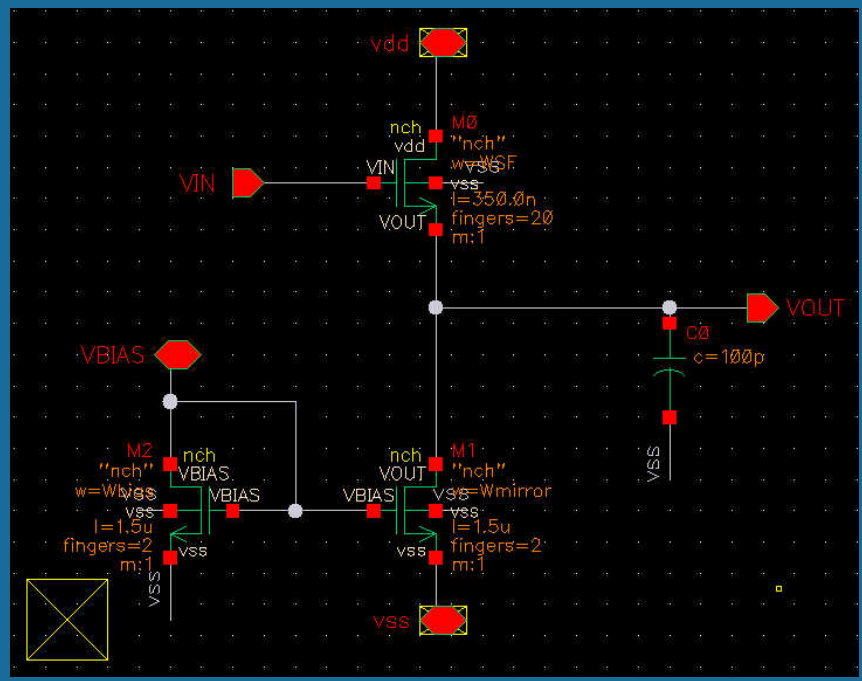
L shaped 3T pixel

- Resist protection oxide (RPO)
- 3V N+ implant lightly doped drain (NLDD_3V)
- wellbody

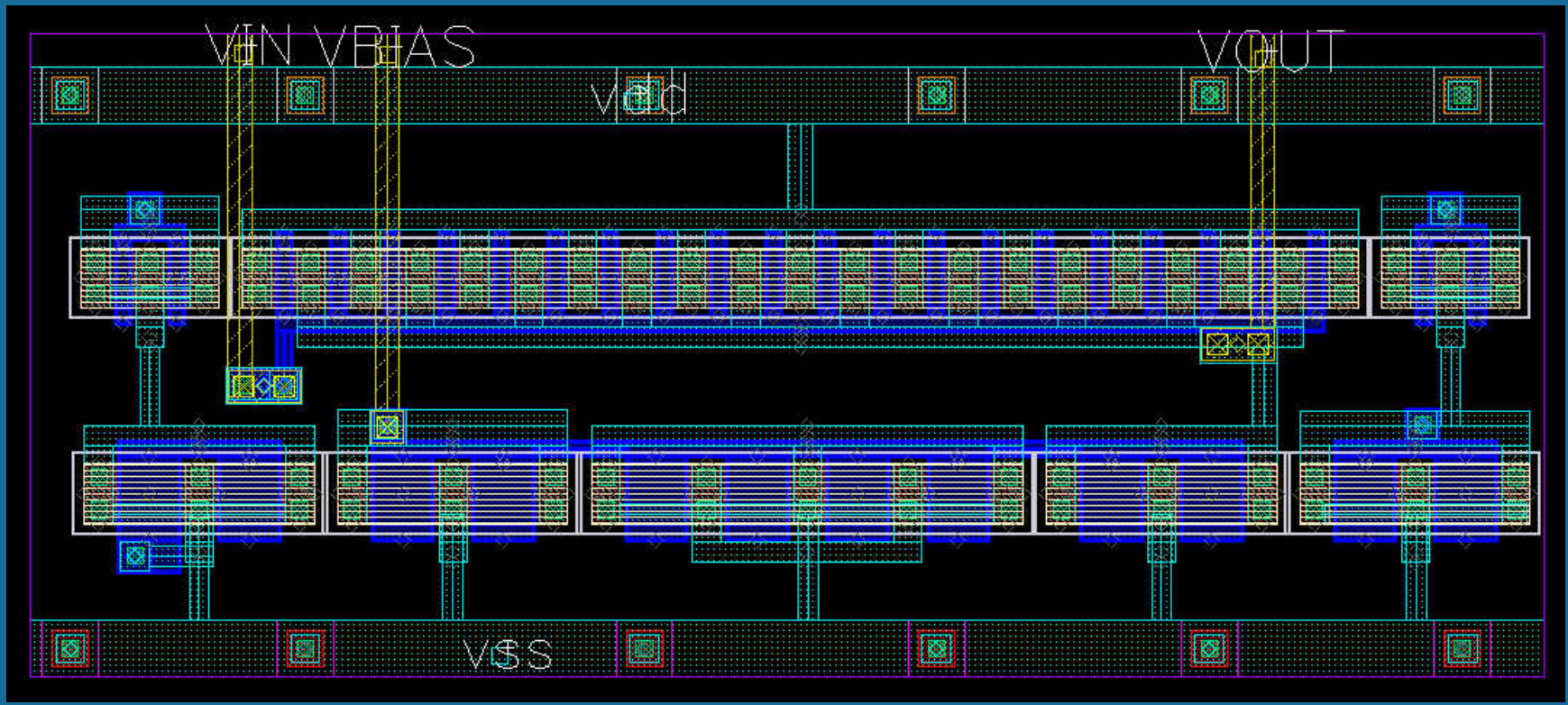


nMOS source follower output buffer

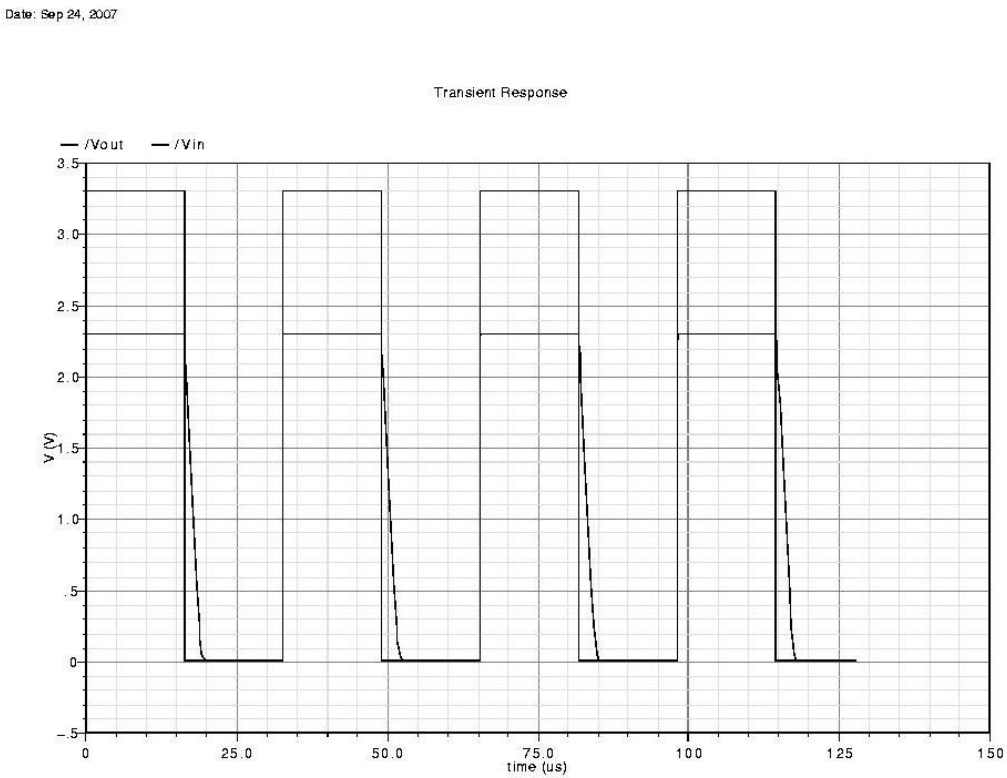
- dc gain of -3.1dB with 100pF load
- 1V bias voltage



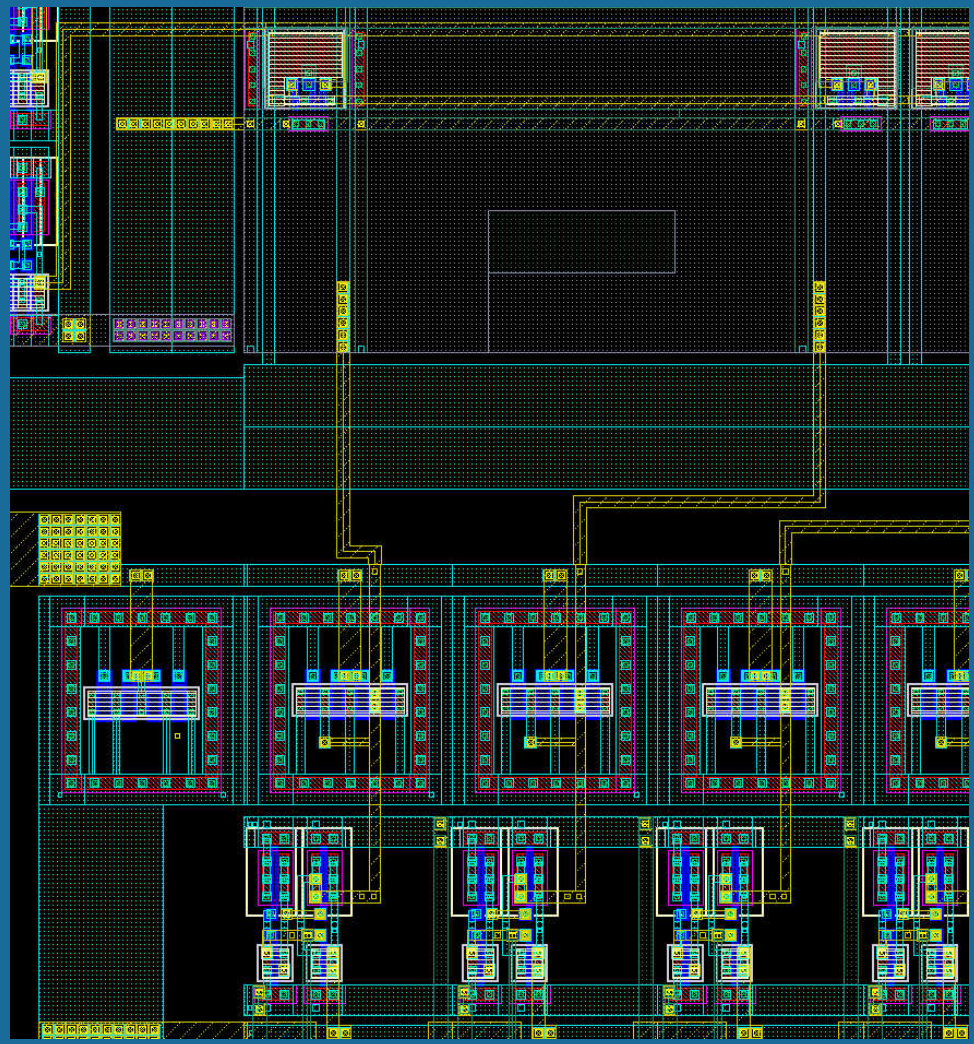
nMOS source follower output buffer



Source follower output buffer transient results



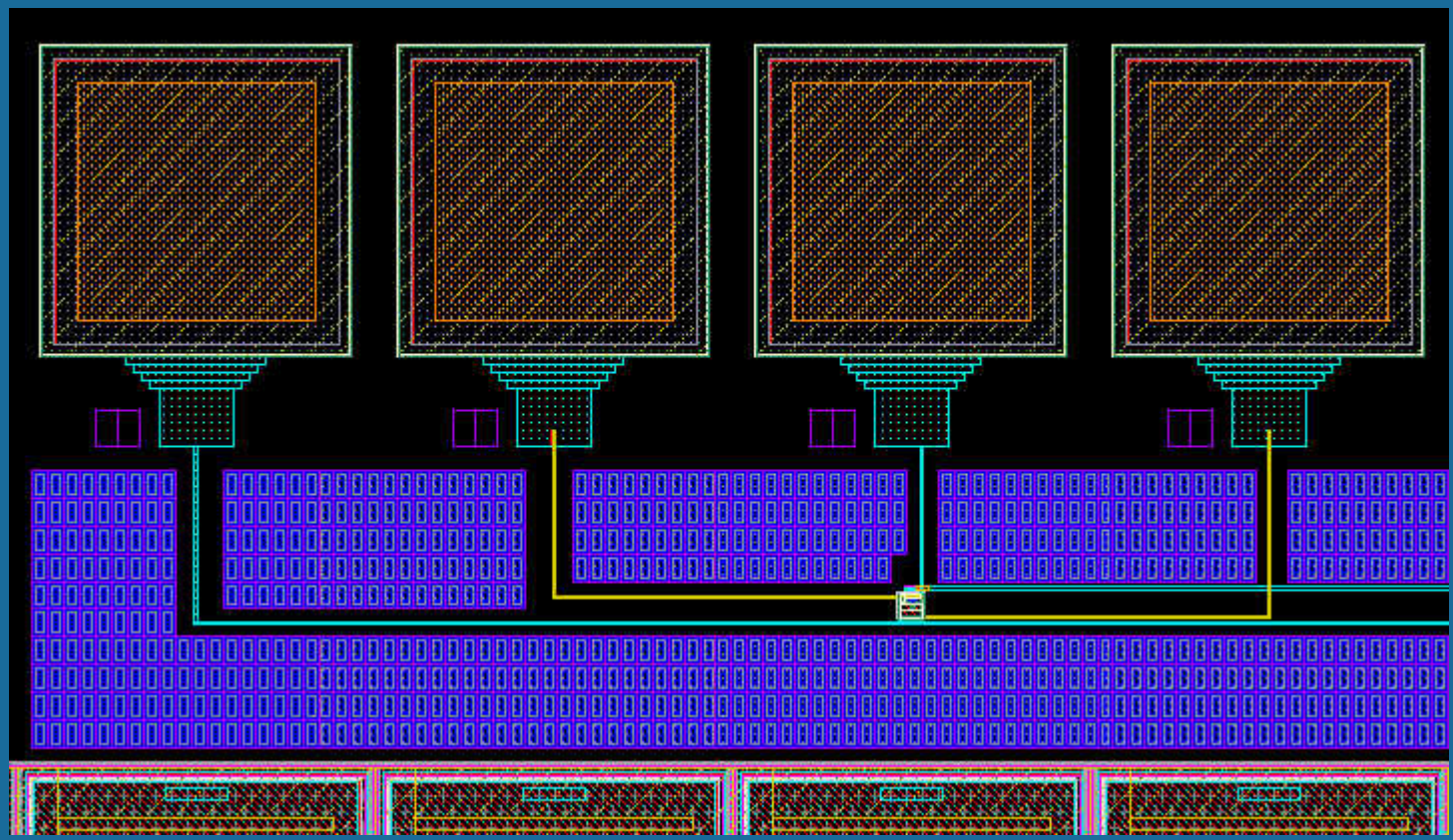
Pixel source follower bias current



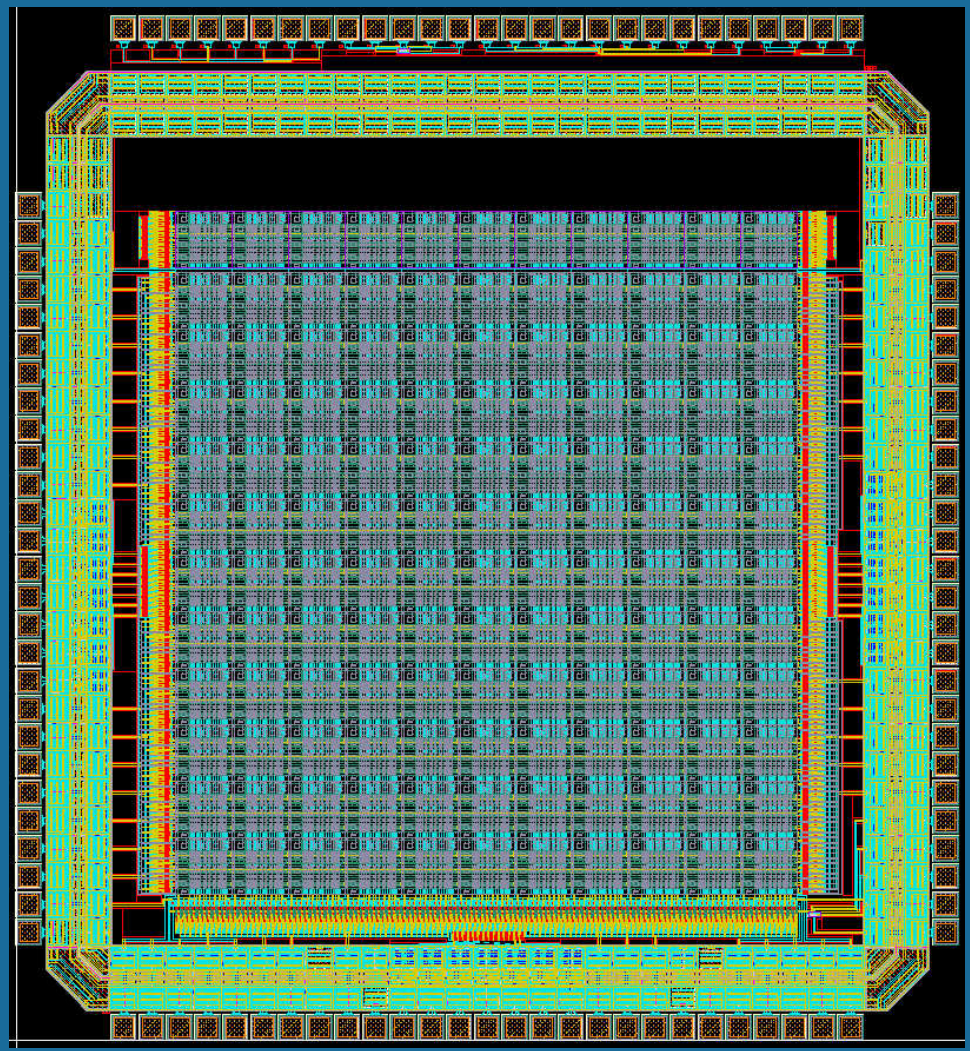
Test structures

- Located on north orientation of chip
- Electrically isolated from the rest of the sensor
  - A mix of bonded and unbonded chips
- 5 circuits
  - L photodiode pixel
  - Circle photodiode pixel
  - nMOS source follower output buffer
  - 7-bit static row decoder
  - Row driver

Test structure (L photodiode pixel)



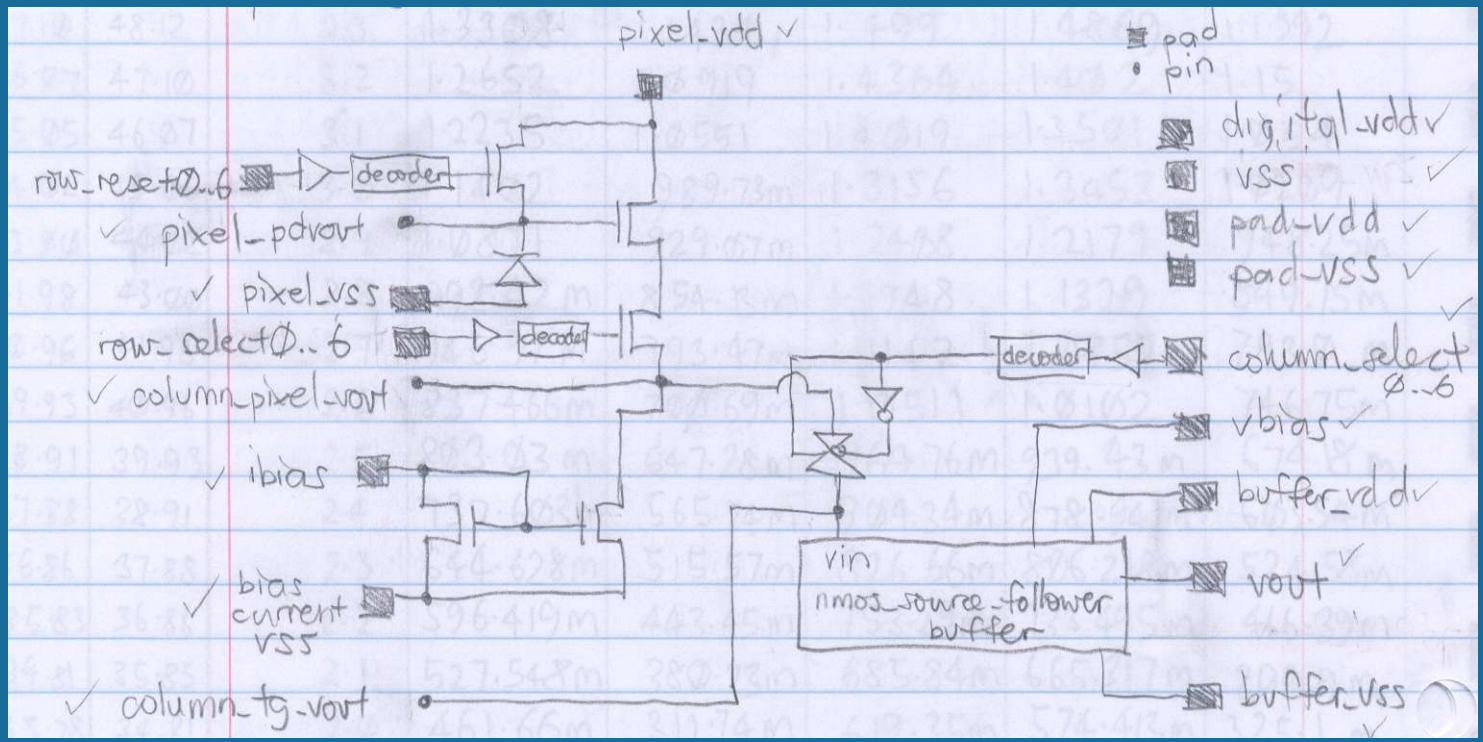
2-dimension AFT APS imager rev5



Simulation

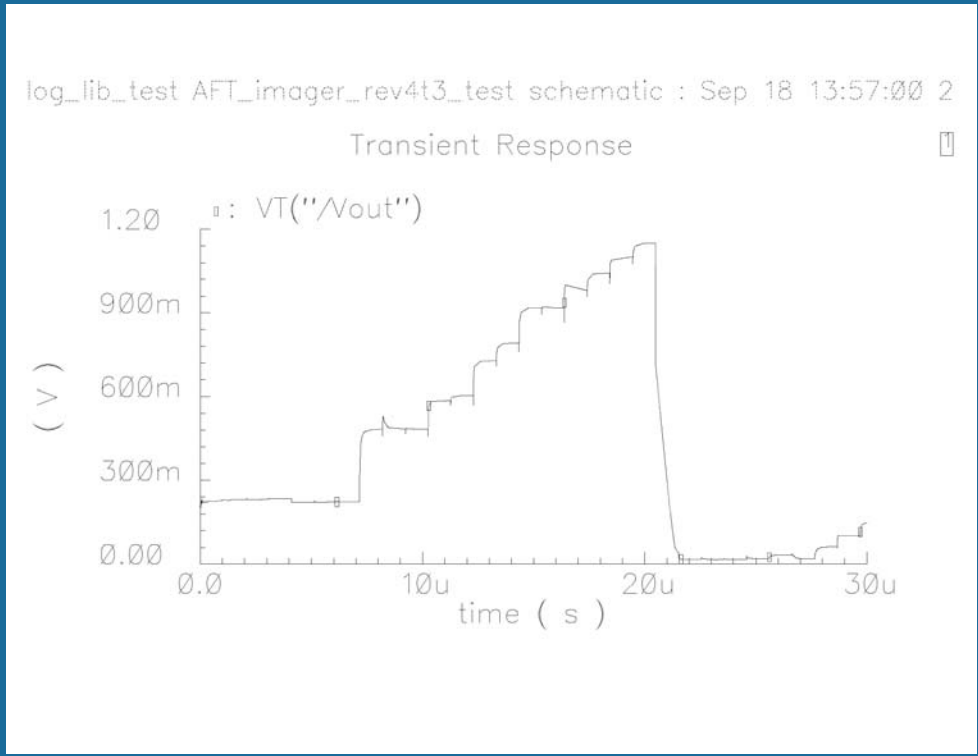
- Methodology
  - Simulate av_extracted view of entire imager in Cadence
  - Simulate photodiode voltage with “external” input pin
  - Simulate each pixel with a different voltage ranging from 3.3 to 1.0V

Simulation schematic



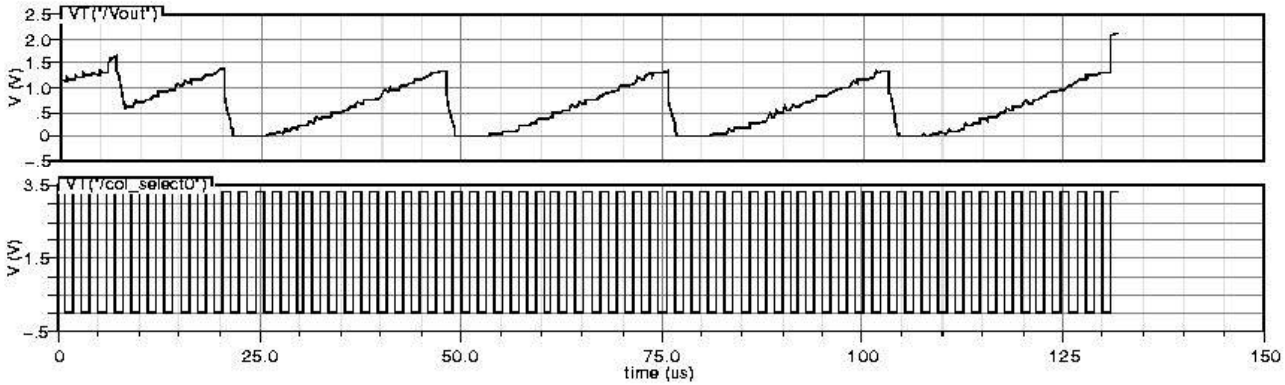
Simulation results

- 121 x 121 pixel array with pad frame



Simulation results

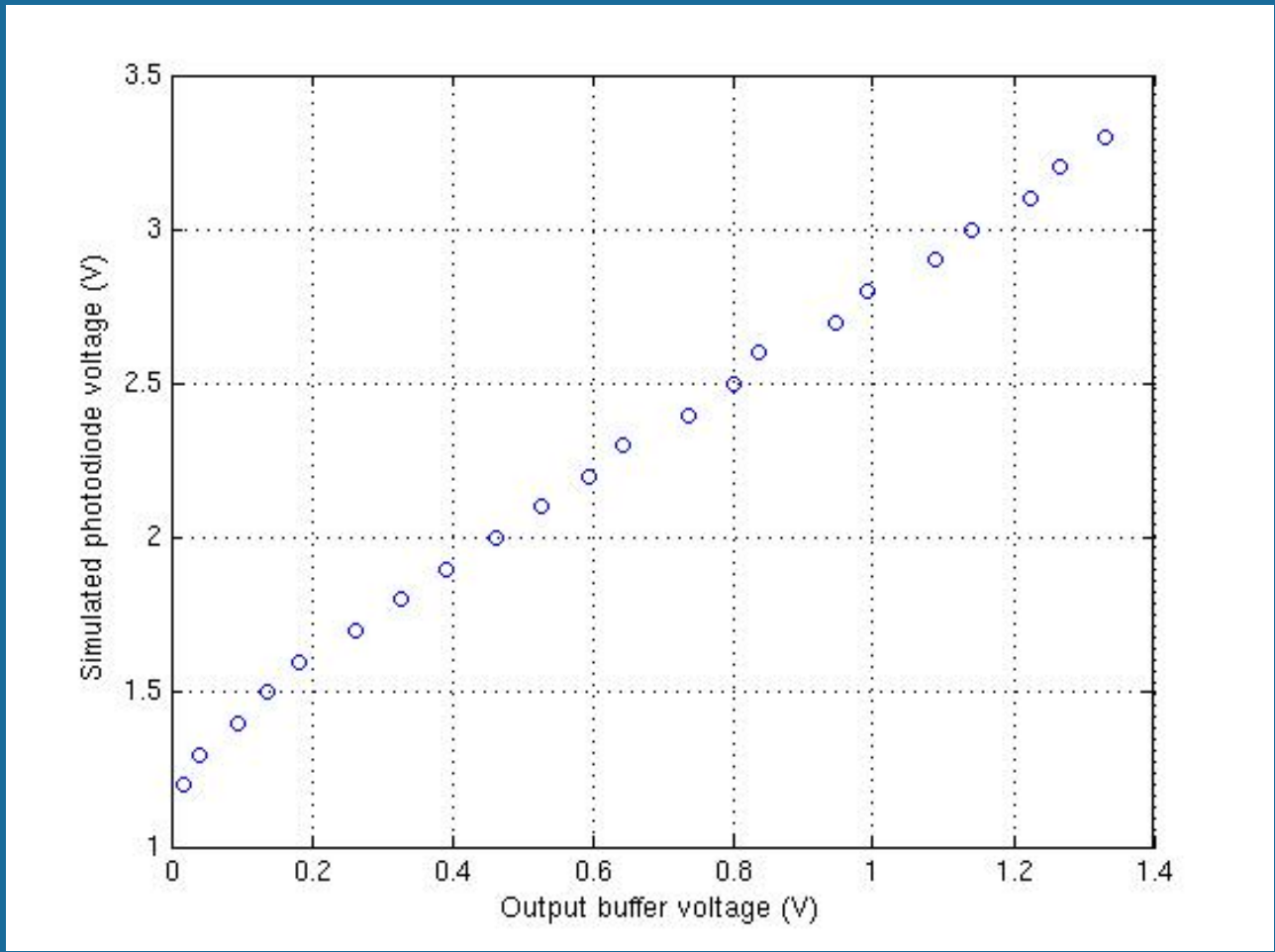
- 121 x 121 pixel array without pad frame



Pixel dynamic range

- Plot photodiode voltage versus imager output voltage
- Fit best straight line with each data point keeping within 3% deviation/error

Linear response of pixel signal path



Current and future work

- Redesign imager sensor evaluation board
  - New output buffer requires biasing voltage
  - 108pin pin grid array (PGA) package
  - Surface mount technology (SMT) devices to reduce board size and cost
- Simulate AFT imaging with standard CMOS camera-based APS sensor

Evaluation board block diagram